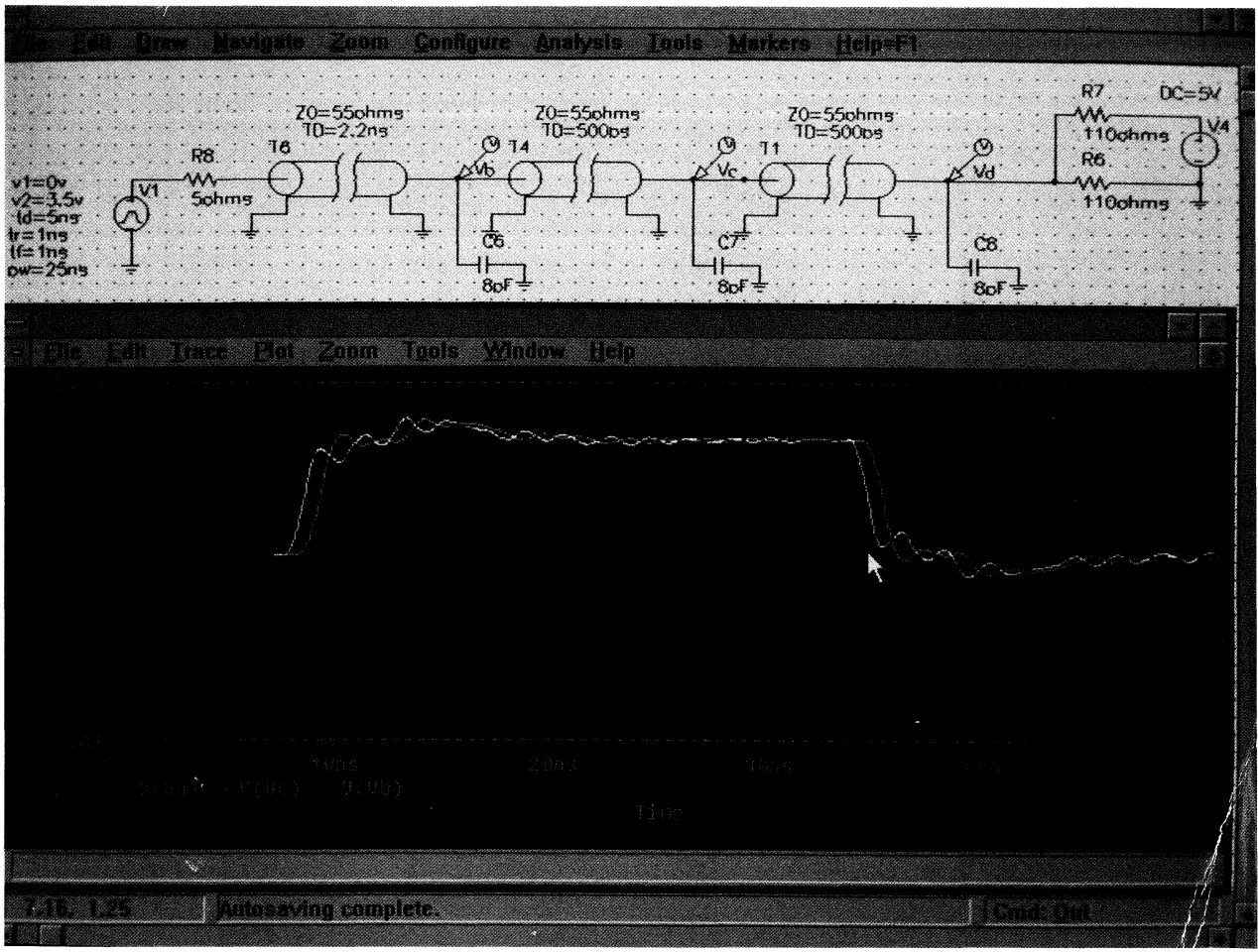
SPICE I/O Models for 5 Volt and 3.3 Volt Standard Logic Families



1995

DATA MANUAL

Philips Semiconductors

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SPICE I/O Models for 5 Volt and 3.3 Volt Standard Logic Families

CONTENTS

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Printed in USA

Preface

SPICE

This manual is version 1.0 of the SPICE I/O modeling guide for our 5 volt BiCMOS logic families: ABT, ABT16, 3 volt BiCMOS logic families: LVT, LVT16; 3 volt CMOS logic families: LV, LVC, HLL, and ALVC; and the 5 volt HCMOS family. The models in this manual and the accompanying diskettes are intended to provide modeling information that will assist system designers with interconnection evaluations. This includes transmission line effects and device response to circuit loads. It is also our intent to provide models which are practical to use.

This manual contains models which accurately represent device interfaces to the outside world. Since we provide only input and output models in this manual, the functionality of devices is not simulated, and AC speeds may not meet published specifications. For more detailed electrical characteristics, see the data handbook for the particular product family of interest.

Process variations can cause parts to operate differently from their typical conditions. Therefore, we have provided model options for the nominal, fast, and slow process corners of our devices.

Since continuous improvement is a key policy of Philips, we are improving our SPICE models regularly, so please contact your Philips Semiconductors sales representative for the latest version of our SPICE models.

We want to be **your first choice for the products we provide**. Please let us know what we can do to meet your needs. Thank you for your interest in our products.

Standard Logic Product Group

Section 1
Introduction

CONTENTS

Introduction

The products in our ABT, ABT16, LVT, LVT16, LVC, HLL, and ALVC families offer you all the benefits of QUBiC, our truly integrated advanced BiCMOS process, and all the benefits of our advanced sub-micron CMOS process. They offer very high speed, low power, and high dynamic output drive. In order to assist designers in their design activities, we have provided SPICE models which simulate input and output characteristics of each device. Models are also included for our 5 volt HCMOS and 3 volt LV product families.

The models are included on the accompanying diskettes and are meant to be used on 386/486 and Pentium based PC compatible computers. If you do not have a copy of a particular diskette, please contact your local Philips Semiconductors sales representative.

MODEL INFORMATION

The attached diskettes contain all the files necessary to model the devices in this manual. Subdirectories for each product family contain the netlists needed to model that particular family. The first step would be to copy the files onto your fixed disk for more convenient use and access.

The models have been designed for easy use. Each major section of the book, except for packaging, contains netlists for that particular product family. Follow the instructions for that family.

Using the ABT family as an example, the main netlist is called ABTBS.CIR. In this file, the command ".INC C:\SPICE\ABT\MODN.BSP" references the Berkeley SPICE model library for ABT transistors, diodes, and other primitive elements. The other .INC command references ABT subcircuits that have capacitors and inductors connected to simulate a part in a package. The capacitors and inductors use default values that can be changed by the end user to fit the particular package being simulated. The Packaging section of the book gives information on these values.

The remainder of the file simulates a circuit that includes one part type with a standard AC test load resistor and capacitor connected. The input is connected to an AC voltage source, and the output signal can be observed to see the device's response to a standard 500Ω, 50 pF load. The circuit may be modified by the user to do other simulations such as transmission line effects on a printed circuit board by changing the input stimulus and output loading. Follow instructions in that file to begin running the program.

To run simulations on these models, you will need regular versions of SPICE software, since the models are too complicated for demonstration or evaluation versions of SPICE. Also, you will need a full circuit analog simulator rather than a small circuit analog version to run the LVT and LVT16 models due to their complexity and memory requirements.

Contents

Contents

Contents

Contents

Contents

Contents

Contents

Product Status

SPICE

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	**Formative or in Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

Section 2
ABT

SPICE

CONTENTS

Each ABT device requires some combination of an input stage, an output stage, possibly an inverting stage, and some parasitic reactance. Table 2-1 shows ABT model combinations that correlate input, inverting, and output structures for each part type. Dashes indicate that no inverting stage is needed.

Table 2-1. ABT Model Combinations

ABT	Input Circuit	Inverter Circuit	Output Circuit	Inverting Output	Subcircuit Name
125	A	–	A	No	BUFFER1
126	A	–	A	No	BUFFER1
240	A	A	A	Yes	INVBUFFER
240-1	A	A	B	Yes	INVBUFFER2
241	B	–	C	No	BUFFER2
244	B	–	C	No	BUFFER2
244-1	B	–	D	No	BUFFER3
245	B	–	C	No	BUFFER2
245-1	B	–	L	No	BUFFER4
273A	A	A	K	No	FLOP4
373A	A	A	K	No	FLOP4
374	A	A	K	No	FLOP4
377	A	–	E	No	FLOP1
534	A	–	C	Yes	INVFLOP
540	A	A	A	Yes	INVBUFFER1
541	B	–	C	No	BUFFER2
543A	A	A	K	No	FLOP4
544	A	–	F	Yes	FLOP5
573	A	A	C	No	FLOP2
574	A	A	C	No	FLOP2
620	A	A	A	Yes	INVBUFFER1
623	B	–	C	No	BUFFER2
640	A	A	A	Yes	INVBUFFER1
646	A	A	K	No	FLOP4
648	A	–	F	Yes	FLOP5
651	A	A	K	No	FLOP4
652A	A	A	K	No	FLOP4
657	B	–	F	No	BUFFER5
821	A	A	F	No	FLOP3
823	A	A	F	No	FLOP3
827	B	–	F	No	BUFFER5
833	B	–	F	No	BUFFER5
841	A	A	F	No	FLOP3
843	A	A	F	No	FLOP3
845	A	A	F	No	FLOP3
853	B	–	F	No	BUFFER5
861	B	–	F	No	BUFFER5
863	B	–	F	No	BUFFER5
899	C	–	F	No	FLOP6
2952	A	A	F	No	FLOP3
2953	A		F	Yes	FLOP5
5074	D	–	I	No	FLOP7

The data sheet section provides information on each ABT part type. Each data sheet contains a part description, part features, quick reference data, ordering information, pin configuration, logic symbol or diagram, and function table.

To do simulations on a particular part type, refer to the ABT SPICE Netlist section of the book. That section contains files called "ABTXX.CIR" which are simulation test circuits for individual device types. The files are also in the ABT directory in the attached diskette. The "XX" in ABTXX.CIR refers to BS, PS, or HS for the Berkeley SPICE, PSPICE, and HSPICE protocols. Figure 2-1 shows how the test circuits are assembled.

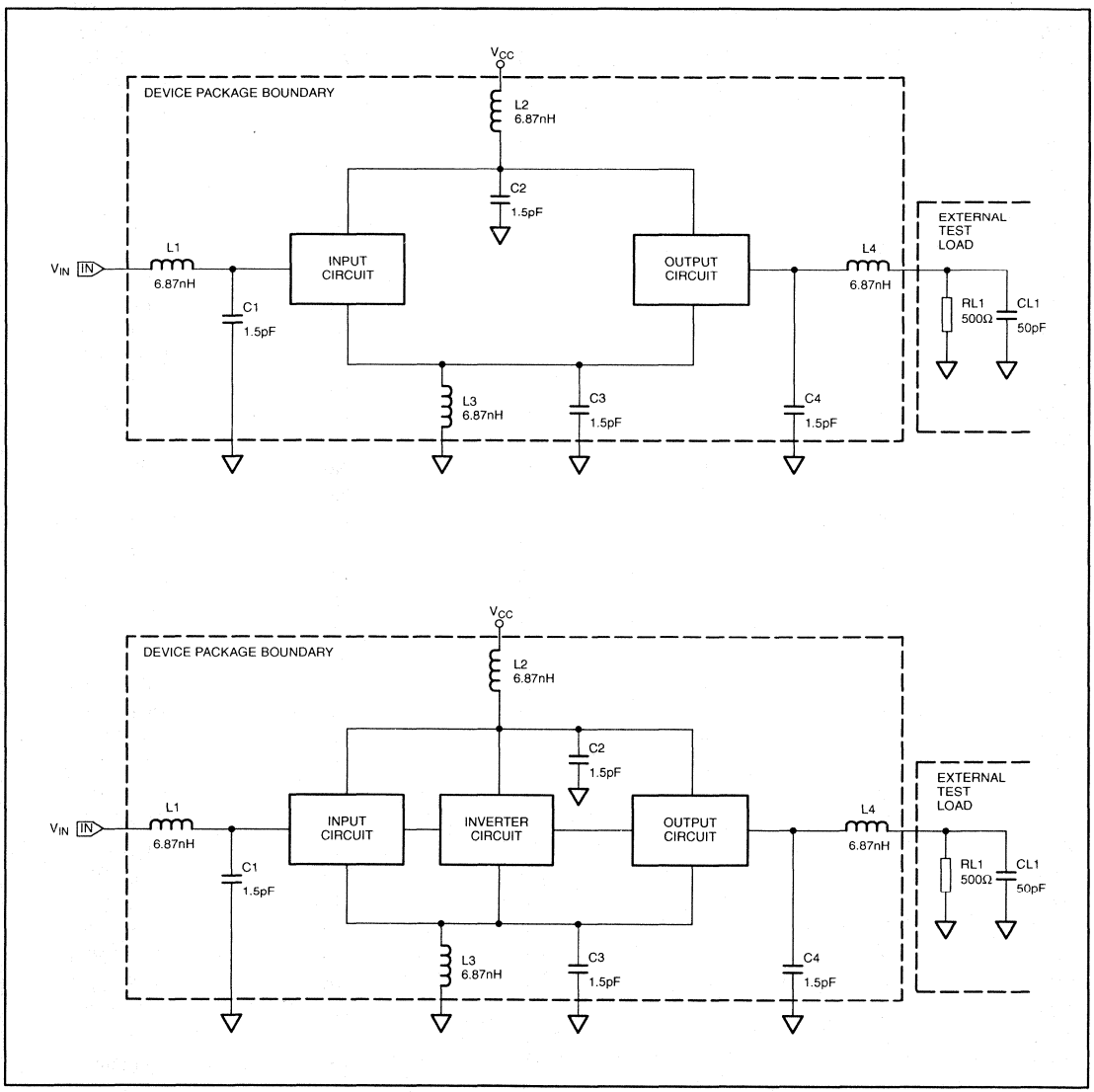


Figure 2-1. Example of Test Circuits

Netlists for subcircuits are also in the ABT Netlists section of the book. The subcircuit files are called ABTXXX.SUB and are also located in the ABT directory on the attached diskette. The "XXX" in ABTXXX refers to NOM, FAS, and SLO which represent the nominal, fast, and slow process corners. The files contain subcircuits for input, inverter, and output blocks, along with package parasitics representing a device in a package. The inductance values may be changed depending on the package used for a simulation. Refer to the Packaging section of the book for these values.

The libraries for transistors, diodes, and other primitive elements are included in the attached diskette in the ABT directory and are called "ABTMODX.XXX". The "X" in ABTMODX refers to N, F, and S for nominal, fast, and slow process corners. The "XXX" in the file extension refers to BSP, PSP, and HSP for the Berkeley, PSPICE, and HSPICE protocols.

The following illustration shows how the three programs interact with each other:

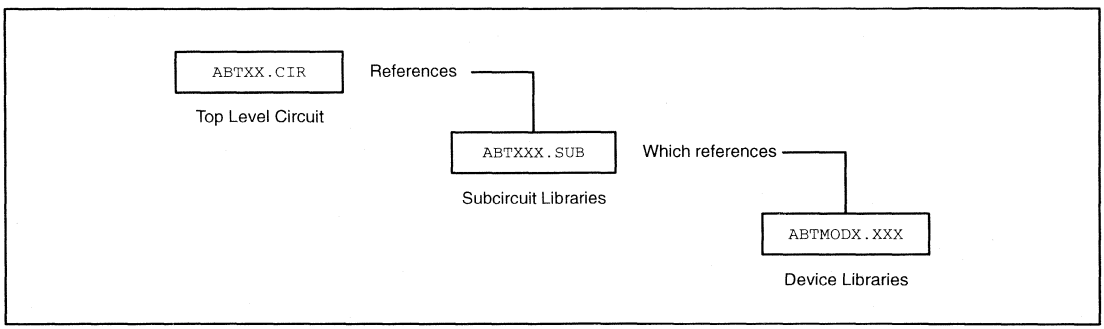


Figure 2-2. ABT SPICE Program Hierarchy

The top level program, ABTXX.CIR, uses standard data book AC test conditions with a square wave input of 3V, rise and fall times of 2.5ns, V_{CC} of 5V, but a period of 25ns. These conditions may be modified to suit the application. Also, the ".INC" and ".LIB" commands which specify the path to reference the other two programs should be modified to reflect your disk directory structure.

ABT Short-form Datasheets

Quad buffer (3-State)

74ABT125

FEATURES

- Quad bus interface
- 3-State buffers
- Live insertion/extraction permitted
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Power-up 3-State

DESCRIPTION

The 74ABT125 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT125 device is a quad buffer that is ideal for driving bus lines. The device features four Output Enables ($\overline{OE}0$, $\overline{OE}1$, $\overline{OE}2$, $\overline{OE}3$), each controlling one of the 3-State outputs.

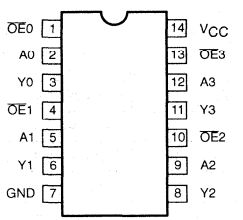
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	50	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
14-pin plastic DIP	–40°C to +85°C	74ABT125N	0405B
14-pin plastic SO	–40°C to +85°C	74ABT125D	0175D

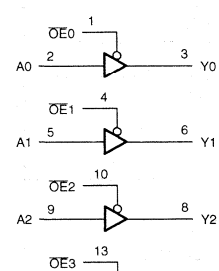
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 5, 9, 12	A0 – A3	Data inputs
3, 6, 8, 11	Y0 – Y3	Data outputs
1, 4, 10, 13	$\overline{OE}0$ – $\overline{OE}3$	Output enable inputs (active-Low)
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL



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FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}n$	An	Yn
L	L	L
L	H	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

Quad buffer (3-State) 74ABT126

FEATURES

- Quad bus interface
- 3-State buffers
- Live insertion/extraction permitted
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Power-up 3-State

DESCRIPTION

The 74ABT126 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT126 device is a quad buffer that is ideal for driving bus lines. The device features four Output Enables (OE0, OE1, OE2, OE3), each controlling one of the 3-State outputs.

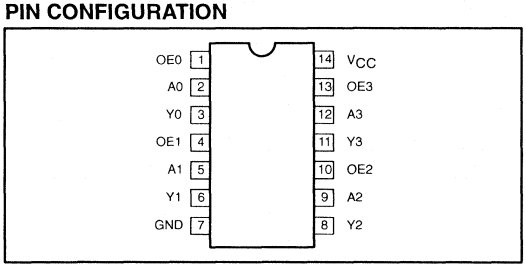
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	50	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
14-pin plastic DIP	–40°C to +85°C	74ABT126N	SOT27-1
14-pin plastic SO	–40°C to +85°C	74ABT126D	SOT108-1
14-pin plastic SSOP Type II	–40°C to +85°C	74ABT126DB	SOT337-1
14-pin plastic TSSOP Type I	–40°C to +85°C	74ABT126PW	SOT402-1

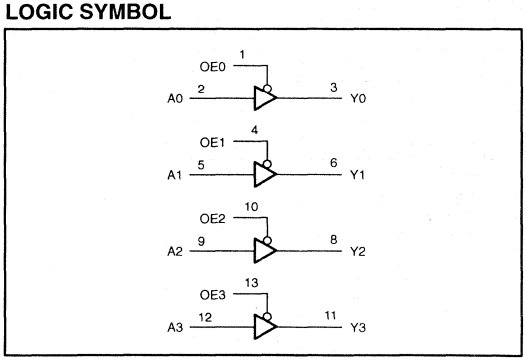
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 5, 9, 12	A0 – A3	Data inputs
3, 6, 8, 11	Y0 – Y3	Data outputs
1, 4, 10, 13	OE0 – OE3	Output enable inputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS
OEn	An	Yn
H	L	L
H	H	H
L	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

Octal inverting buffer (3-State) 74ABT240

FEATURES

- Octal bus interface
- 3-State buffers
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT240 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT240 device is an octal inverting buffer that is ideal for driving bus lines. The device features two Output Enables ($1\overline{OE}$, $2\overline{OE}$), each controlling four of the 3-State outputs.

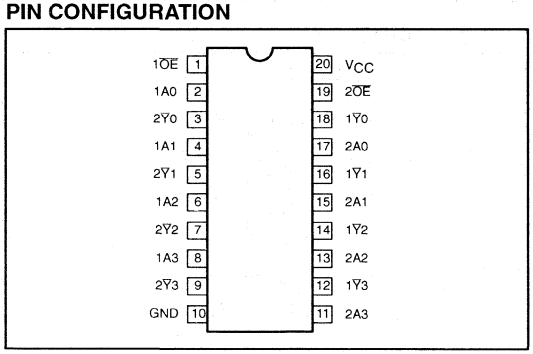
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	C_L = 50pF; V_{CC} = 5V	3.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	50	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin plastic DIP	–40°C to +85°C	74ABT240N	0408B
20-pin plastic SOL	–40°C to +85°C	74ABT240D	0172D
20-pin SSOP Type II	–40°C to +85°C	74ABT240DB	1640A

PIN CONFIGURATION



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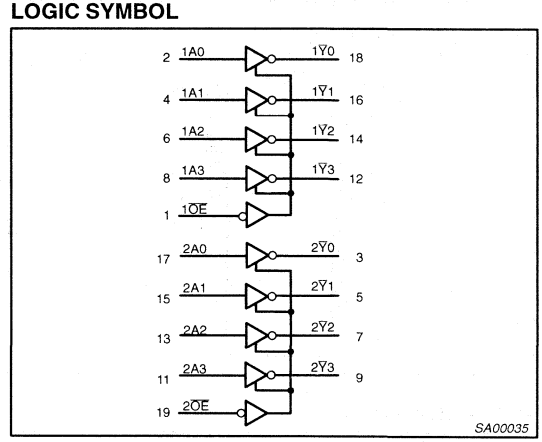


PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
11, 13, 15, 17	2A0 – 2A3	Data inputs
18, 16, 14, 12	1$\overline{Y}$0 – 1$\overline{Y}$3	Data outputs
9, 7, 5, 3	2$\overline{Y}$0 – 2$\overline{Y}$3	Data outputs
1, 19	1$\overline{OE}$, 2$\overline{OE}$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	
1$\overline{OE}$	1An	2$\overline{OE}$	2An	1$\overline{Y}$n	2$\overline{Y}$n
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

Octal inverting buffer with 30Ω series termination resistors (3-State)

74ABT240-1

FEATURES

- Octal bus interface
- 3-State buffers
- Live insertion/extraction permitted
- Outputs include series resistance of 30W, making external termination resistors unnecessary
- Output capability: +12mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State

DESCRIPTION

The 74ABT240-1 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT240-1 device is an octal inverting buffer that is ideal for driving bus lines. The device features two Output Enables ($1\overline{OE}$, $2\overline{OE}$), each controlling four of the 3-State outputs.

The 74ABT240-1 is designed with 30W series resistance in both the High and Low states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters.

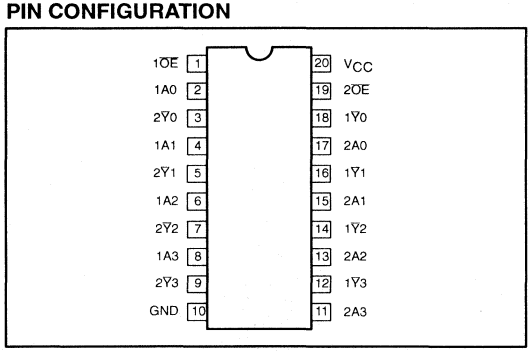
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Y}$n	C_L = 50pF; V_{CC} = 5V	3.5	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	50	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin plastic DIP	–40°C to +85°C	74ABT240-1N	0408B
20-pin plastic SOL	–40°C to +85°C	74ABT240-1D	0172D
20-pin SSOP Type II	–40°C to +85°C	74ABT240-1DB	1640A

PIN CONFIGURATION



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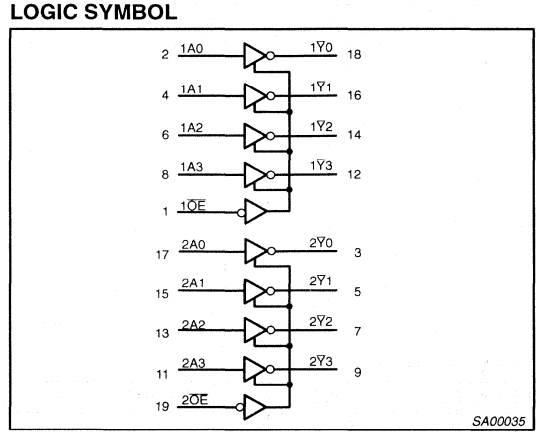


PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
11, 13, 15, 17	2A0 – 2A3	Data inputs
18, 16, 14, 12	$1\overline{Y}0$ – $1\overline{Y}3$	Data outputs
9, 7, 5, 3	$2\overline{Y}0$ – $2\overline{Y}3$	Data outputs
1, 19	$1\overline{OE}$, $2\overline{OE}$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	
$1\overline{OE}$	1An	$2\overline{OE}$	2An	$1\overline{Y}$n	$2\overline{Y}$n
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

Octal buffer/line driver (3-State) 74ABT241

FEATURES

- Octal bus interface
- 3-State buffers
- Power-up 3-State
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT241 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT241 device is an octal buffer that is ideal for driving bus lines. The device features two Output Enables ($1\overline{OE}$, 2OE), each controlling four of the 3-State outputs.

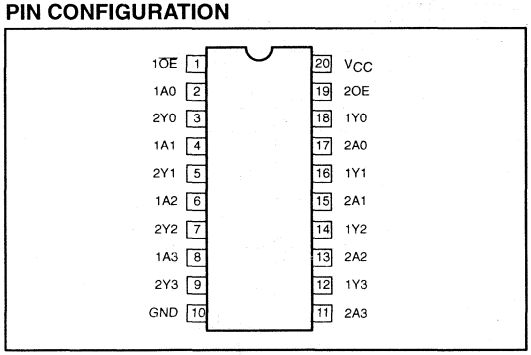
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	500	nA

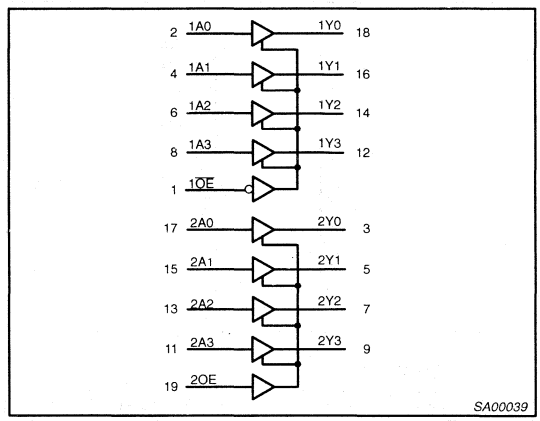
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin plastic DIP	–40°C to +85°C	74ABT241N	0408B
20-pin plastic SOL	–40°C to +85°C	74ABT241D	0173D
20-pin plastic SSOP Type II	–40°C to +85°C	74ABT241DB	1640A

PIN CONFIGURATION



LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
17, 15, 13, 11	2A0 – 2A3	Data inputs
18, 16, 14, 12	1Y0 – 1Y3	Data outputs
3, 5, 7, 9	2Y0 – 2Y3	Data outputs
1, 19	$1\overline{OE}$, 2OE	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	
$1\overline{OE}$	1An	2OE	2An	1Yn	2Yn
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

Octal buffer/line driver (3-State) 74ABT244

FEATURES

- Octal bus interface
- 3-State buffers
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State

DESCRIPTION

The 74ABT244 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT244 device is an octal buffer that is ideal for driving bus lines. The device features two Output Enables ($1\overline{OE}$, $2\overline{OE}$), each controlling four of the 3-State outputs.

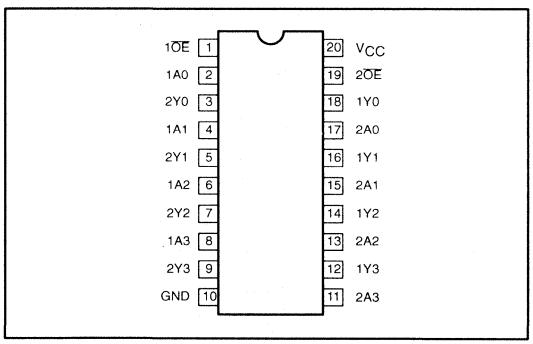
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	500	nA

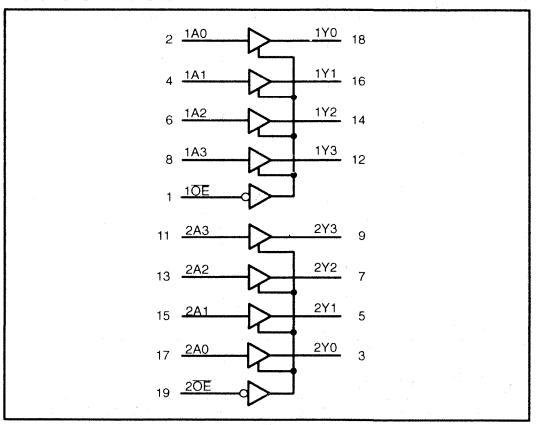
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin plastic DIP	–40°C to +85°C	74ABT244N	0408B
20-pin plastic SOL	–40°C to +85°C	74ABT244D	0172D
20-pin SSOP Type II	–40°C to +85°C	74ABT244DB	1640A

PIN CONFIGURATION



LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
11, 13, 15, 17	2A0 – 2A3	Data inputs
18, 16, 14, 12	1Y0 – 1Y3	Data outputs
9, 7, 5, 3	2Y0 – 2Y3	Data outputs
1, 19	$1\overline{OE}$, $2\overline{OE}$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	
$1\overline{OE}$	1An	$2\overline{OE}$	2An	1Yn	2Yn
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

Octal buffer/line driver with 30Ω series termination resistors (3-State)

74ABT244-1

FEATURES

- Octal bus interface
- 3-State buffers
- Live insertion/extraction permitted
- Outputs include series resistance of 30Ω, making external termination resistors unnecessary
- Output capability: +5mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State

DESCRIPTION

The 74ABT244-1 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT244-1 device is an octal buffer that is ideal for driving bus lines. The device features two Output Enables ($1\overline{OE}$, $2\overline{OE}$), each controlling four of the 3-State outputs.

The 74ABT244-1 is designed with 30Ω series resistance in both the High and Low states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters.

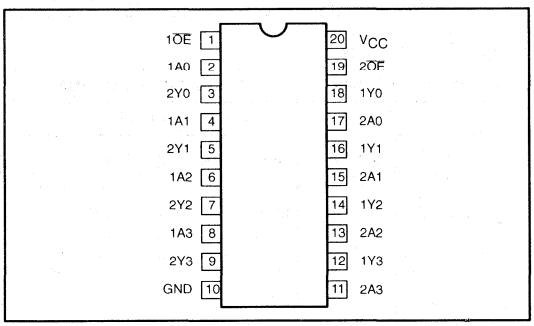
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 5V	3.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	500	nA

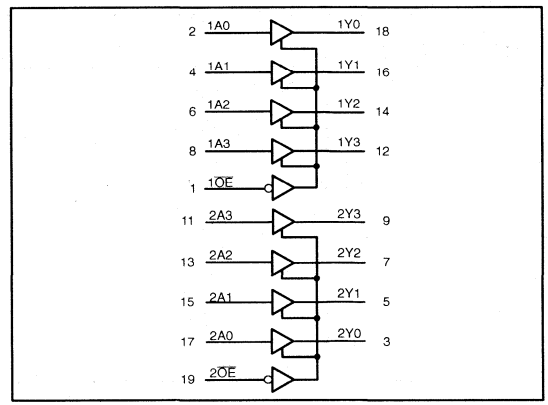
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin plastic DIP	–40°C to +85°C	74ABT244-1N	0408B
20-pin plastic SOL	–40°C to +85°C	74ABT244-1D	0172D
20-pin SSOP Type II	–40°C to +85°C	74ABT244-1DB	1640A

PIN CONFIGURATION



LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
11, 13, 15, 17	2A0 – 2A3	Data inputs
18, 16, 14, 12	1Y0 – 1Y3	Data outputs
9, 7, 5, 3	2Y0 – 2Y3	Data outputs
1, 19	$1\overline{OE}$, $2\overline{OE}$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	
$1\overline{OE}$	1An	$2\overline{OE}$	2An	1Yn	2Yn
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

Octal transceiver with direction pin (3-State) 74ABT245

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 833 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT245 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT245 device is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

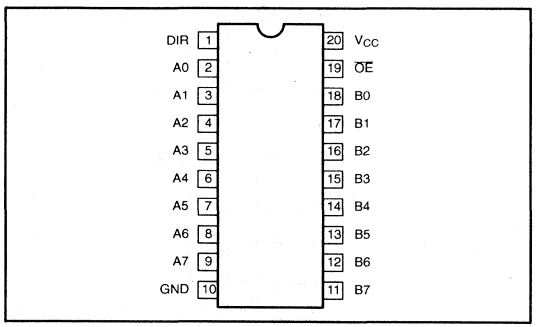
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	50	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin plastic DIP	–40°C to +85°C	74ABT245N	SOT146-1
20-pin plastic SOL	–40°C to +85°C	74ABT245D	SOT163-1
20-pin SSOP Type II	–40°C to +85°C	74ABT245DB	SOT339-1
20-pin SSOP Type I	–40°C to +85°C	74ABT245PW	SOT360-1

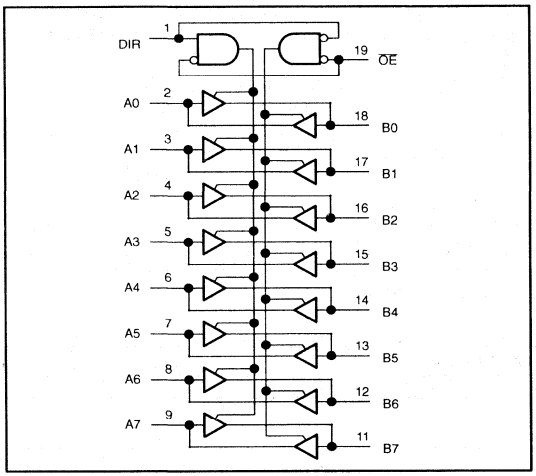
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	DIR	Direction control input
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs/outputs (A side)
18, 17, 16, 15, 14, 13, 12, 11	B0 – B7	Data inputs/outputs (B side)
19	$\overline{OE}$	Output enable input (active-Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	An	Bn
L	L	An = Bn	Inputs
L	H	Inputs	Bn = An
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

Octal transceiver with direction pin and 30Ω series termination resistors (3-State)

74ABT245-1

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Output capability: +12mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 833 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT245-1 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT245-1 device is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

The 74ABT245-1 is designed with 30Ω series resistance in both the High and Low states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters.

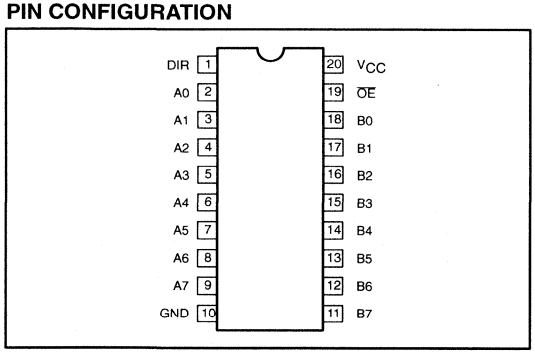
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	3.9	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	50	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin plastic DIP	–40°C to +85°C	74ABT245-1N	0408B
20-pin plastic SOL	–40°C to +85°C	74ABT245-1D	0172D
20-pin SSOP Type II	–40°C to +85°C	74ABT245-1DB	1640B
20-pin TSSOP Type I	–40°C to +85°C	74ABT245-1PW	SOT360-1

PIN CONFIGURATION



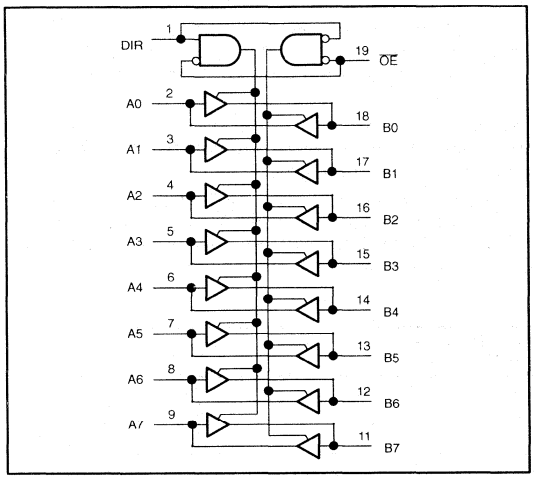
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	DIR	Direction control input
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs/outputs (A side)
18, 17, 16, 15, 14, 13, 12, 11	B0 – B7	Data inputs/outputs (B side)
19	$\overline{OE}$	Output enable input (active-Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

Octal transceiver with direction pin and 30Ω series termination resistors (3-State)

74ABT245-1

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	An	Bn
L	L	An = Bn	Inputs
L	H	Inputs	Bn = An
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

Octal D-type flip-flop 74ABT273A

FEATURES

- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Buffered asynchronous Master Reset
- Power-up reset
- See 74ABT377 for clock enable version
- See 74ABT373 for transparent latch version
- See 74ABT374 for 3-State version
- ESD protection exceeds 2000 V per Mil Std 833 Method 3015 and 200 V per machine model.

DESCRIPTION

The 74ABT273A has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced Low independent of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the CP and $\overline{MR}$ are common elements.

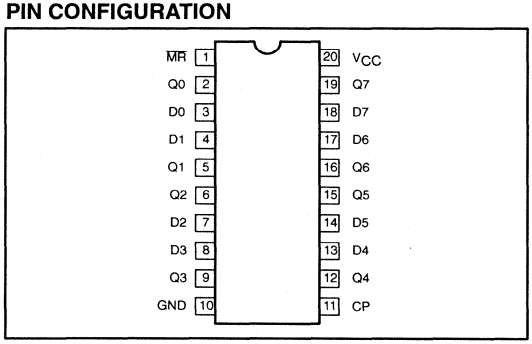
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 5V	3.0 3.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	pF
I_{CCH}	Total supply current	Outputs High; V_{CC} =5.5V	150	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin plastic DIP	-40°C to +85°C	74ABT273AN	SOT146-1
20-pin plastic SOL	-40°C to +85°C	74ABT273AD	SOT163-1
20-pin plastic SSOP Type II	-40°C to +85°C	74ABT273ADB	SOT339-1
20-pin plastic TSSOP Type I	-40°C to +85°C	74ABT273APW	SOT360-1

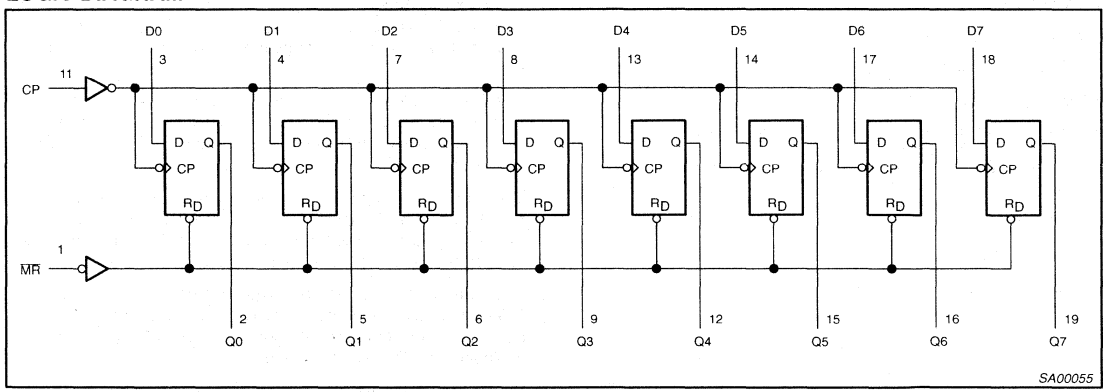
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
11	CP	Clock pulse input (active rising edge)
3, 4, 7, 8, 13, 14, 17, 18	D0 - D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	Q0 - Q7	Data outputs
1	$\overline{MR}$	Master Reset input (active-Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{MR}$	CP	Dn	Q0 - Q7	
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

Octal transparent latch (3-State) 74ABT373A

FEATURES

- 8-bit transparent latch
- 3-State output buffers
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Power-up reset
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT373A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT373A device is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

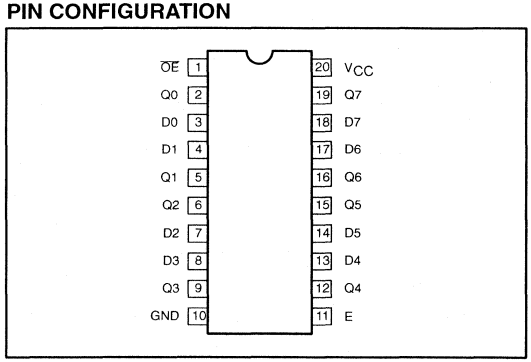
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	C_L = 50pF; V_{CC} = 5V	3.2 3.6	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	100	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin plastic DIP	–40°C to +85°C	74ABT373AN	SOT146-1
20-pin plastic SOL	–40°C to +85°C	74ABT373AD	SOT163-1
20-pin plastic SSOP Type II	–40°C to +85°C	74ABT373ADB	SOT339-1
20-pin plastic TSSOP Type I	–40°C to +85°C	74ABT373APW	SOT360-1

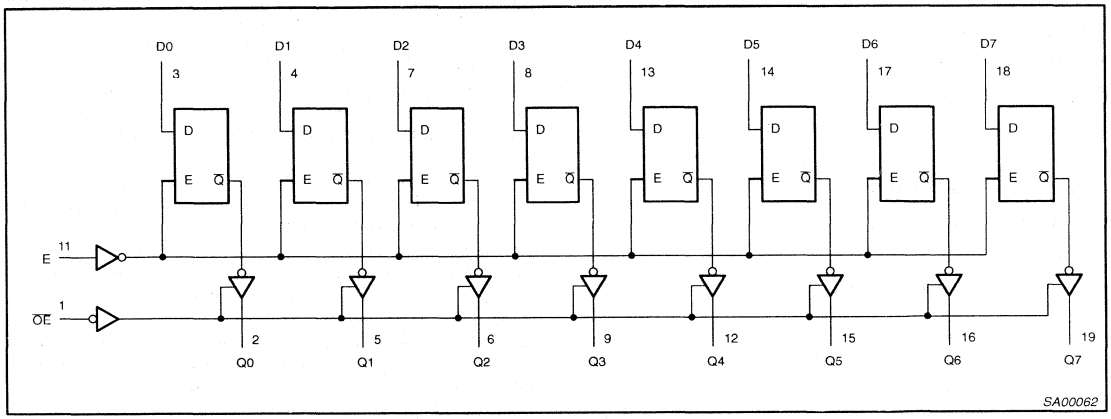
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
3, 4, 7, 8, 13, 14, 17, 18	D0-D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	Q0-Q7	Data outputs
11	E	Enable input (active-High)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	Dn		Q0 – Q7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	l h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

Octal D-type flip-flop; positive-edge trigger (3-State)

74ABT374A

FEATURES

- 8-bit positive edge triggered register
- 3-State output buffers
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Power-up reset
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT374A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT374A is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the clock operation.

When $\overline{OE}$ is Low, the stored data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

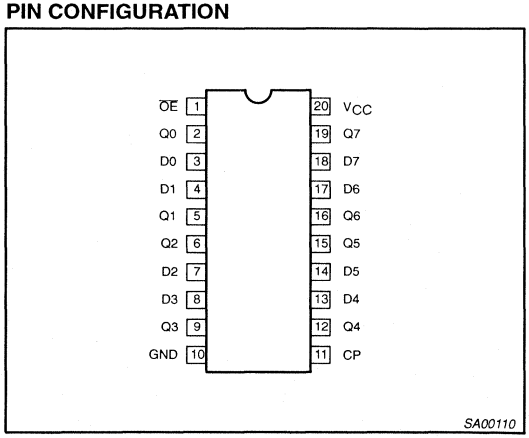
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 5V	3.4 3.8	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	110	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin plastic DIP	–40°C to +85°C	74ABT374AN	SOT146-1
20-pin plastic SOL	–40°C to +85°C	74ABT374AD	SOT163-1
20-pin plastic SSOP Type II	–40°C to +85°C	74ABT374ADB	SOT339-1
20-pin plastic TSSOP Type I	–40°C to +85°C	74ABT374APW	SOT360-1

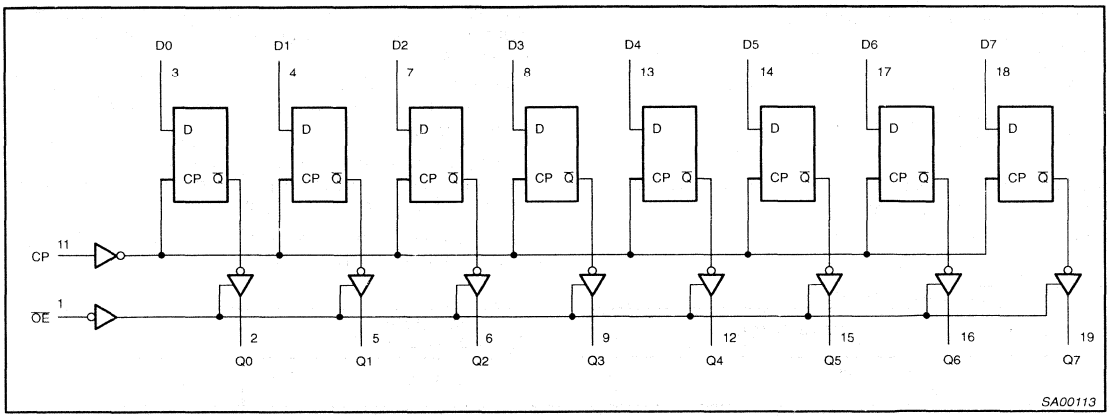
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
3, 4, 7, 8, 13, 14, 17, 18	D0-D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	Q0-Q7	Data outputs
11	CP	Clock pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn		Q0 – Q7	
L	↑	l	L	L	Latch and read register
L	↑	h	H	H	
L	↕	X	NC	NC	Hold
H	↕	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = not a Low-to-High clock transition

Octal D-type flip-flop with enable | 74ABT377

FEATURES

- Ideal for addressable register applications
- 8-bit positive edge-triggered register
- Enable for address and data synchronization applications
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Power-up reset

DESCRIPTION

The 74ABT377 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT377 has 8 edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered clock (CP) input loads all flip-flops simultaneously when the Enable ($\overline{E}$) input is Low.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The $\overline{E}$ input must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

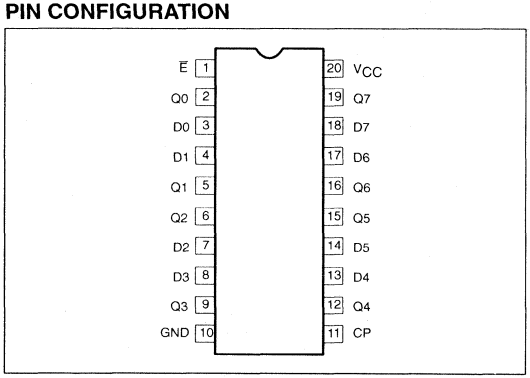
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 5V	5.3	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
I_{CCH}	Total current supply	Outputs High; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20–pin plastic DIP	-40°C to +85°C	74ABT377N	0408B
20–pin plastic SOL	-40°C to +85°C	74ABT377D	0172D
20–pin plastic SSOP Type II	-40°C to +85°C	74ABT377DB	1640A

PIN CONFIGURATION

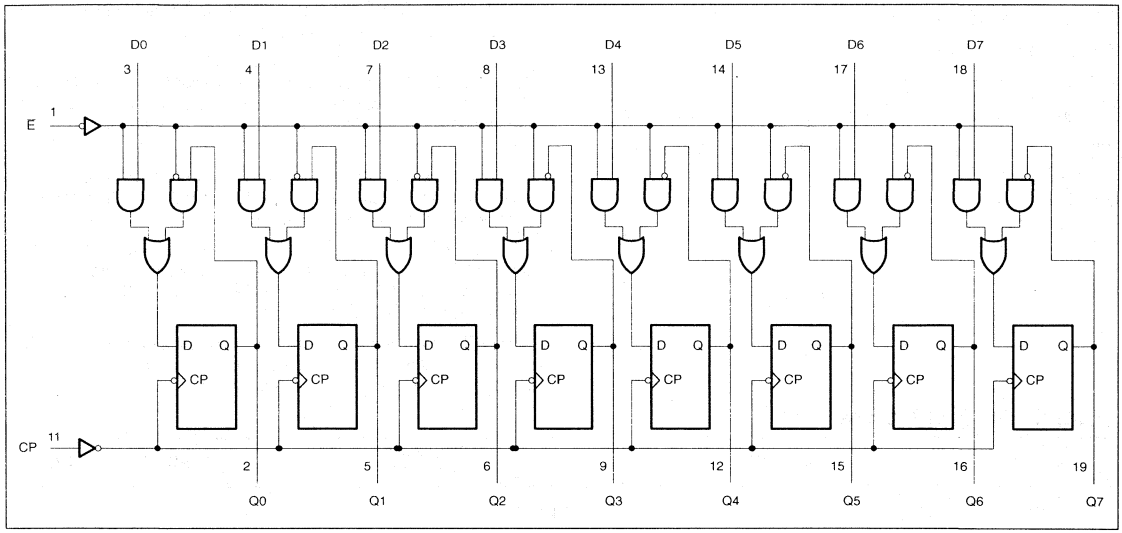


PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{E}$	Enable input (active–Low)
3, 4, 7, 8, 13, 14, 17, 18	D0-D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	Q0-Q7	Data outputs
11	CP	Clock Pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

Octal D-type flip-flop with enable 74ABT377

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{E}$	CP	Dn	Qn	
l	↑	h	H	Load "1"
l	↑	l	L	Load "0"
h H	↑ X	X X	no change no change	Hold (do nothing)

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

Octal D-type flip-flop, inverting (3-State) 74ABT534

FEATURES

- 8-bit positive edge triggered register
- 3-State output buffers
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State

DESCRIPTION

The 74ABT534 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT534 is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip–flop's output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the clock operation.

When $\overline{OE}$ is Low, the stored data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High–impedance "OFF" state, which means they will neither drive nor load the bus.

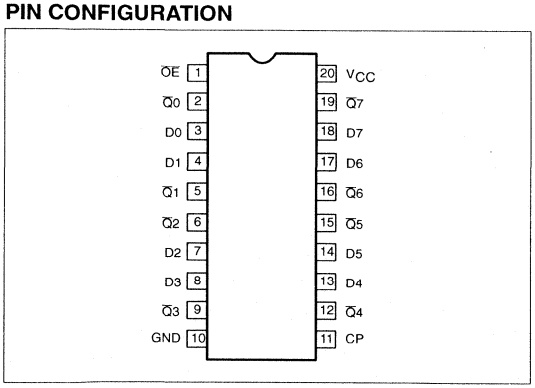
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}n$	C_L = 50pF; V_{CC} = 5V	6.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20–pin plastic DIP	–40°C to +85°C	74ABT534N	0408B
20–pin plastic SOL	–40°C to +85°C	74ABT534D	0172D
20–pin SSOP Type II	–40°C to +85°C	74ABT534DB	1640A

PIN CONFIGURATION

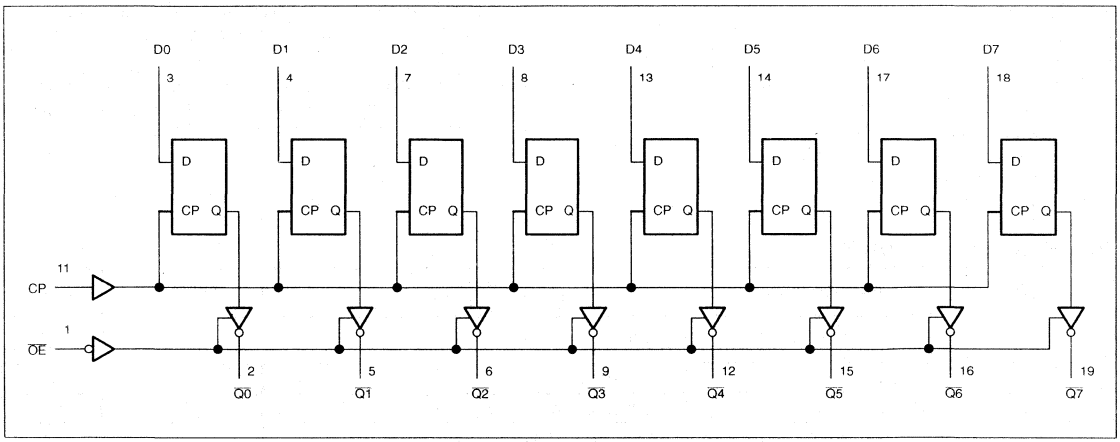


PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
3, 4, 7, 8, 13, 14, 17, 18	D0-D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	$\overline{Q}0$-$\overline{Q}7$	Inverting 3-State outputs
11	CP	Clock pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

Octal D-type flip-flop, inverting (3-State) 74ABT534

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn	REGISTER	$\overline{Q0} - \overline{Q7}$	
L L	↑ ↑	l h	L H	H L	Latch and read register
L	↕	X	NC	NC	Hold
H H	↕ ↑	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = not a Low-to-High clock transition

Octal buffer, inverting (3-State) 74ABT540

FEATURES

- Octal bus interface
- 3-State buffers
- Live insertion/extraction permitted
- Efficient pinout to facilitate PC board layout
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State

DESCRIPTION

The 74ABT540 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT540 device is an octal inverting buffer that is ideal for driving bus lines. The device features input and outputs on opposite sides of the package to facilitate printed circuit board layout.

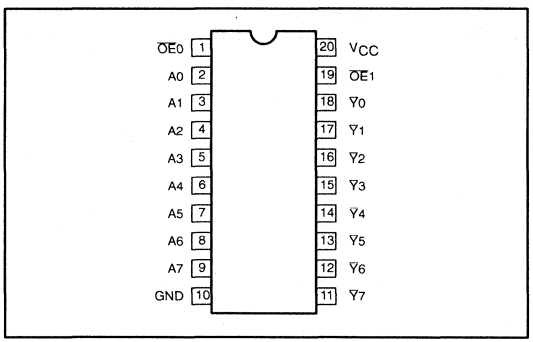
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Y}n$	C_L = 50pF; V_{CC} = 5V	3.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	50	µA

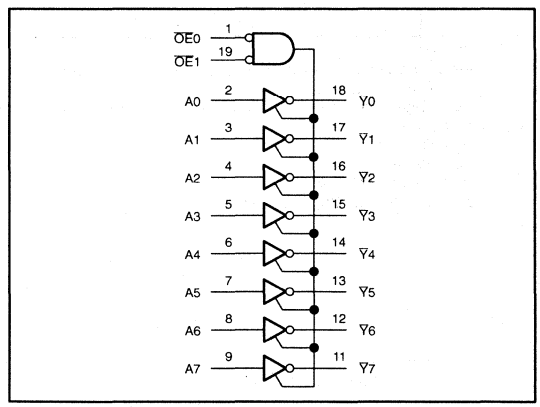
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin plastic DIP	–40°C to +85°C	74ABT540N	0408B
20-pin plastic SOL	–40°C to +85°C	74ABT540D	0172D
20-pin SSOP Type II	–40°C to +85°C	74ABT540DB	1640A

PIN CONFIGURATION



LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs
18, 17, 16, 15, 14, 13, 12, 11	$\overline{Y}0$ – $\overline{Y}7$	Data outputs
1, 19	$\overline{OE}0$, $\overline{OE}1$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{OE}0$	$\overline{OE}1$	An	$\overline{Y}n$
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

Octal buffer/line driver (3-State) 74ABT541

FEATURES

- Octal bus interface
- Functions similar to the 'ABT241
- Provides ideal interface and increases fan-out of MOS Microprocessors
- Efficient pinout to facilitate PC board layout
- 3-State buffer outputs sink 64mA and source 32mA
- Power-up 3-State
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT541 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT541 device is an octal buffer that is ideal for driving bus lines. The outputs are all capable of sinking 64mA and sourcing 32mA. The device features input and outputs on opposite sides of the package to facilitate printed circuit board layout.

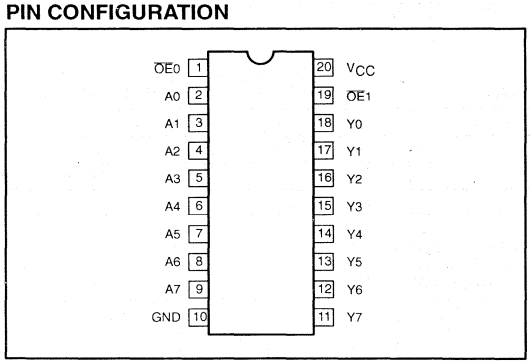
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	500	nA

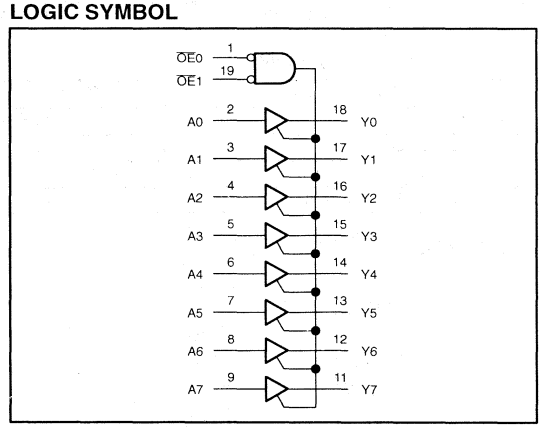
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMER
20–pin plastic DIP	–40°C to +85°C	74ABT541N	0408B
20–pin plastic SOL	–40°C to +85°C	74ABT541D	0172D
20–pin SSOP Type II	–40°C to +85°C	74ABT541DB	1640A

PIN CONFIGURATION



LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs
18, 17, 16, 15, 14, 13, 12, 11	Y0 – Y7	Data outputs
1, 19	$\overline{OE0}$, $\overline{OE1}$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{OE0}$	$\overline{OE1}$	An	Yn
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

Octal latched transceiver with dual enable (3-State)

74ABT543A

FEATURES

- Combines 74ABT245 and 74ABT373 type functions in one device
- 8-bit octal transceiver with D–type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Output capability: +64mA/–32mA
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT543A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT543A Octal Registered Transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of data transfer in either direction. The outputs are guaranteed to sink 64mA.

FUNCTIONAL DESCRIPTION

The 'ABT543A contains two sets of eight D–type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable ($\overline{EAB}$) input and the A-to-B Latch Enable ($\overline{LEAB}$) input are Low the A-to-B path is transparent. A subsequent Low-to-High transition of the $\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

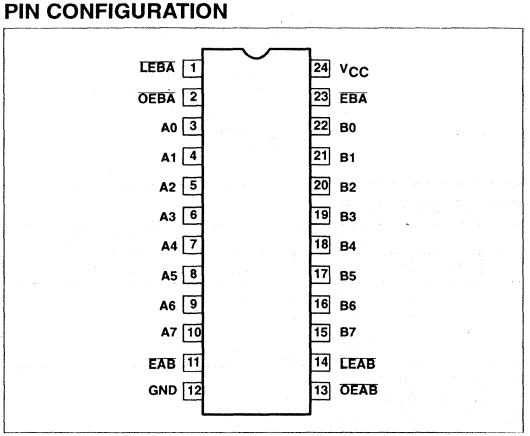
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	2.9 3.6	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	110	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24–pin plastic DIP	–40°C to +85°C	74ABT543AN	SOT222-1
24–pin plastic SOL	–40°C to +85°C	74ABT543AD	SOT137-1
24–pin plastic SSOP type II	–40°C to +85°C	74ABT543ADB	SOT340-1
24–pin plastic TSSOP type III	–40°C to +85°C	74ABT543APW	SOT355-1

PIN CONFIGURATION



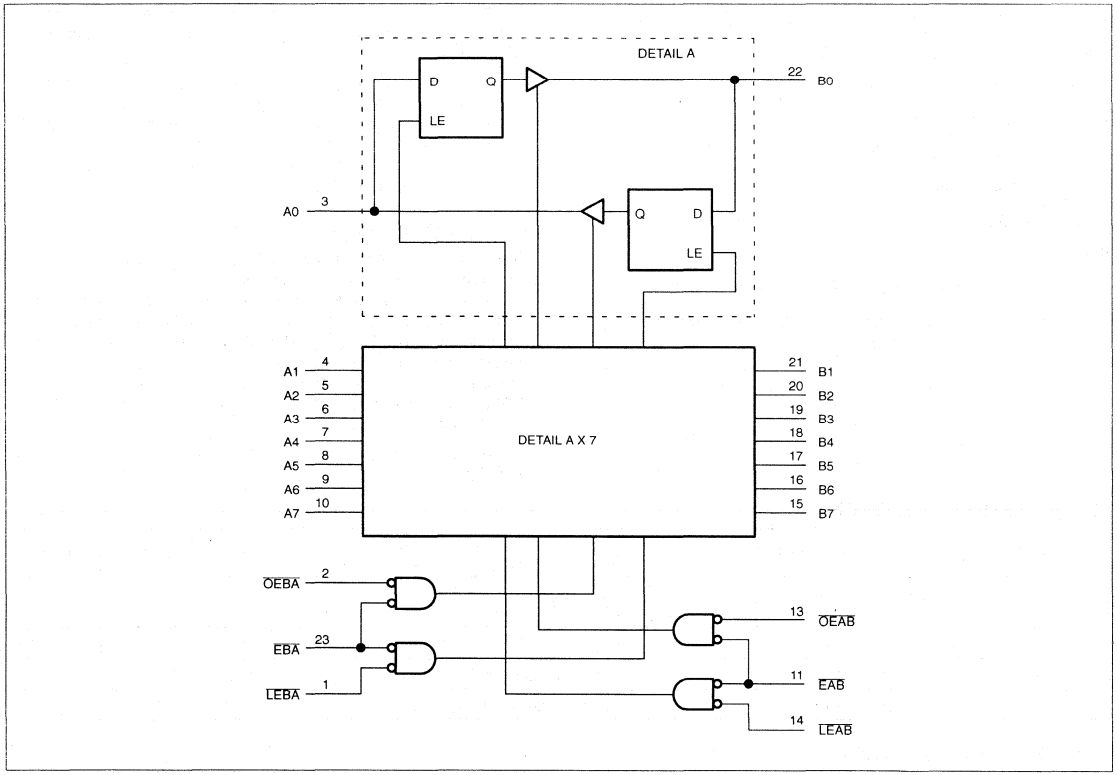
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
14, 1	$\overline{LEAB}$ / $\overline{LEBA}$	A to B / B to A Latch Enable input (active–Low)
11, 23	$\overline{EAB}$ / $\overline{EBA}$	A to B / B to A Enable input (active–Low)
13, 2	$\overline{OEAB}$ / $\overline{OEBA}$	A to B / B to A Output Enable input (active–Low)
3, 4, 5, 6, 7, 8, 9, 10	A0 – A7	Port A, 3–State outputs
22, 21, 20, 19, 18, 17, 16, 15	B0 – B7	Port B, 3–State outputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

Octal latched transceiver with dual enable (3-State)

74ABT543A

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OE}XX$	$\overline{E}XX$	$\overline{LE}XX$	An or Bn	Bn or An	
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	H L	Latch + Display
L L	L L	L L	H L	H L	Transparent
L	L	H	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High transition of $\overline{LE}XX$ or $\overline{E}XX$ (XX = AB or BA)
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High transition of $\overline{LE}XX$ or $\overline{E}XX$ (XX = AB or BA)
X = Don't care
↑ = Low-to-High transition of $\overline{LE}XX$ or $\overline{E}XX$ (XX = AB or BA)
NC= No change
Z = High impedance or "off" state

Octal latched transceiver with dual enable, inverting (3-State)

74ABT544

FEATURES

- Combines 74ABT245 and 74ABT373 type functions in one device
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Output capability: +64mA/–32mA
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT544 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT544 Octal Registered Transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of data transfer in either direction. The outputs are guaranteed to sink 64mA.

FUNCTIONAL DESCRIPTION

The 'ABT544 contains two sets of eight D–type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable ($\overline{EAB}$) input and the A-to-B Latch Enable ($\overline{LEAB}$) input are Low the A-to-B path is transparent. A subsequent Low-to-High transition of the $\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both Low, the 3-State B output buffers are active and invert the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

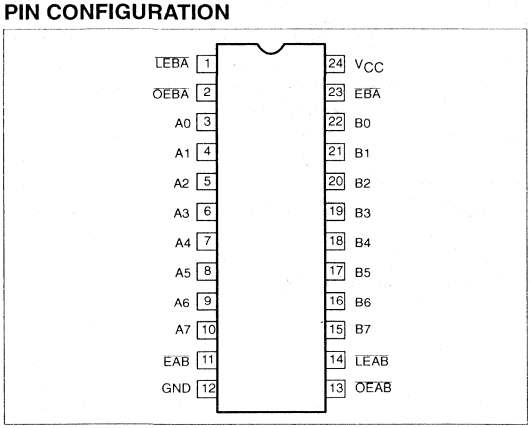
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay $\overline{An}$ to $\overline{Bn}$ or $\overline{Bn}$ to $\overline{An}$	C_L = 50pF; V_{CC} = 5V	3.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	110	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-pin plastic DIP	–40°C to +85°C	74ABT544N	0410D
24-pin plastic SOL	–40°C to +85°C	74ABT544D	0173D
24-pin plastic SSOP Type II	–40°C to +85°C	74ABT544DB	1641A

PIN CONFIGURATION



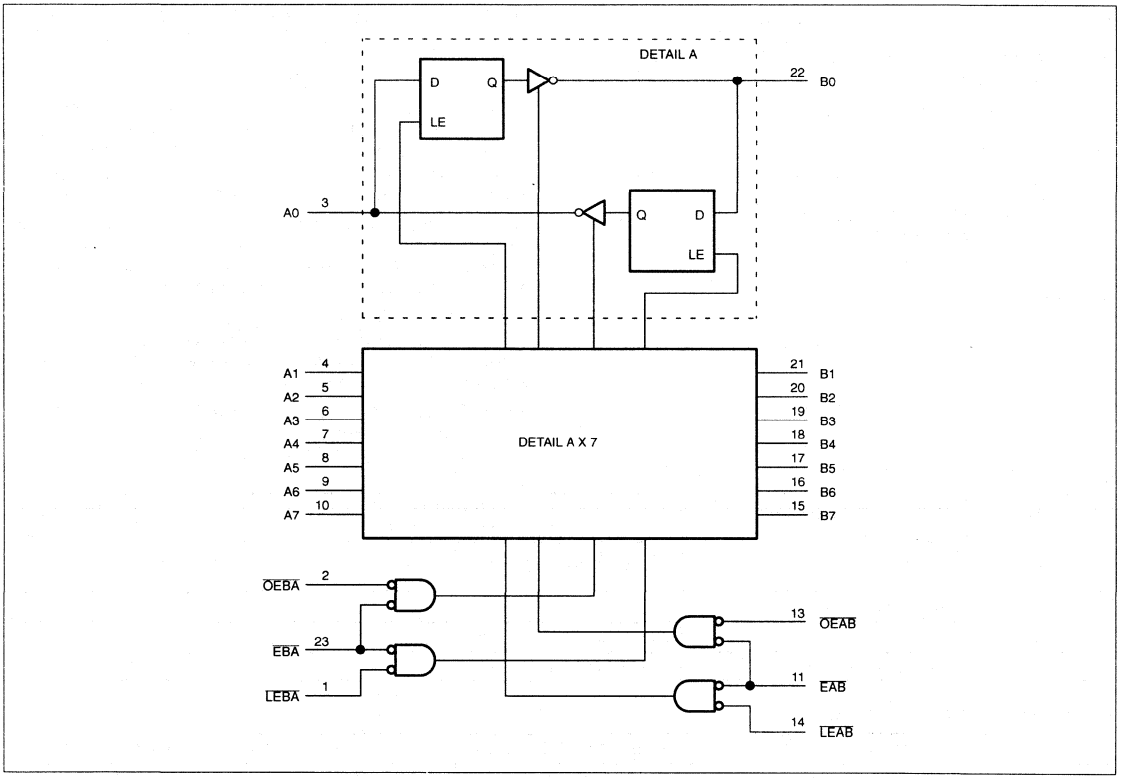
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
14, 1	$\overline{LEAB}$ / $\overline{LEBA}$	A to B / B to A Latch Enable input (active-Low)
11, 23	$\overline{EAB}$ / $\overline{EBA}$	A to B / B to A Enable input (active-Low)
13, 2	$\overline{OEAB}$ / $\overline{OEBA}$	A to B / B to A Output Enable input (active-Low)
3, 4, 5, 6, 7, 8, 9, 10	$\overline{A0}$ – $\overline{A7}$	Port A, 3-State outputs
22, 21, 20, 19, 18, 17, 16, 15	$\overline{B0}$ – $\overline{B7}$	Port B, 3-State outputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

Octal latched transceiver with dual enable, inverting (3-State)

74ABT544

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OE}Xx$	$\overline{E}Xx$	$\overline{LE}Xx$	An or Bn	An or Bn	
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	L H	Latch + Display
L L	L L	L L	H L	L H	Transparent
L	L	H	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
NC= No change
Z = High impedance or "off" state

Octal D-type transparent latch (3-State) 74ABT573

FEATURES

- 74ABT573 is broadside pinout version of 74ABT373
- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- 3-State output buffers
- Common output enable
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Power-up reset

DESCRIPTION

The 74ABT573 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT573 device is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates. The 74ABT573 is functionally identical to the 74ABT373 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

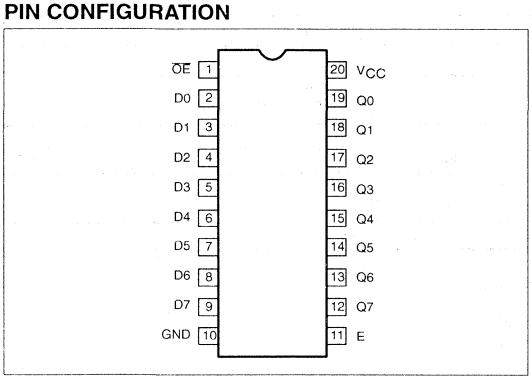
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	C_L = 50pF; V_{CC} = 5V	4.2	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin plastic DIP	–40°C to +85°C	74ABT573N	0408B
20-pin plastic SOL	–40°C to +85°C	74ABT573D	0172D
20-pin plastic SSOP Type II	–40°C to +85°C	74ABT573D	1640A

PIN CONFIGURATION

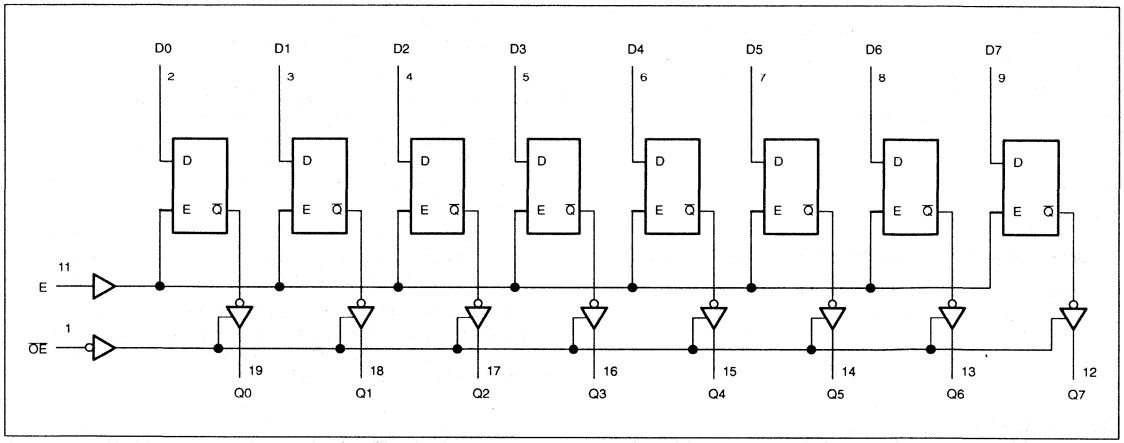


PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9	D0-D7	Data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0-Q7	Data outputs
11	E	Enable input (active-High)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

Octal D-type transparent latch (3-State) 74ABT573

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	Dn	REGISTER	Q0 – Q7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	l h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

Octal D-type flip-flop (3-State) 74ABT574

FEATURES

- 74ABT574 is broadside pinout version of 74ABT374
- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- 3-State outputs for bus interfacing
- Power-up 3-State
- Power-up reset
- Common output enable
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Live insertion/extraction permitted.

DESCRIPTION

The 74ABT574 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT574 is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates. The state of each D input (one set-up time before the Low-to-High clock transition) is transferred to the corresponding flip-flop's Q output.

When $\overline{OE}$ is Low, the stored data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "off" state, which means they will neither drive nor load the bus.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the clock operation.

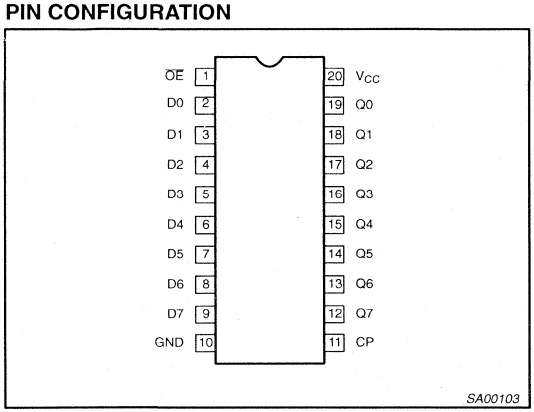
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 5V	4.8	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	115	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin plastic DIP	–40°C to +85°C	74ABT574N	SOT146-1
20–pin plastic SOL	–40°C to +85°C	74ABT574D	SOT163-1
20–pin plastic SSOP Type II	–40°C to +85°C	74ABT574DB	SOT339-1
20-pin plastic TSSOP Type I	–40°C to +85°C	74ABT574PW	SOT360-1

PIN CONFIGURATION

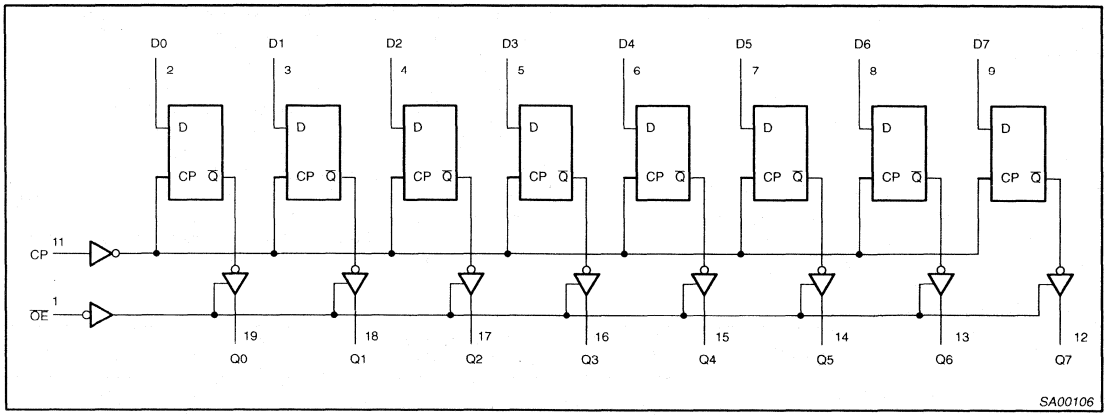


PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9	D0-D7	Data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0-Q7	Data outputs
11	CP	Clock pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

Octal D-type flip-flop (3-State) 74ABT574

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn		Q0 – Q7	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↕	X	NC	NC	Hold
H H	↕ ↑	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low–to–High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low–to–High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = not a Low-to-High clock transition

Octal transceiver with dual enable, inverting (3-State)

74ABT620

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Power-up 3-State
- Live insertion/extraction permitted
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT620 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT620 device is an octal transceiver featuring inverting 3-State bus compatible outputs in both send and receive directions. The 74ABT620 is designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs ($\overline{OEBA}$ and OEAB). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

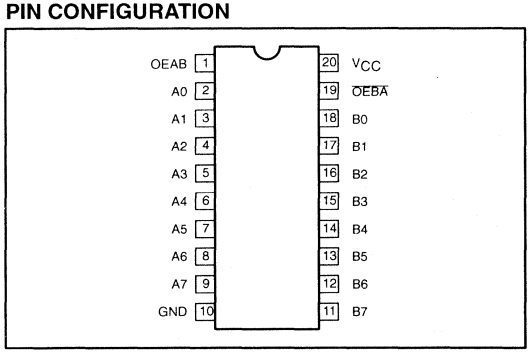
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	3.1	ns
C_{IN}	Input capacitance OEAB, $\overline{OEBA}$	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	50	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin plastic DIP	–40°C to +85°C	74ABT620N	0408B
20-pin plastic SOL	–40°C to +85°C	74ABT620D	0172D
20-pin plastic SSOP type II	–40°C to +85°C	74ABT620DB	1640A

PIN CONFIGURATION



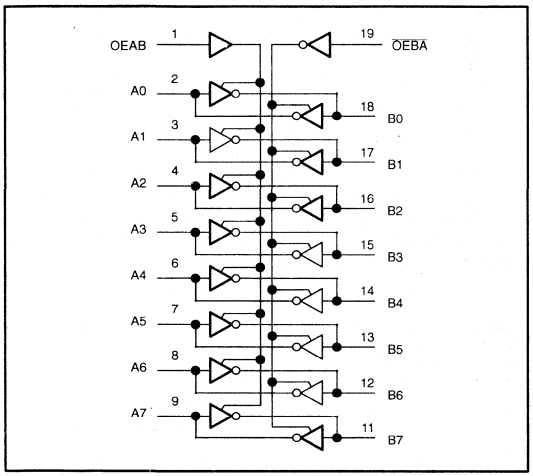
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	Output enable input, A side to B side (active-High)
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs/outputs (A side)
18, 17, 16, 15, 14, 13, 12, 11	B0 – B7	Data inputs/outputs (B side)
19	$\overline{OEBA}$	Output enable input, B side to A side (active-Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

Octal transceiver with dual enable, inverting (3-State)

74ABT620

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OEBA}$	OEAB	An	Bn
L	L	$\overline{Bn}$	Inputs
H	H	Inputs	$\overline{An}$
H	L	Z	Z
L	H	$\overline{Bn}$ or Inputs	Inputs $\overline{An}$

H = High voltage level
L = Low voltage level
Z = High impedance "off" state

Octal transceiver with dual enable, non-inverting (3-State)

74ABT623

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Power-up 3-State
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT623 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT623 device is an octal transceiver featuring non–inverting 3-State bus compatible outputs in both send and receive directions. The 74ABT623 is designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs ($\overline{OEBA}$ and OEAB). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

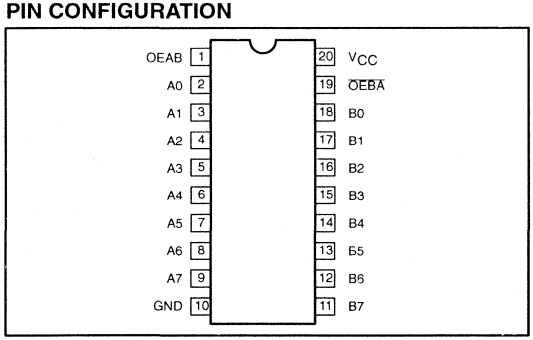
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance OEAB, $\overline{OEBA}$	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin plastic DIP	–40°C to +85°C	74ABT623N	0408B
20-pin plastic SOL	–40°C to +85°C	74ABT623D	0172D
20-pin plastic SSOP Type II	–40°C to +85°C	74ABT623D	1640A

PIN CONFIGURATION



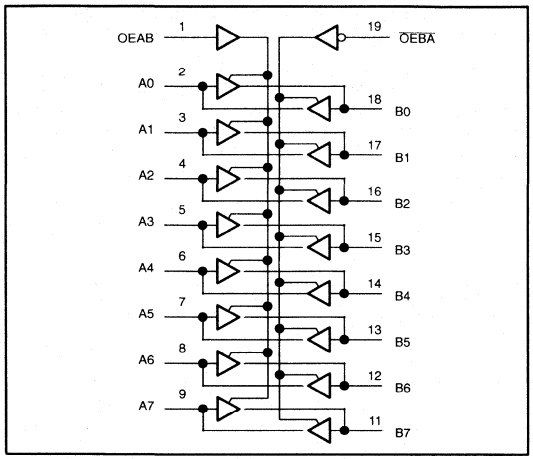
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	Output enable input, A side to B side (active-High)
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs/outputs (A side)
18, 17, 16, 15, 14, 13, 12, 11	B0 – B7	Data inputs/outputs (B side)
19	$\overline{OEBA}$	Output enable input, B side to A side (active-Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

Octal transceiver with dual enable, non-inverting (3-State)

74ABT623

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OEBA}$	OEAB	An	Bn
L	L	An = Bn	Inputs
H	H	Inputs	Bn = An
H	L	Z	Z
L	H	An = Bn	Bn = An

H = High voltage level
L = Low voltage level
Z = High impedance "off" state

Octal transceiver with direction pin, inverting (3-State)

74ABT640

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Power-up 3-State
- Live insertion/extraction permitted
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT640 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT640 device is an octal transceiver featuring inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

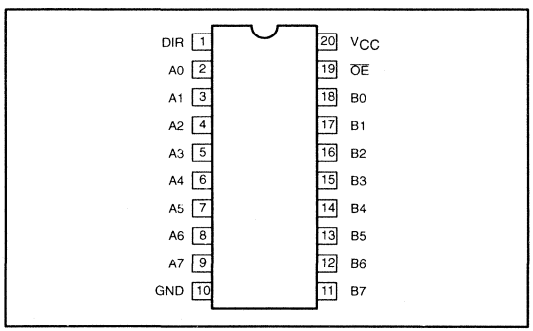
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	3.1	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	50	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin plastic DIP	–40°C to +85°C	74ABT640N	0408B
20-pin plastic SOL	–40°C to +85°C	74ABT640D	0172D
20-pin plastic SSOP Type II	–40°C to +85°C	74ABT640DB	1640A

PIN CONFIGURATION



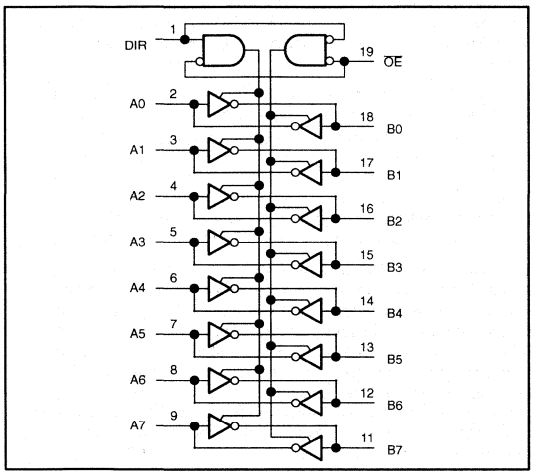
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	DIR	Direction control input
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs/outputs (A side)
18, 17, 16, 15, 14, 13, 12, 11	B0 – B7	Data inputs/outputs (B side)
19	$\overline{OE}$	Output enable input, B side to A side (active-Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

Octal transceiver with direction pin, inverting (3-State)

74ABT640

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	An	Bn
L	L	$\overline{Bn}$	Inputs
L	H	Inputs	$\overline{An}$
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

Octal bus transceiver/register (3-State) 74ABT646A

FEATURES

- Combines 74ABT245 and 74ABT374 type functions in one device
- Independent registers for A and B buses
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Multiplexed real-time and stored data
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT646A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT646A transceiver/register consists of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The Select (SAB, SBA) pins determine whether data is stored or transferred through the device in real-time. The DIR determines which bus will receive data when the $\overline{OE}$ is active (Low). In the isolation mode ($\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. The examples on the next page demonstrate the four fundamental bus management functions that can be performed with the 74ABT646A.

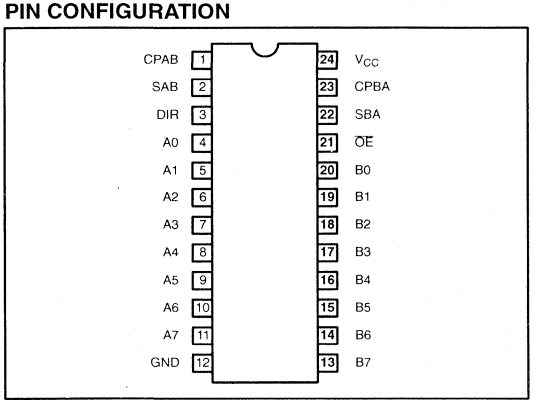
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	3.2 3.7	ns
C_{IN}	Input capacitance CP, S, $\overline{OE}$, DIR	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	110	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-pin plastic DIP	–40°C to +85°C	74ABT646AN	SOT222
24-pin plastic SOL	–40°C to +85°C	74ABT646AD	SOT137-1
24-pin plastic SSOP Type II	–40°C to +85°C	74ABT646ADB	SOT340-1
24-pin plastic TSSOP Type I	–40°C to +85°C	74ABT646APW	SOT355-1

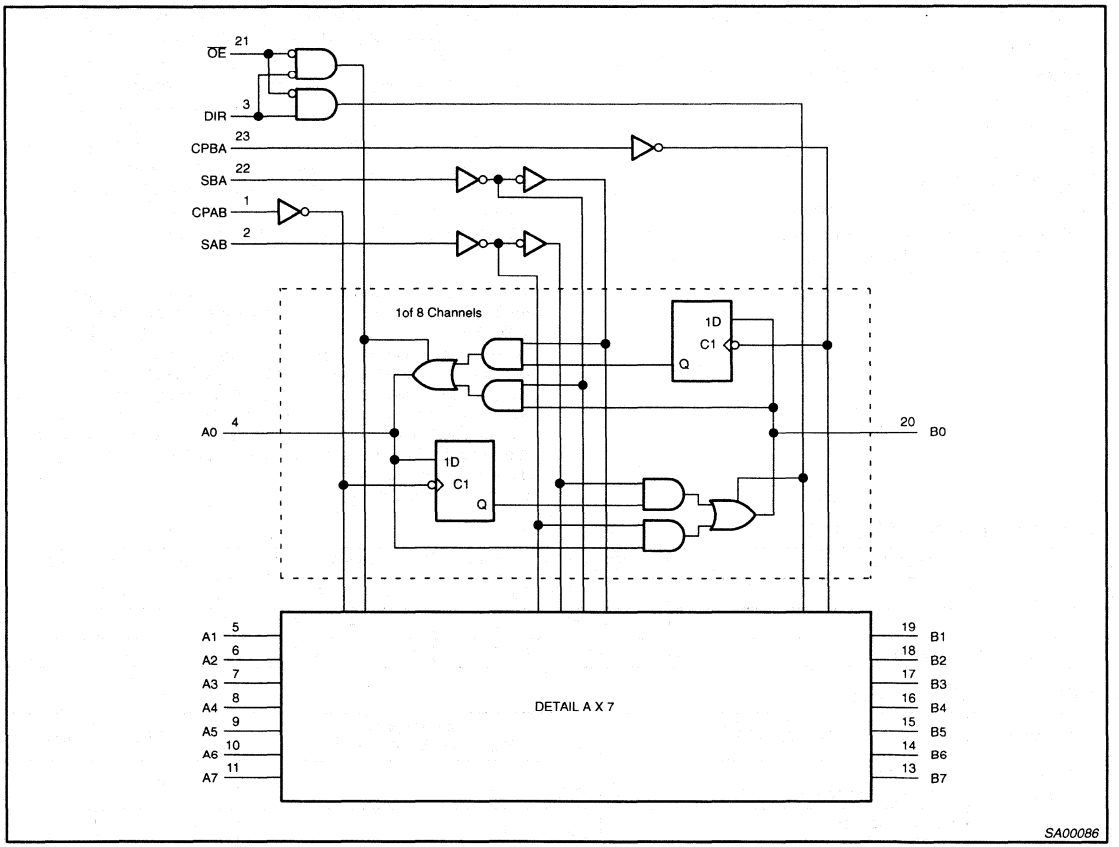
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 23	CPAB / CPBA	A to B clock input / B to A clock input
2, 22	SAB / SBA	A to B select input / B to A select input
3	DIR	Direction control input
4, 5, 6, 7, 8, 9, 10, 11	A0 – A7	Data inputs/outputs (A side)
20, 19, 18, 17, 16, 15, 14, 13	B0 – B7	Data inputs/outputs (B side)
21	$\overline{OE}$	Output enable input (active-Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	An	Bn	
X	X	↑	X	X	X	Input	Unspecified output*	Store A, B unspecified
X	X	X	↑	X	X	Unspecified output*	Input	Store B, A unspecified
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Stored A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the $\overline{OE}$ input. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

Octal bus transceiver/register, inverting (3-State) 74ABT648

FEATURES

- Combines 74ABT245 and 74ABT374 type functions in one device
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Output capability: +64mA/–32mA
- Power-up 3-state
- Power-up reset
- Live insertion/extraction permitted
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT648 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT648 transceiver/register consists of bus transceiver circuits with inverting 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The Select (SAB, SBA) pins determine whether data is stored or transferred through the device in real–time. The DIR determines which bus will receive data when the $\overline{OE}$ is active (Low). In the isolation mode ($\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register. Outputs from real-time, or stored registers will be inverted. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time. The examples on the next page demonstrate the four fundamental bus management functions that can be performed with the 74ABT648.

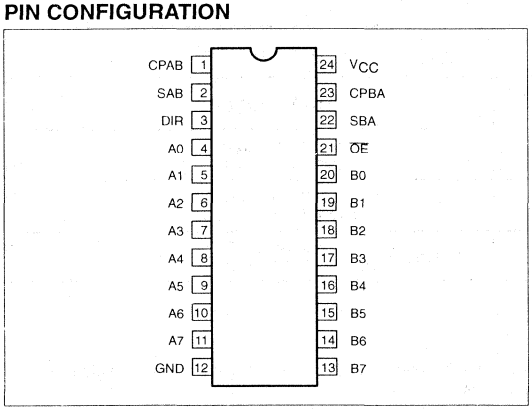
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-pin plastic DIP	–40°C to +85°C	74ABT648N	0410D
24-pin plastic SOL	–40°C to +85°C	74ABT648D	0173D
24-pin plastic SSOP Type II	–40°C to +85°C	74ABT648DB	1641A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	5.9	ns
C_{IN}	Input capacitance CP, S, $\overline{OE}$, DIR	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	110	µA

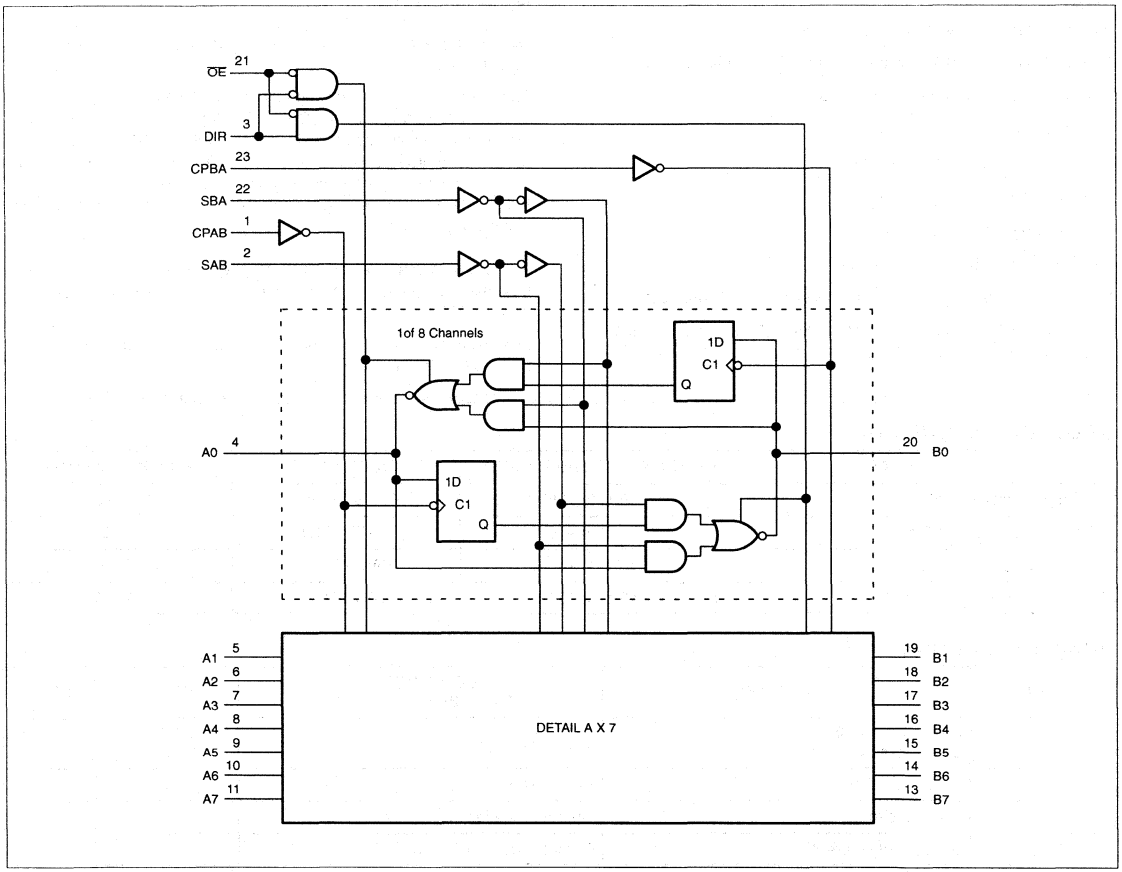
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 23	CPAB / CPBA	A to B clock input / B to A clock input
2, 22	SAB / SBA	A to B select input / B to A select input
3	DIR	Direction control input
4, 5, 6, 7, 8, 9, 10, 11	A0 – A7	Data inputs/outputs (A side)
20, 19, 18, 17, 16, 15, 14, 13	B0 – B7	Data inputs/outputs (B side)
21	$\overline{OE}$	Output enable input (active-Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	An	Bn	
X	X	↑	X	X	X	Input	Unspecified output*	Store A, B unspecified
X	X	X	↑	X	X	Unspecified output*	Input	Store B, A unspecified
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time $\overline{B}$ data to A bus Stored $\overline{B}$ data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real time $\overline{A}$ data to B bus Stored $\overline{A}$ data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the $\overline{OE}$ input. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

Octal transceiver/register, inverting (3-State) 74ABT651

FEATURES

- Independent registers for A and B buses
- The 74ABT651 is the inverting version of the 74ABT652
- Multiplexed real–time and stored data
- 3-State outputs
- Live insertion/extraction permitted.
- Power-up 3-State
- Power-up reset
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT651 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT651 transceiver/register consists of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{OEBA}$) and Select (SAB, SBA) pins are provided for bus management.

The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74ABT651.

The select pins determine whether data is stored or transferred through the device in real time.

The output enable pins determine the direction of the data flow.

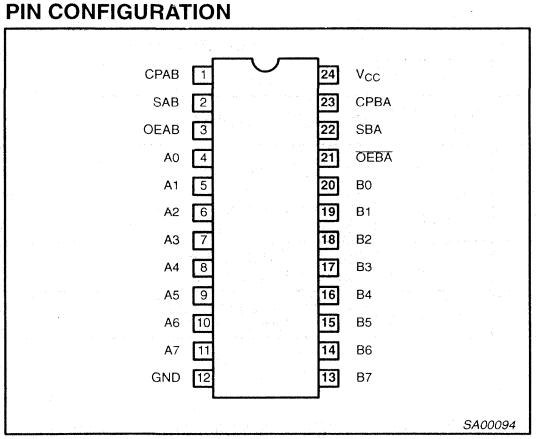
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-pin plastic DIP (300mil)	–40°C to +85°C	74ABT651N	SOT222
24-pin plastic SOL (300mil)	–40°C to +85°C	74ABT651D	SOT137-1
24-pin plastic SSOP Type II	–40°C to +85°C	74ABT651DB	SOT340-1
24-pin plastic TSSOP Type I	–40°C to +85°C	74ABT651PW	SOT355-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPBA to An or CPAB to Bn	C_L = 50pF; V_{CC} = 5V	3.8 4.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	110	μA

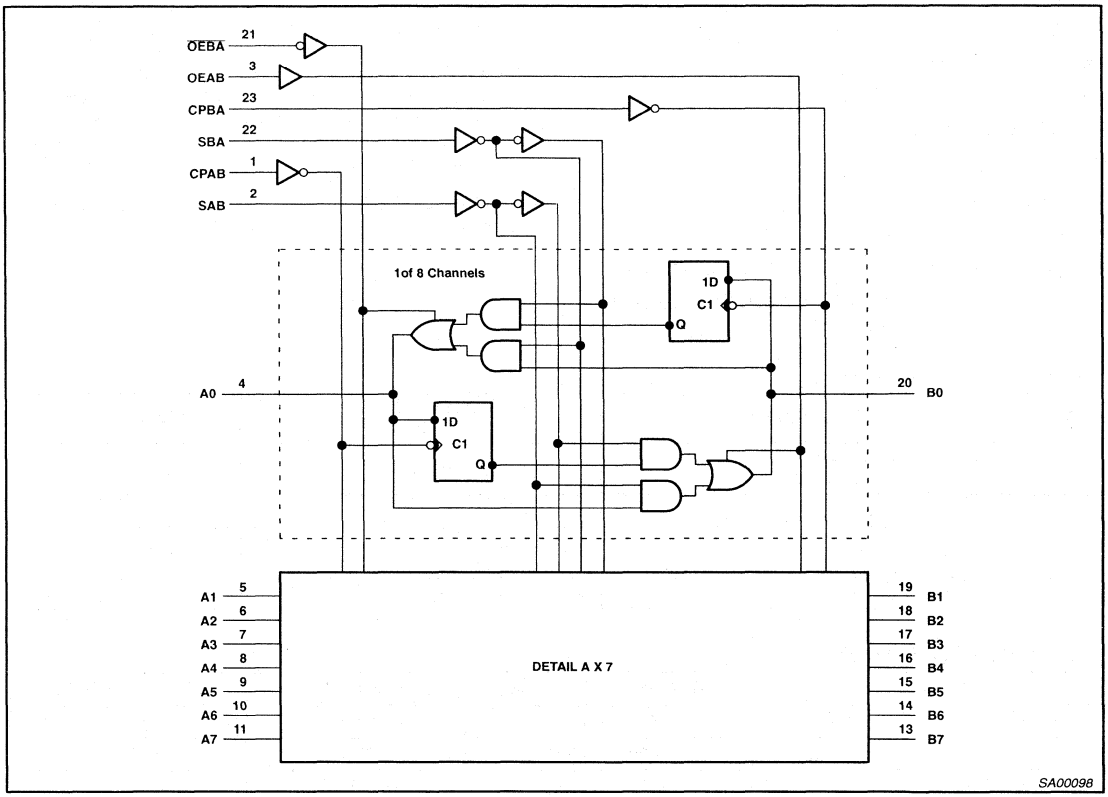
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 23	CPAB / CPBA	A to B clock input / B to A clock input
2, 22	SAB / SBA	A to B select input / B to A select input
3, 21	OEAB / $\overline{OEBA}$	A to B Output Enable input / B to A Output Enable input (active–Low)
4, 5, 6, 7, 8, 9, 10, 11	A0 – A7	Data inputs/outputs (A side)
20, 19, 18, 17, 16, 15, 14, 13	B0 – B7	Data inputs/outputs (B side)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	An	Bn	
L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B data
X H	H H	↑ ↑	H or L ↑	X **	X X	Input	Unspecified output*	Store A, Hold B Store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X **	Unspecified output*	Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time $\overline{B}$ data to A bus Stored $\overline{B}$ data to A bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real time $\overline{A}$ data to B bus Store $\overline{A}$ data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ data to B bus Stored $\overline{B}$ data to A bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the $\overline{OEBA}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
** If both Select controls (SAB and SBA) are Low, then clocks can occur simultaneously. If either Select control is High, the clocks must be staggered in order to load both registers.

Octal transceiver/register, non-inverting (3-State) 74ABT652A

FEATURES

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- 3-State outputs
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT652A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT652A transceiver/register consists of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{OEBA}$) and Select (SAB, SBA) pins are provided for bus management.

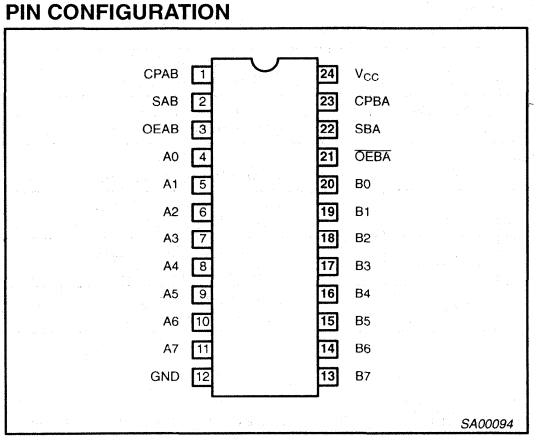
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPBA to An or CPAB to Bn	C_L = 50pF; V_{CC} = 5V	3.7 4.3	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	110	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-pin plastic DIP	–40°C to +85°C	74ABT652AN	SOT222
24-pin plastic SOL	–40°C to +85°C	74ABT652AD	SOT137-1
24-pin plastic SSOP Type II	–40°C to +85°C	74ABT652ADB	SOT340-1
24-pin plastic TSSOP Type I	–40°C to +85°C	74ABT652APW	SOT355-1

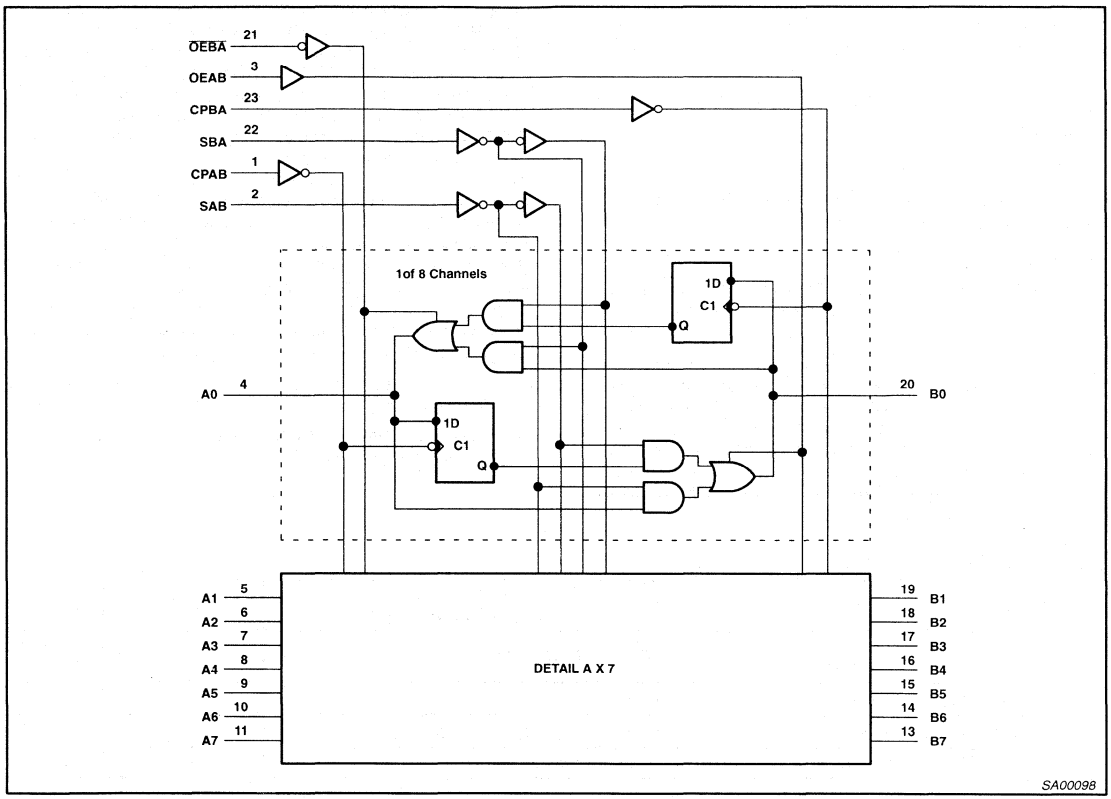
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 23	CPAB / CPBA	A to B clock input / B to A clock input
2, 22	SAB / SBA	A to B select input / B to A select input
3, 21	OEAB / $\overline{OEBA}$	A to B Output Enable input / B to A Output Enable input (active–Low)
4, 5, 6, 7, 8, 9, 10, 11	A0 – A7	Data inputs/outputs (A side)
20, 19, 18, 17, 16, 15, 14, 13	B0 – B7	Data inputs/outputs (B side)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	An	Bn	
L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B data
X H	H H	↑ ↑	H or L ↑	X **	X X	Input	Unspecified output*	Store A, Hold B Store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X **	Unspecified output*	Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Store A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus Stored B data to A bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the $\overline{OEBA}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
** If both Select controls (SAB and SBA) are Low, then clocks can occur simultaneously. If either Select control is High, the clocks must be staggered in order to load both registers.

Octal transceiver with parity generator/checker (3-State)

74ABT657

FEATURES

- Combinational functions in one package
- Low static and dynamic power dissipation with high speed and high output drive
- Output capability: +64mA/–32mA
- Power-up 3-State
- Latch–up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT657 high–performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT657 is an octal transceiver featuring non–inverting buffers with 3–State outputs and an 8-bit parity generator/checker, and is intended for bus–oriented applications. The buffers have a guaranteed current sinking capability of 64mA. The Transmit/Receive (T/$\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active-High) enables data from A ports to B ports; Receive (active-Low) enables data from B ports to A ports.

The Output Enable ($\overline{OE}$) input disables both the A and B ports by placing them in a high impedance condition when the $\overline{OE}$ input is High. The parity select (ODD/$\overline{EVEN}$) input gives the user the option of odd or even parity systems. The parity (PARITY) pin is an output from the generator/checker when transmitting from the port A to B (T/$\overline{R}$ = High) and an input when receiving from port B to A port (T/$\overline{R}$ = Low). When transmitting (T/$\overline{R}$ = High) the parity select (ODD/$\overline{EVEN}$) input is set, then the A port data is polled to determine the number of High bits. The parity (PARITY) output then goes to the logic state determined by the parity select (ODD/$\overline{EVEN}$) setting and by the number of High bits on port A. For example, if the parity select (ODD/$\overline{EVEN}$) is set Low (even parity), and the number of High bits on port A is odd, then the parity (PARITY) output will be High, transmitting even parity. If the number of High bits on port A is even, then the parity (PARITY) output will be Low, keeping even parity. When in receive mode (T/$\overline{R}$ = Low) the B port is polled to determine the number of High bits. If parity select (ODD/$\overline{EVEN}$) is Low (even parity) and the number of Highs on port B is:

(1) odd and the parity (PARITY) input is High, then $\overline{ERROR}$ will be High, signifying no error.

(2) even and the parity (PARITY) input is High, then $\overline{ERROR}$ will be asserted Low, indicating an error.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	3.3	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	500	nA

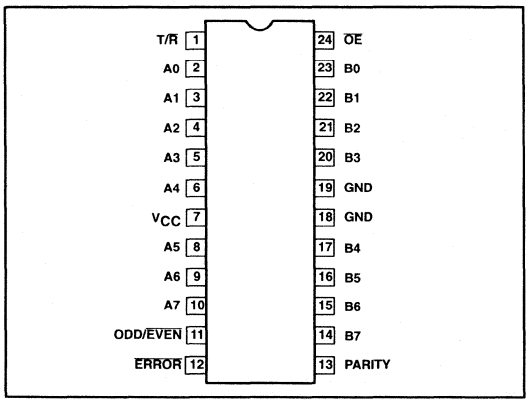
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24–pin plastic DIP	–40°C to +85°C	74ABT657N	0410D
24–pin plastic SOL	–40°C to +85°C	74ABT657D	0173D
24–pin plastic SSOP Type II	–40°C to +85°C	74ABT657DB	1641A

Octal transceiver with parity generator/checker (3-State)

74ABT657

PIN CONFIGURATION



PIN DESCRIPTION

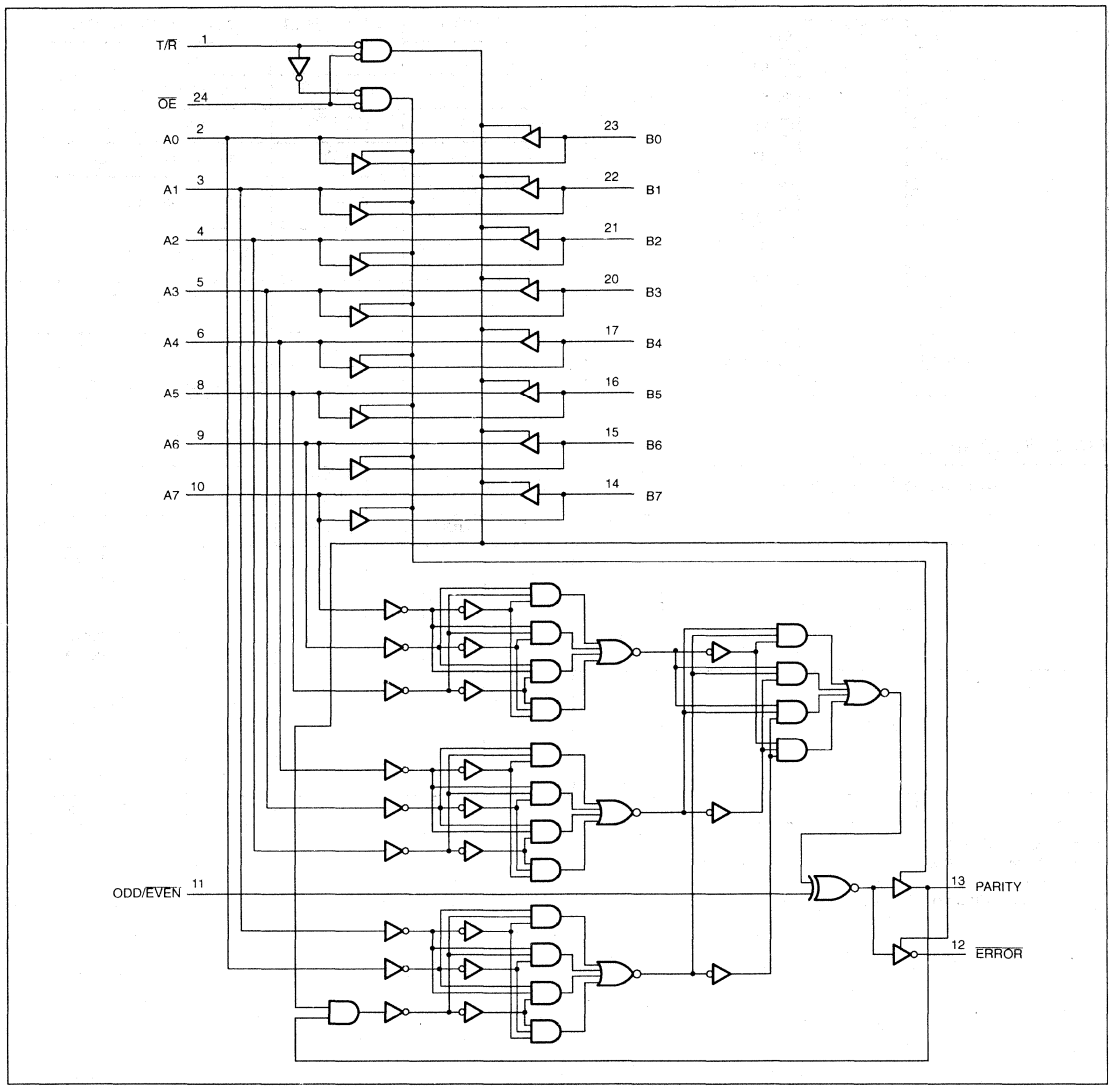
SYMBOL	PIN NUMBER	NAME AND FUNCTION
13	PARITY	Parity output
11	ODD/$\overline{\text{EVEN}}$	Parity select input
12	$\overline{\text{ERROR}}$	Error output
1	T/$\overline{\text{R}}$	Transmit/receive input
2, 3, 4, 5, 6, 8, 9, 10	A0 – A7	A port 3-State outputs
23, 22, 21, 20, 17, 16, 15, 14	B0 – B7	B port 3-State outputs
24	$\overline{\text{OE}}$	Output enable input (active-Low)
18, 19	GND	Ground (0V)
7	V_{CC}	Positive supply voltage

FUNCTION TABLE

NUMBER OF HIGH INPUTS	INPUTS			INPUT/ OUTPUT	OUTPUTS	
	$\overline{\text{OE}}$	T/$\overline{\text{R}}$	ODD/$\overline{\text{EVEN}}$	PARITY	$\overline{\text{ERROR}}$	OUTPUTS MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	3–State

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM



10-bit D-type flip-flop; positive-edge trigger (3-State)

74ABT821

FEATURES

- High speed parallel registers with positive edge–triggered D-type flip-flops
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Power-up Reset

DESCRIPTION

The 74ABT821 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT821 Bus interface Register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 'ABT821 is a buffered 10-bit wide version of the 'ABT374/'ABT534 functions.

The 'ABT821 is a 10-bit, edge triggered register coupled to ten 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active Low Output Enable ($\overline{OE}$) controls all ten 3-State buffers independent of the register operation. When $\overline{OE}$ is Low, the data in the register appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

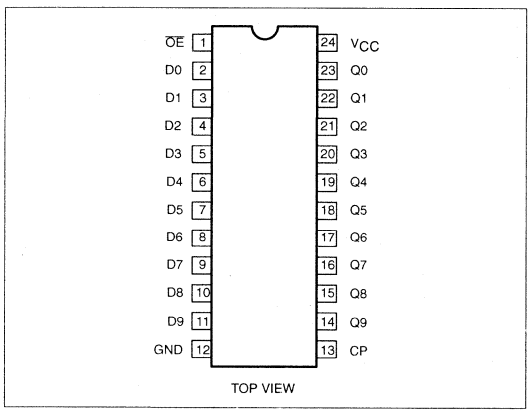
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 5V	4.6	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-pin plastic DIP	–40°C to +85°C	74ABT821N	0410D
24-pin plastic SOL	–40°C to +85°C	74ABT821D	0173D
24-pin plastic SSOP Type II	–40°C to +85°C	74ABT821DB	1641A

PIN CONFIGURATION



TOP VIEW

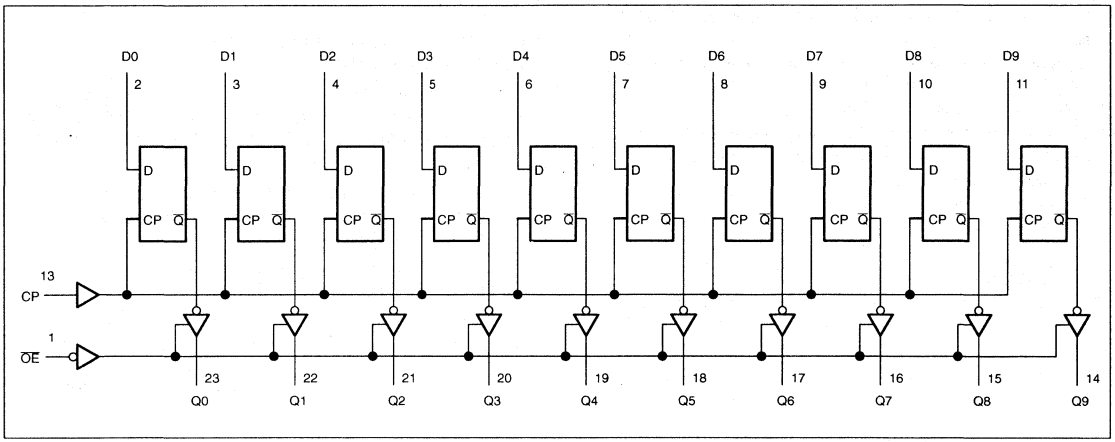
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	D0-D9	Data inputs
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	Q0-Q9	Data outputs
13	CP	Clock pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

10-bit D-type flip-flop; positive-edge trigger (3-State)

74ABT821

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn	REGISTER	Q0 – Q9	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↕	X	NC	NC	Hold
H H	↕ ↑	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low to High clock transition
↕ = Not a Low-to-High clock transition

9-bit D-type flip-flop with reset and enable (3-State)

74ABT823

FEATURES

- High speed parallel registers with positive edge-triggered D-type flip-flops
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Power-up Reset

DESCRIPTION

The 74ABT823 Bus interface Register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 'ABT823 is a 9-bit wide buffered register with Clock Enable ($\overline{CE}$) and Master Reset ($\overline{MR}$) which are ideal for parity bus interfacing in high microprogrammed systems.

The register is fully edge-triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

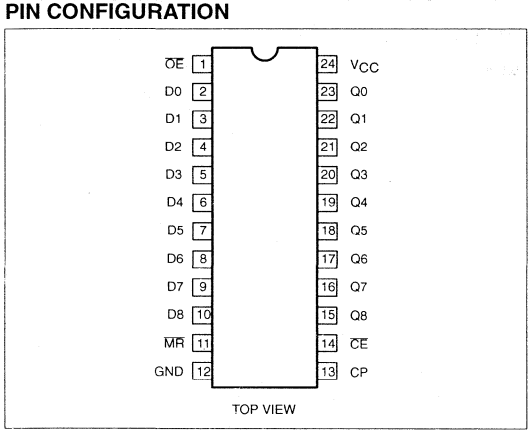
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 5V	4.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-pin plastic DIP	–40°C to +85°C	74ABT823N	0410D
24-pin plastic SOL	–40°C to +85°C	74ABT823D	0173D
24-pin plastic SSOP Type II	–40°C to +85°C	74ABT823DB	1641A

PIN CONFIGURATION



TOP VIEW

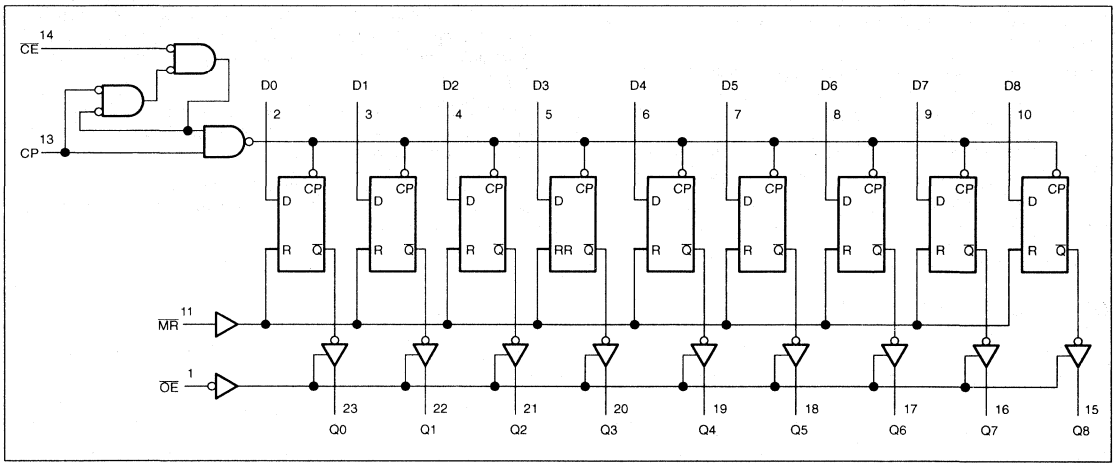
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9, 10	D0-D8	Data inputs
23, 22, 21, 20, 19,18, 17, 16, 15	Q0-Q8	Data outputs
13	CP	Clock pulse input (active rising edge)
14	$\overline{CE}$	Clock enable input (active-Low)
11	$\overline{MR}$	Master reset input (active-Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

9-bit D-type flip-flop with reset and enable (3-State)

74ABT823

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
$\overline{OE}$	$\overline{MR}$	$\overline{CE}$	CP	Dn	Q0 – Q8	
L	L	X	X	X	L	Clear
L	H	L	↑	h	H	Load and read data
L	H	L	↑	l	L	
L	H	H	↕	X	NC	Hold
H	X	X	X	X	Z	High impedance

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low to High clock transition
↕ = Not a Low-to-High clock transition

10-bit buffer/line driver, non-inverting (3-State) 74ABT827

FEATURES

- Ideal where high speed, light loading, or increased fan-in are required
- Flow through pinout architecture for microprocessor oriented applications
- Output capability: +64mA/–32mA
- Slim 300 mil-wide plastic 24–pin package
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State

DESCRIPTION

The 74ABT827 high–performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT827 10-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables ($\overline{OE}0$, $\overline{OE}1$) for maximum control flexibility.

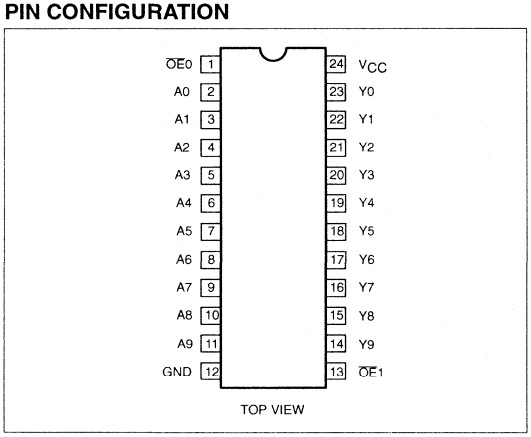
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 5V	3.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-pin plastic DIP	–40°C to +85°C	74ABT827N	0410D
24-pin plastic SOL	–40°C to +85°C	74ABT827D	0173D
24-pin plastic SSOP Type II	–40°C to +85°C	74ABT827DB	1641A

PIN CONFIGURATION

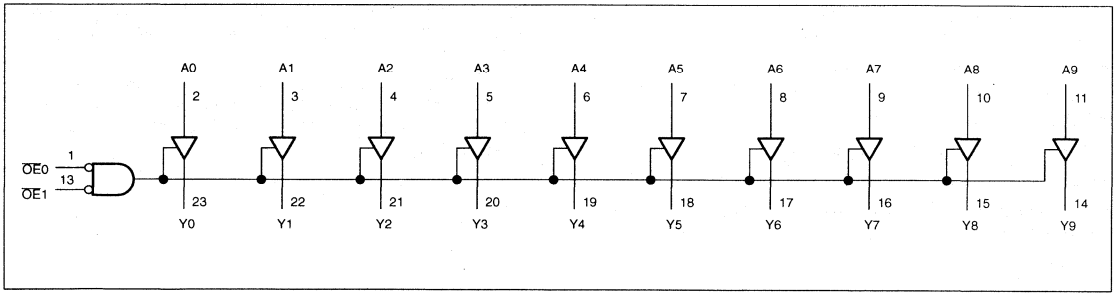


TOP VIEW

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 13	$\overline{OE}0$, $\overline{OE}1$	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	A0-A9	Data inputs
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	Y0-Y9	Data outputs
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS	OPERATING MODE
$\overline{OE}n$	An	Yn	
L	L	L	Transparent
L	H	H	Transparent
H	X	Z	High impedance

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

Octal transceiver with parity generator/checker (3-State)

74ABT833

- Low static and dynamic power dissipation with high speed and high output drive
- Open–collector $\overline{\text{ERROR}}$ output with flag register
- Output capability: +64mA/–32mA
- Latch–up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power up/down 3-State
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT833 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT833 is an octal transceiver with a parity generator/checker and is intended for bus–oriented applications.

When Output Enable A ($\overline{\text{OEA}}$) is High, it will place the A outputs in a high impedance state. Output Enable B ($\overline{\text{OEB}}$) controls the B outputs in the same way.

The parity generator creates an odd parity output (PARITY) when $\overline{\text{OEB}}$ is Low. When $\overline{\text{OEA}}$ is Low, the parity of the B port, including the PARITY input, is checked for odd parity. When an error is detected, the error data is sent to the input of a storage register. If a Low-to-High transition happens at the clock input (CP), the error data is stored in the register and the Open-collector error flag ($\overline{\text{ERROR}}$) will go Low. The error flag register is cleared with a Low pulse on the $\overline{\text{CLEAR}}$ input.

If both $\overline{\text{OEA}}$ and $\overline{\text{OEB}}$ are Low, data will flow from the A bus to the B bus and the part is forced into an error condition which creates an inverted PARITY output. This error condition can be used by the designer for system diagnostics.

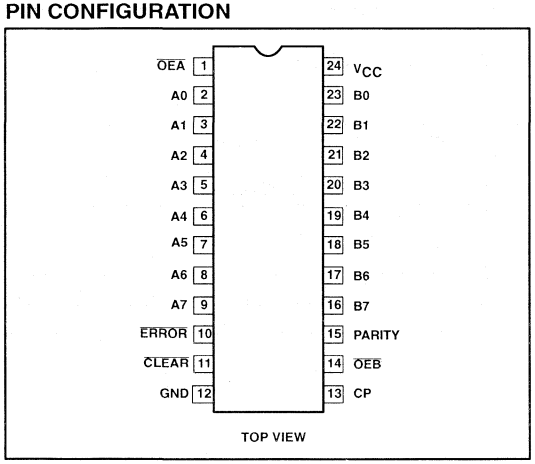
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	3.4	ns
t_{PLH} t_{PHL}	Propagation delay An to PARITY	C_L = 50pF; V_{CC} = 5V	7.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	50	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24–pin plastic DIP	–40°C to +85°C	74ABT833N	0410D
24–pin plastic SOL	–40°C to +85°C	74ABT833D	0173D
24–pin plastic SSOP Type II	–40°C to +85°C	74ABT833DB	1641A

PIN CONFIGURATION



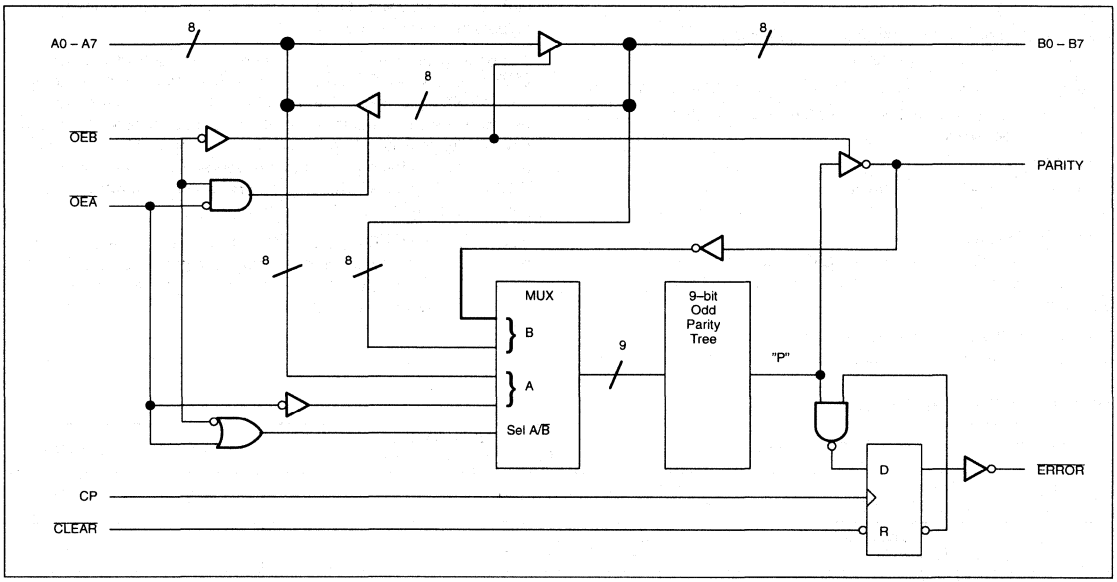
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	A port 3-State inputs/outputs
23, 22, 21, 20, 19, 18, 17, 16	B0 – B7	B port 3-State inputs/outputs
1	$\overline{\text{OEA}}$	Enables the A outputs when Low
14	$\overline{\text{OEB}}$	Enables the B outputs when Low
15	PARITY	Parity output/input
10	$\overline{\text{ERROR}}$	Error output (open collector)
11	$\overline{\text{CLEAR}}$	Clears the error flag register when Low
13	CP	Clock input
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

Octal transceiver with parity generator/checker (3-State)

74ABT833

LOGIC DIAGRAM



FUNCTION TABLE

MODE	INPUTS				OUTPUTS		
	$\overline{OEB}$	$\overline{OEA}$	An Σ of Highs	Bn + Parity Σ of Highs	An	Bn	PARITY
A data to B bus and generate odd parity output	L	H	Odd Even	(output)	(input)	An	L H
B data to A bus and check for parity error[1]	H	L	(output)	X	Bn	(input)	(input)
A bus and B bus disabled[2]	H	H	X	X	Z	Z	Z
A data to B bus and generate inverted parity output	L	L	Odd Even	(output)	(input)	An	H L

NOTES:
1. Error checking is detailed in the Error Flag Function Table below.
2. When clocked, the error output is Low if the sum of A inputs is even or High if the sum of A inputs is odd.

ERROR FLAG FUNCTION TABLE

MODE	INPUTS			Internal node	Output	
	CLEAR	CP	Bn + Parity Σ of Highs	Point "P"	Pre–state $\overline{ERROR}$n–1	$\overline{ERROR}$ OUTPUT
Sample	H H H	↑ ↑ X	Odd Even X	H L X	H X L	H L L
Hold	H	↧	X	X	X	NC
Clear	L	X	X	X	X	H

H = High voltage level steady state
L = Low voltage level steady state
X = Don't care
NC = No change
Z = High impedance "off" state
↑ = Low-to-High clock transition
↧ = Not a Low-to-High clock transition

10-bit bus interface latch (3-State) — 74ABT841

FEATURES

- High speed parallel latches
- Extra data width for wide address/data paths or buses carrying parity
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Slim DIP 300 mil package
- Broadside pinout
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Power-up reset

DESCRIPTION

The 74ABT841 Bus interface register is designed to provide extra data width for wider data/address paths of buses carrying parity.

The 'ABT841 consists of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the LE High-to-Low transition, the data that meets the setup and hold time is latched.

Data appears on the bus when the Output Enable ($\overline{OE}$) is Low. When $\overline{OE}$ is High the output is in the High-impedance state.

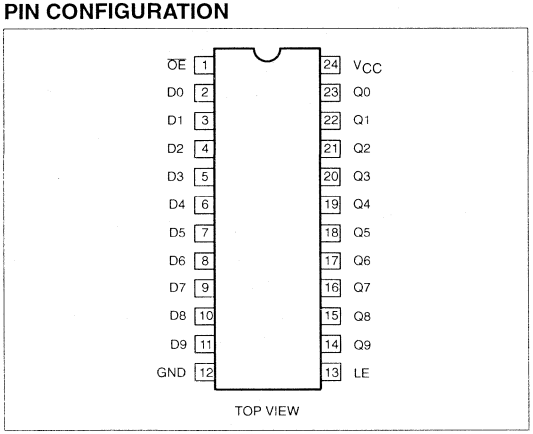
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	C_L = 50pF; V_{CC} = 5V	4.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabkled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP	–40°C to +85°C	74ABT841N
24-pin plastic SOL	–40°C to +85°C	74ABT841D
24-pin SSOP Type II	–40°C to +85°C	74ABT841DB

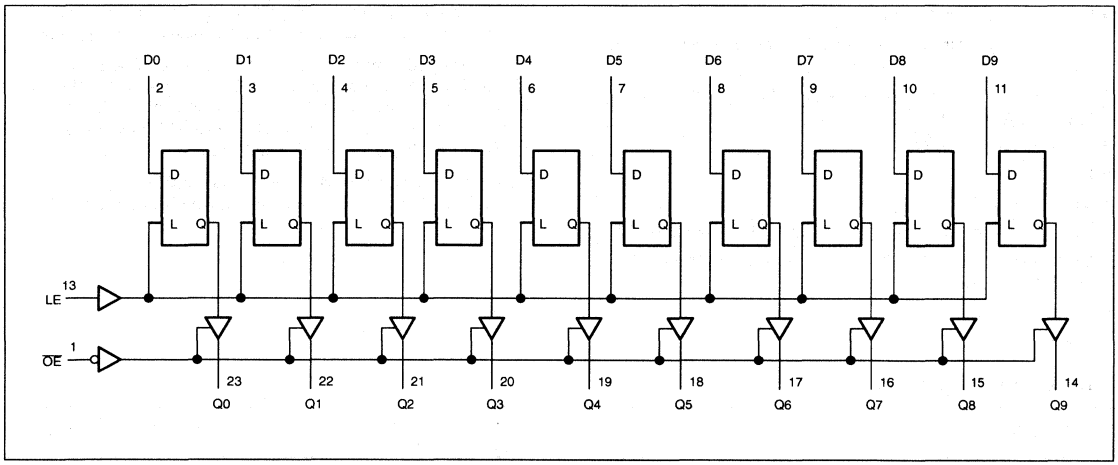
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	D0-D9	Data inputs
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	Q0-Q9	Data outputs
13	LE	Latch enable input (active falling edge)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{OE}$	LE	Dn	Q0 – Q9	
L L	H H	L H	L H	Transparent
L L	↓ ↓	l h	L H	Latched
H	X	X	Z	High impedance
L	L	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low LE transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low LE transition
↓ = High-to-Low LE transition
NC= No change
X = Don't care
Z = High impedance "off" state

9-bit bus interface latch with set and reset (3-State)

74ABT843

FEATURES

- High speed parallel latches
- Extra data width for wide address/data paths or buses carrying parity
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Slim DIP 300 mil package
- Broadside pinout
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Power-up 3-State
- Power-up reset

DESCRIPTION

The 74ABT843 Bus interface latch is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 'ABT843 consists of nine D-type latches with 3-State outputs. In addition to the LE and $\overline{OE}$ pins, it has a Master Reset ($\overline{MR}$) pin and Preset ($\overline{PRE}$) pin. These pins are ideal for parity bus interfacing in high performance systems. When $\overline{MR}$ is Low, the outputs are Low if $\overline{OE}$ is Low. When $\overline{MR}$ is High, data can be entered into the latch. When $\overline{PRE}$ is Low, the outputs are High, if $\overline{OE}$ is Low. $\overline{PRE}$ overrides $\overline{MR}$.

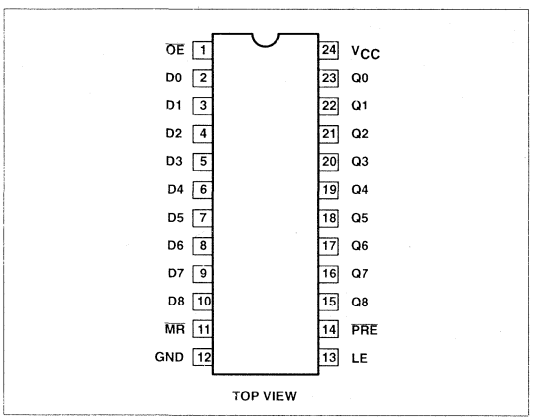
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	C_L = 50pF; V_{CC} = 5V	5.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-pin plastic DIP	–40°C to +85°C	74ABT843N	0410D
24-pin plastic SOL	–40°C to +85°C	74ABT843D	0173D
24-pin SSOP Type II	–40°C to +85°C	74ABT843DB	1641A

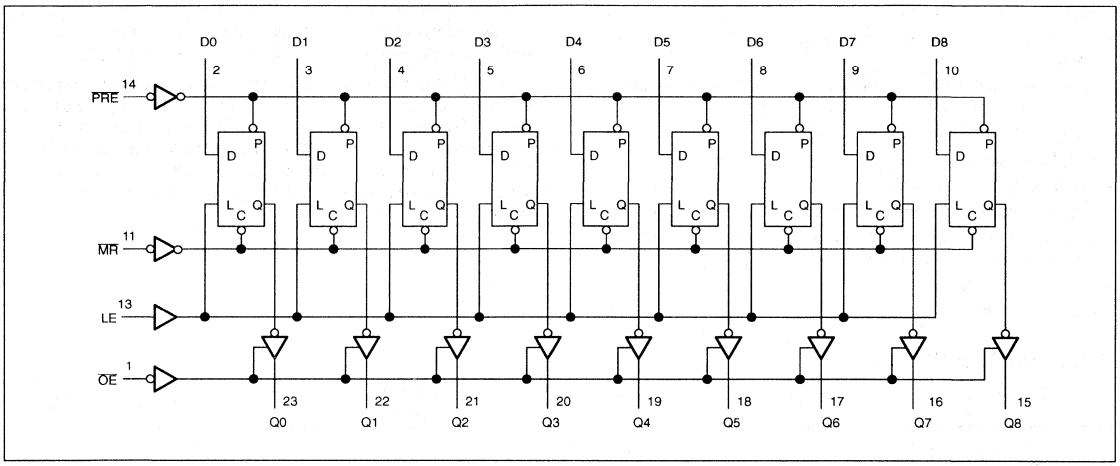
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9, 10	D0-D8	Data inputs
23, 22, 21, 20, 19, 18, 17, 16, 15	Q0-Q8	Data outputs
11	$\overline{MR}$	Master reset input (active-Low)
13	LE	Latch enable input (active rising edge)
14	$\overline{PRE}$	Preset input (active-Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
$\overline{OE}$	$\overline{PRE}$	$\overline{MR}$	LE	Dn	Qn	
L	L	X	X	X	H	Preset
L	H	L	X	X	L	Clear
L L	H H	H H	H H	L H	L H	Transparent
L L	H H	H H	↓ ↓	l h	L H	Latched
H	X	X	X	X	Z	High impedance
L	H	H	L	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low LE transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low LE transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low transition

8-bit bus interface latch with set and reset (3-State)

74ABT845

FEATURES

- High speed parallel latches
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Broadside pinout
- Output capability: +64mA/–32mA
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT845 consists of eight D–type latches with 3-State outputs. In addition to the LE, $\overline{OE}$, $\overline{MR}$ and $\overline{PRE}$ pins, the 'ABT845 has two additional $\overline{OE}$ pins, making a total of three Output Enable ($\overline{OE}0$, $\overline{OE}1$, $\overline{OE}2$) pins. The multiple Output enables allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$.

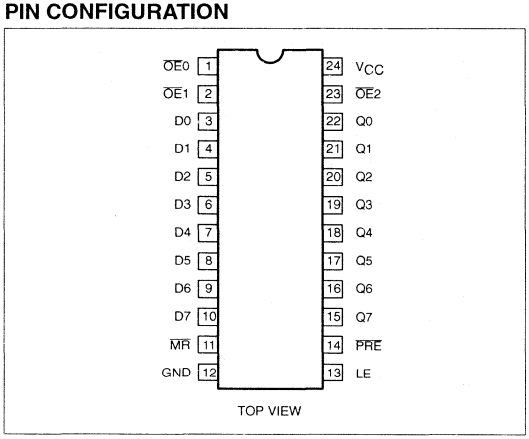
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	C_L = 50pF; V_{CC} = 5V	5.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-Pin Plastic DIP	–40°C to +85°C	74ABT845N	0410D
24–Pin Plastic SOL	–40°C to +85°C	74ABT845D	0173D
24-Pin Plastic SSOP	–40°C to +85°C	74ABT845DB	1641A

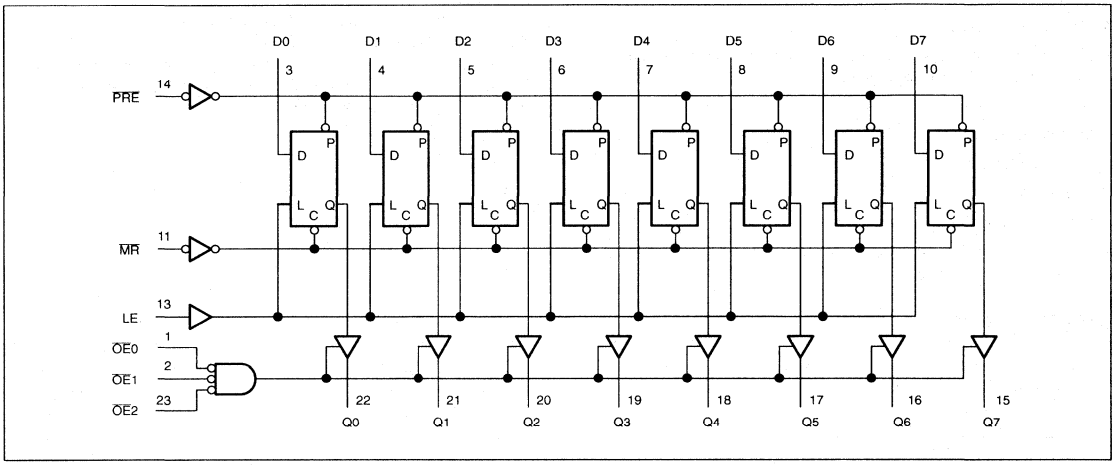
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 2, 23	$\overline{OE}0$ – $\overline{OE}2$	Output enable inputs (active-Low)
3, 4, 5, 6, 7, 8, 9, 10	D0-D7	Data inputs
22, 21, 20, 19,18, 17, 16, 15	Q0-Q7	Data outputs
11	$\overline{MR}$	Master reset input (active-Low)
13	LE	Latch enable input (active-High)
14	$\overline{PRE}$	Preset input (active-Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
$\overline{OE}n$	$\overline{PRE}$	$\overline{MR}$	LE	Dn	Qn	
L	L	X	X	X	H	Preset
L	H	L	X	X	L	Clear
L L	H H	H H	H H	L H	L H	Transparent
L L	H H	H H	↓ ↓	l h	L H	Latched
H	X	X	X	X	Z	High impedance
L	H	H	L	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low LE transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low LE transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low transition

8-bit transceiver with 9-bit parity checker/ generator and flag latch (3-State)

74ABT853

FEATURES

- Low static and dynamic power dissipation with high speed and high output drive
- Open-collector $\overline{\text{ERROR}}$ output
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT853 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT853 is an octal transceiver with a parity generator/checker and is intended for bus–oriented applications.

When Output Enable A ($\overline{\text{OEA}}$) is High, it will place the A outputs in a high impedance state. Output Enable B ($\overline{\text{OEB}}$) controls the B outputs in the same way.

The parity generator creates an odd parity output (PARITY) when $\overline{\text{OEB}}$ is Low. When $\overline{\text{OEA}}$ is Low, the parity of the B port, including the PARITY input, is checked for odd parity. When an error is detected, the error data is sent to the input of a latch. The error data can then be passed, stored, cleared, or sampled depending on the $\overline{\text{ENABLE}}$ and $\overline{\text{CLEAR}}$ control signals.

If both $\overline{\text{OEA}}$ and $\overline{\text{OEB}}$ are Low, data will flow from the A bus to the B bus and the part is forced into an error condition which creates an inverted PARITY output. This error condition can be used by the designer for system diagnostics.

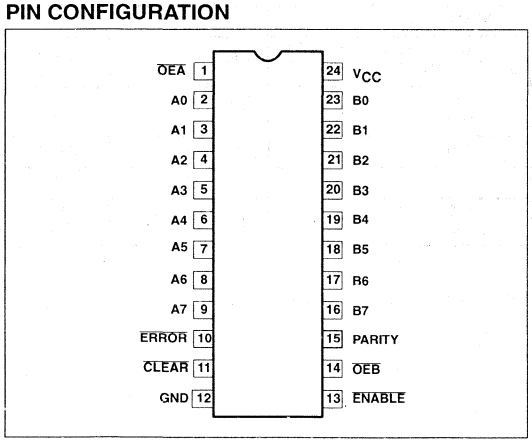
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	3.4	ns
t_{PLH} t_{PHL}	Propagation delay An to PARITY	C_L = 50pF; V_{CC} = 5V	7.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	50	µA

ORDERING INFORMATION

PACKAGES	CONDITIONS T_{amb} = 25°C; GND = 0V	ORDER CODE	DRAWING NUMBER
24-pin plastic DIP	-40°C to +85°C	74ABT853N	0410D
24-pin plastic SOL	-40°C to +85°C	74ABT853D	0173D
24–pin SSOP Type II	-40°C to +85°C	74ABT853DB	1641A

PIN CONFIGURATION



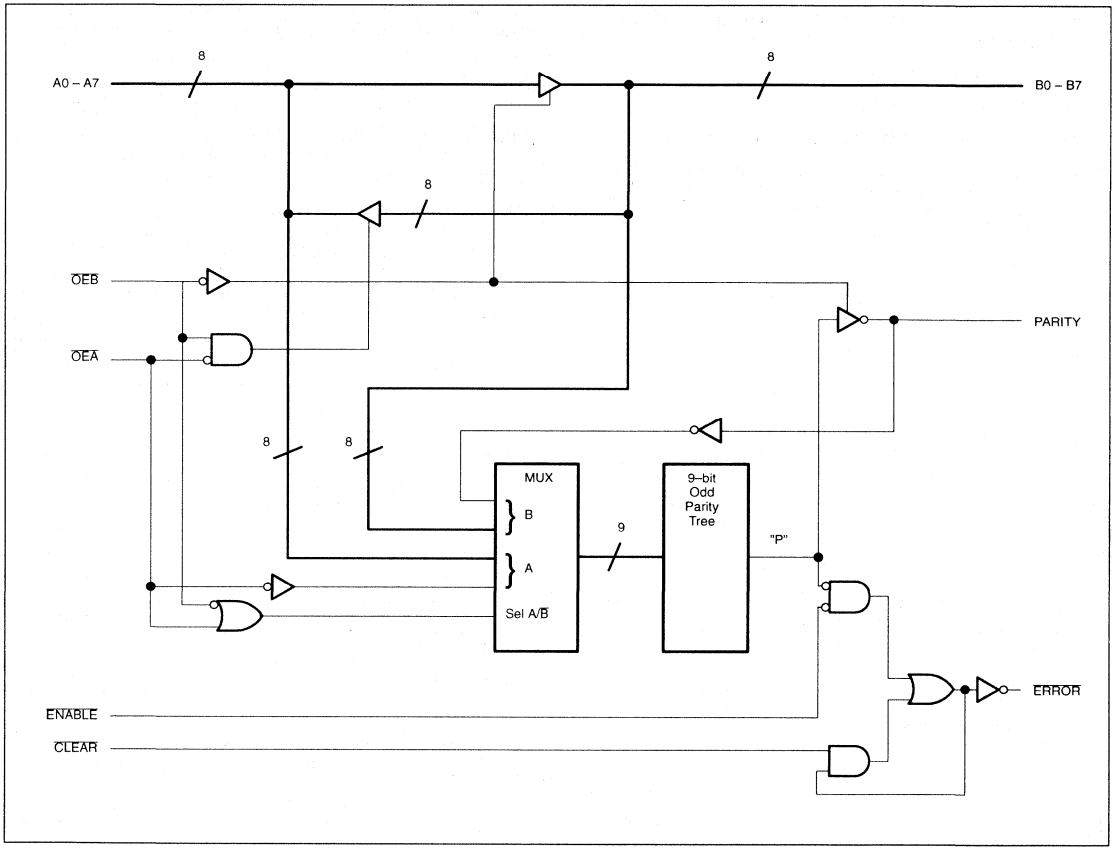
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	A port 3–State inputs/outputs
23, 22, 21, 20, 19, 18, 17, 16	B0 – B7	B port 3–State inputs/outputs
1	$\overline{\text{OEA}}$	Enables the A outputs when Low
14	$\overline{\text{OEB}}$	Enables the B outputs when Low
15	PARITY	Parity output/input
10	$\overline{\text{ERROR}}$	Error output (open collector)
11	$\overline{\text{CLEAR}}$	Clears the error flag register when Low
13	$\overline{\text{ENABLE}}$	Enable input (active-Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

8-bit transceiver with 9-bit parity checker/ generator and flag latch (3-State)

74ABT853

LOGIC DIAGRAM



FUNCTION TABLE

MODE	INPUTS				OUTPUTS		
	$\overline{OEB}$	$\overline{OEA}$	An Σ OF HIGHS	Bn + PARITY Σ OF HIGHS	An	Bn	PARITY
A data to B bus and generate odd parity output	L	H	Odd Even	(output)	(input)	An	L H
B data to A bus and check for parity error[1]	H	L	(output)	X	Bn	(input)	(input)
A bus and B bus disabled[2]	H	H	X	X	Z	Z	Z
A data to B bus and generate inverted parity output	L	L	Odd Even	(output)	(input)	An	H L

NOTES:
1. Error checking is detailed in the Error Flag Function Table below.
2. When $\overline{ENABLE}$ is Low, $\overline{ERROR}$ is Low if the sum of A inputs is even or $\overline{ERROR}$ is High if the sum of A inputs is odd.

ERROR FLAG FUNCTION TABLE

MODE	INPUTS			INTERNAL NODE	OUTPUT	
	$\overline{\text{ENABLE}}$	$\overline{\text{CLEAR}}$	Bn + PARITY Σ OF HIGHS	POINT "P"	PRE-STATE $\overline{\text{ERROR}}$n-1	$\overline{\text{ERROR}}$ OUTPUT
Pass	L	L	Odd Even	H L	X	H L
Sample	L	H	Odd Even X	H L X	H X L	H L L
Clear	H	L	X	X	X	H
Store	H	H	X	X	L H	L H

H = High voltage level steady state
L = Low voltage level steady state
X = Don't care
Z = High impedance "off" state

10-bit bus transceiver (3-State) 74ABT861

FEATURES

- Buffered control inputs for light loading, or increased fan-in as required with MOS microprocessors
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State

DESCRIPTION

The 74ABT861 bus transceiver provides high performance bus interface buffering for wide data/address paths of buses carrying parity.

The 'ABT861 10-bit bus transceiver has NOR-ed transmit and receive output enables for maximum control flexibility.

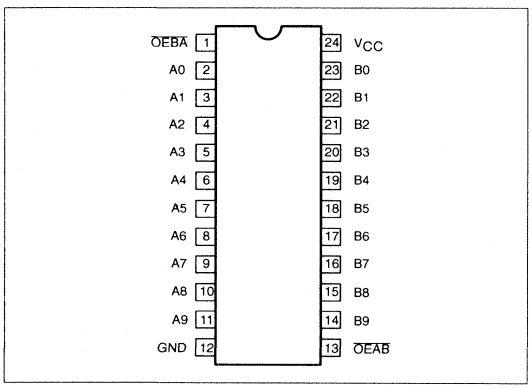
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	3.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-pin plastic DIP	–40°C to +85°C	74ABT861N	0410D
24-pin plastic SOL	–40°C to +85°C	74ABT861D	0173D
24-pin SSOP Type II	–40°C to +85°C	74ABT861DB	1641A

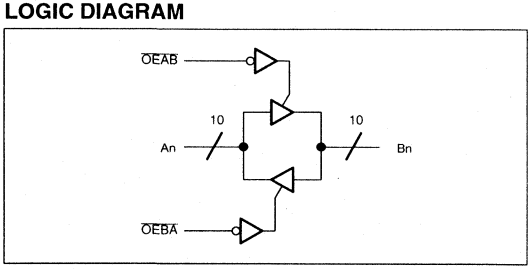
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
13	$\overline{OEAB}$	A side to B side output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	A0-A9	Data inputs/outputs (A side)
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	B0-B9	Data inputs/outputs (B side)
1	$\overline{OEBA}$	B side to A side output enable input (active-Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OPERATING MODE
$\overline{OEAB}$	$\overline{OEBA}$	
L	H	A data to B bus
H	L	B data to A bus
H	H	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

9-bit bus transceiver (3-State) 74ABT863

FEATURES

- Provides high performance bus interface buffering for wide data/address paths or buses carrying parity
- Buffered control inputs for light loading, or increased fan–in as required with MOS microprocessors
- Output capability: +64mA/–32mA
- Latch–up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT863 bus transceiver provides high performance bus interface buffering for wide data/address paths of buses carrying parity.

The 'ABT863 9-bit bus transceiver has NOR-ed transmit and receive output enables for maximum control flexibility.

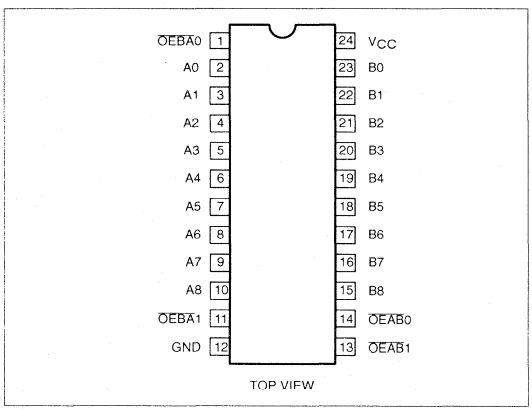
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	3.3	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	110	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-pin plastic DIP	–40°C to +85°C	74ABT863N	0410D
24-pin plastic SOL	–40°C to +85°C	74ABT863D	0173D
24-pin SSOP Type II	–40°C to +85°C	74ABT863DB	1641A

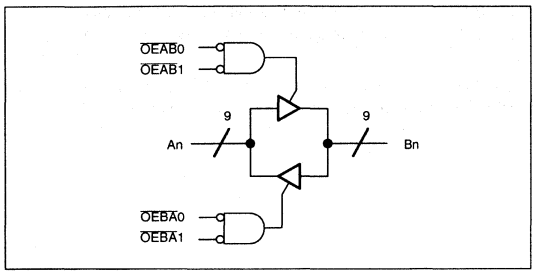
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
14, 13	$\overline{OEAB0}$, $\overline{OEAB1}$	Output enable inputs (active-Low)
2, 3, 4, 5, 6, 7, 8, 9, 10	A0-A8	Data inputs/outputs (A side)
23, 22, 21, 20, 19, 18, 17, 16, 15	B0-B8	Data inputs/outputs (B side)
1, 11	$\overline{OEBA0}$, $\overline{OEBA1}$	Output enable inputs (active-Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OPERATING MODE
$\overline{OEAB0}$	$\overline{OEAB1}$	$\overline{OEBA0}$	$\overline{OEBA1}$	
L	L	H	X	A data to B bus
L	L	X	H	A data to B bus
H	X	L	L	B data to A bus
X	H	L	L	B data to A bus
H	H	H	H	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

9-bit dual latch transceiver with 8-bit parity generator/checker (3-State)

74ABT899

FEATURES

- Symmetrical (A and B bus functions are identical)
- Selectable generate parity or "feed–through" parity for A-to-B and B-to-A directions
- Independent transparent latches for A-to-B and B-to-A directions
- Selectable ODD/$\overline{\text{EVEN}}$ parity
- Continuously checks parity of both A bus and B bus latches as $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$
- Ability to simultaneously generate and check parity
- Can simultaneously read/latch A and B bus data
- Output capability: +64 mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power up 3-State
- Power-up reset
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT899 is a 9-bit to 9-bit parity transceiver with separate transparent latches for the A bus and B bus. Either bus can generate or check parity. The parity bit can be fed–through with no change or the generated parity can be substituted with the $\overline{\text{SEL}}$ input.

Parity error checking of the A and B bus latches is continuously provided with $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$, even with both buses in 3–State.

The 74ABT899 features independent latch enables for the A and B bus latches, a select pin for ODD/$\overline{\text{EVEN}}$ parity, and separate error signal output pins for checking parity.

FUNCTIONAL DESCRIPTION:

The 74ABT899 has three principal modes of operation which are outlined below. All modes apply to both the A-to-B and B-to-A directions.

Transparent latch, Generate parity, Check A and B bus parity:
Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as BPAR (APAR). If LEA and LEB are High and the Mode Select ($\overline{\text{SEL}}$) is Low, the parity generated from A0-A7 and B0-B7 can be checked and monitored by $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$. (Fault detection on both input and output buses.)

Transparent latch, Feed–through parity, Check A and B bus parity:
Bus A (B) communicates to Bus B (A) in a feed-through mode if $\overline{\text{SEL}}$ is High. Parity is still generated and checked as $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ and can be used as an interrupt to signal a data/parity bit error to the CPU.

Latched input, Generate/Feed–through parity, Check A (and B) bus parity:
Independent latch enables (LEA and LEB) allow other permutations of:

- Transparent latch / 1 bus latched / both buses latched
- Feed–through parity / generate parity
- Check in bus parity / check out bus parity / check in and out bus parity

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	2.9	ns
t_{PLH} t_{PHL}	Propagation delay An to $\overline{\text{ERRA}}$	C_L = 50pF; V_{CC} = 5V	6.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	50	µA

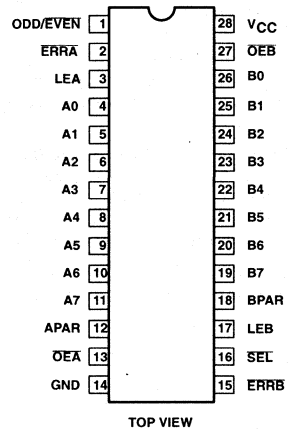
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWINGNUMBER
28–pin PLCC	–40°C to +85°C	74ABT899A	0401F
28–pin plastic SOL	–40°C to +85°C	74ABT899D	0006C

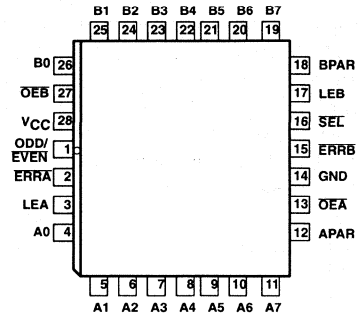
9-bit dual latch transceiver with 8-bit parity generator/checker (3-State)

74ABT899

PIN CONFIGURATIONS



TOP VIEW



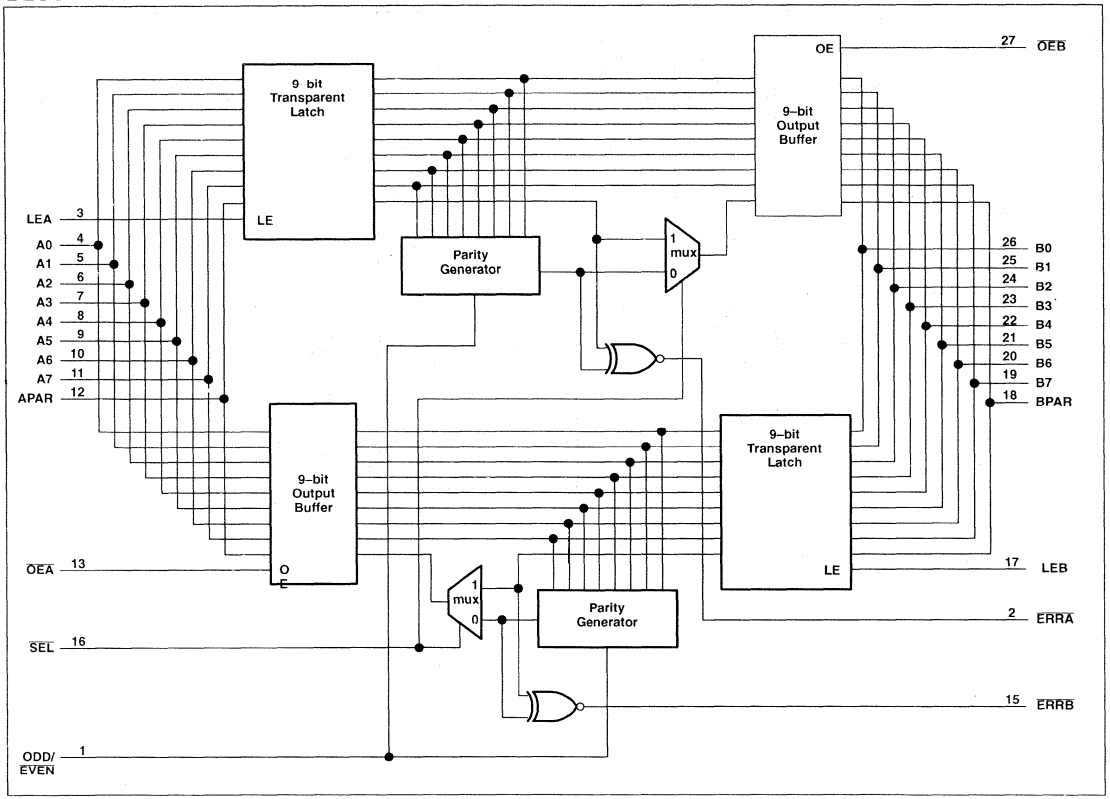
PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
A0 – A7	4, 5, 6, 7, 8, 9, 10, 11	Latched A bus 3-State inputs/outputs
B0 – B7	19, 20, 21, 22, 23, 24, 25, 26	Latched B bus 3-State inputs/outputs
APAR	12	A bus parity 3-State input
BPAR	18	B bus parity 3-State input
ODD/$\overline{\text{EVEN}}$	1	Parity select input (Low for EVEN parity)
$\overline{\text{OEA}}$, $\overline{\text{OEB}}$	13, 27	Output enable inputs (gate A to B, B to A)
$\overline{\text{SEL}}$	16	Mode select input (Low for generate)
LEA, LEB	3, 17	Latch enable inputs (transparent High)
$\overline{\text{ERRA}}$, $\overline{\text{ERRB}}$	2, 15	Error signal outputs (active-Low)
GND	14	Ground (0V)
V_{CC}	28	Positive supply voltage

9-bit dual latch transceiver with 8-bit parity generator/checker (3-State)

74ABT899

BLOCK DIAGRAM



FUNCTION TABLE

INPUTS					OPERATING MODE
$\overline{OEB}$	$\overline{OEA}$	$\overline{SEL}$	LEA	LEB	
H	H	X	X	X	3–State A bus and B bus (input A & B simultaneously)
H	L	L	L	H	B → A, transparent B latch, generate parity from B0 – B7, check B bus parity
H	L	L	H	H	B → A, transparent A & B latch, generate parity from B0 – B7, check A & B bus parity
H	L	L	X	L	B → A, B bus latched, generate parity from latched B0 – B7 data, check B bus parity
H	L	H	X	H	B → A, transparent B latch, parity feed–through, check B bus parity
H	L	H	H	H	B → A, transparent A & B latch, parity feed–through, check A & B bus parity
L	H	L	H	X	A → B, transparent A latch, generate parity from A0 – A7, check A bus parity
L	H	L	H	H	A → B, transparent A & B latch, generate parity from A0 – A7, check A & B bus parity
L	H	L	L	X	A → B, A bus latched, generate parity from latched A0 – A7 data, check A bus parity
L	H	H	H	L	A → B, transparent A latch, parity feed–through, check A bus parity
L	H	H	H	H	A → B, transparent A & B latch, parity feed–through, check A & B bus parity
L	L	X	X	X	Output to A bus and B bus (NOT ALLOWED)

H = High voltage level
L = Low voltage level
X = Don't care

PARITY AND ERROR FUNCTION TABLE

INPUTS				OUTPUTS			PARITY MODES	
$\overline{SEL}$	ODD/$\overline{EVEN}$	xPAR (A or B)	Σ of High Inputs	xPAR (B or A)	$\overline{ERRt}$	$\overline{ERRr}$*		
H	H	H	Even Odd	H H	H L	H L	Odd Mode	Feed–through/check parity
H	H	L	Even Odd	L L	L H	L H		
H	L	H	Even Odd	H H	L H	L H	Even Mode	
H	L	L	Even Odd	L L	H L	H L		
L	H	H	Even Odd	H L	H L	H H	Odd Mode	Generate parity
L	H	L	Even Odd	H L	L H	H H		
L	L	H	Even Odd	L H	L H	H H	Even Mode	
L	L	L	Even Odd	L H	H L	H H		

H = High voltage level
L = Low voltage level
t = Transmit–if the data path is from A→B then $\overline{ERRt}$ is $\overline{ERRA}$
r = Receive–if the data path is from A→B then $\overline{ERRr}$ is $\overline{ERRB}$
* Blocked if latch is not transparent

Octal registered transceiver (3-State) 74ABT2952

FEATURES

- 8-bit registered transceiver
- Independent registers for A and B buses
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Power-up reset
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT2952 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT2952 device is an 8-bit registered transceiver. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{CEXX}$) is Low. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable ($\overline{OEXX}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

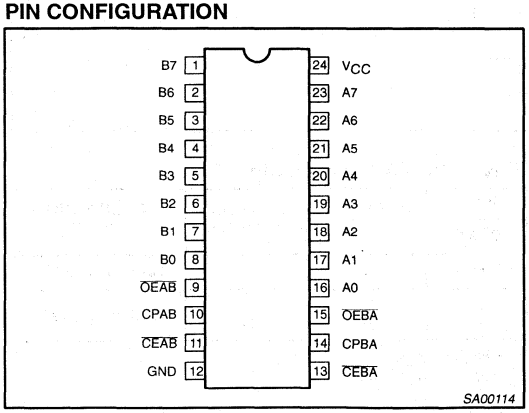
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPBA to An or CPAB to Bn	C_L = 50pF; V_{CC} = 5V	5.7	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	110	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-pin plastic DIP	–40°C to +85°C	74ABT2952N	SOT222
24-pin plastic SOL	–40°C to +85°C	74ABT2952D	SOT137-1
24-pin plastic SSOP Type II	–40°C to +85°C	74ABT2952DB	SOT340-1
24-pin plastic TSSOP Type I	–40°C to +85°C	74ABT2952PW	SOT355-1

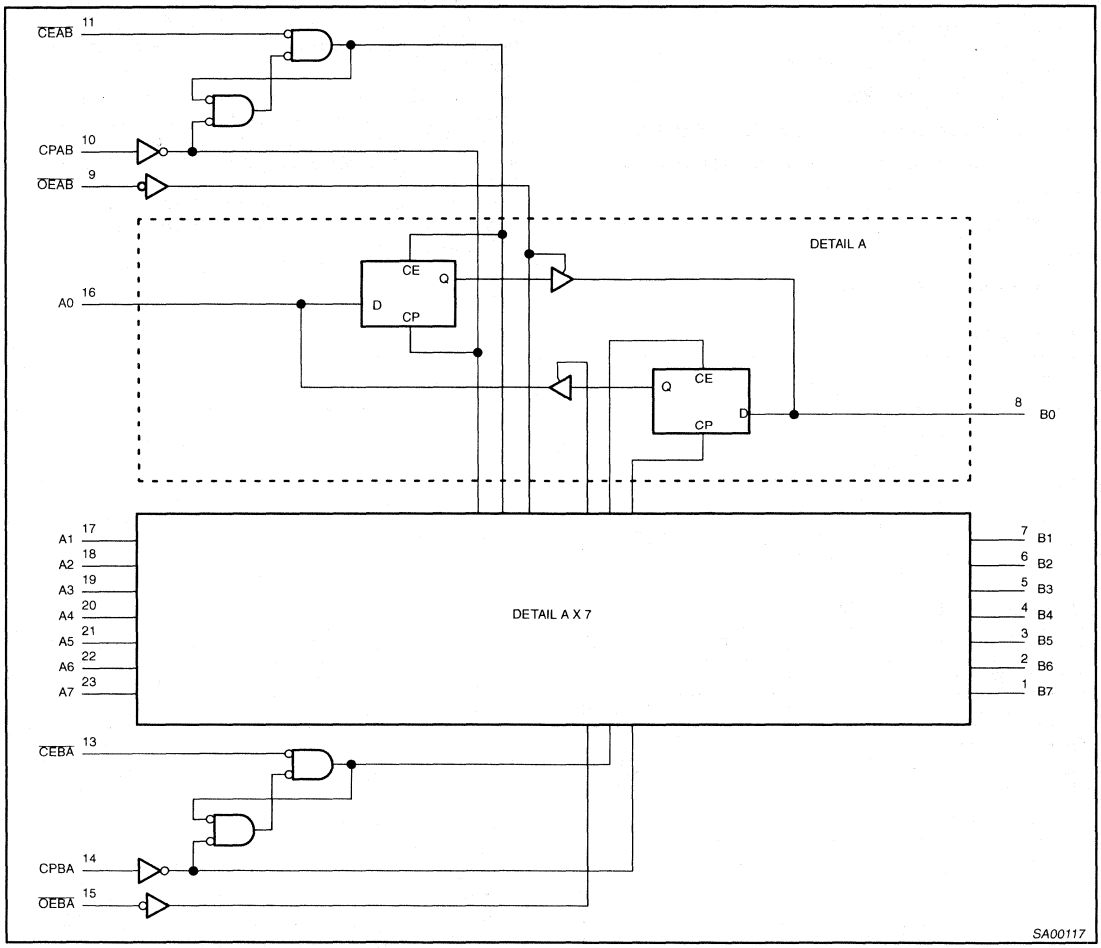
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
10, 14	CPAB / CPBA	Clock input A to B / Clock input B to A
11, 13	$\overline{CEAB}$ / $\overline{CEBA}$	Clock enable input A to B / Clock enable input B to A
16, 17, 18, 19, 20, 21, 22, 23	A0 – A7	Data inputs/outputs (A side)
1, 2, 3, 4, 5, 6, 7, 8	B0 – B7	Data outputs/outputs (B side)
9, 15	$\overline{OEAB}$ / $\overline{OEBA}$	Output enable inputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE for Register An or Bn

INPUTS			INTERNAL Q	OPERATING MODE
An or Bn	CPXX	$\overline{CEXX}$		
X	X	H	NC	Hold data
L H	↑ ↑	L L	L H	Load data

H = High voltage level
L = Low voltage level
↑ = Low–to–High transition
X = Don't care
XX = AB or BA
NC = No change

FUNCTION TABLE for Output Enable

INPUTS	INTERNAL Q	An or Bn OUTPUTS	OPERATING MODE
$\overline{OEXX}$			
H	X	Z	Disable outputs
L L	L H	L H	Enable outputs

H = High voltage level
L = Low voltage level
X = Don't care
XX = AB or BA
Z = High impedance "off" state

Octal registered transceiver, inverting (3-State) 74ABT2953

FEATURES

- 8-bit registered transceiver
- Independent registers for A and B buses
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset

DESCRIPTION

The 74ABT2953 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT2953 device is an 8-bit registered inverting transceiver. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{CEXX}$) is Low. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable ($\overline{OEXX}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

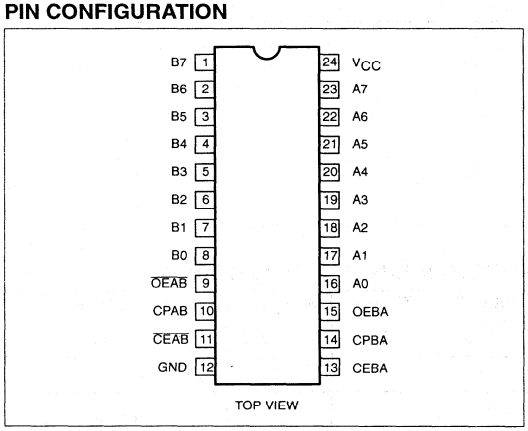
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPBA to $\overline{An}$ or CPAB to $\overline{Bn}$	C_L = 50pF; V_{CC} = 5V	5.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-pin plastic DIP	–40°C to +85°C	74ABT2953N	0410D
24-pin plastic SOL	–40°C to +85°C	74ABT2953D	0173D
24-pin plastic SSOP II	–40°C to +85°C	74ABT2953DB	1641A

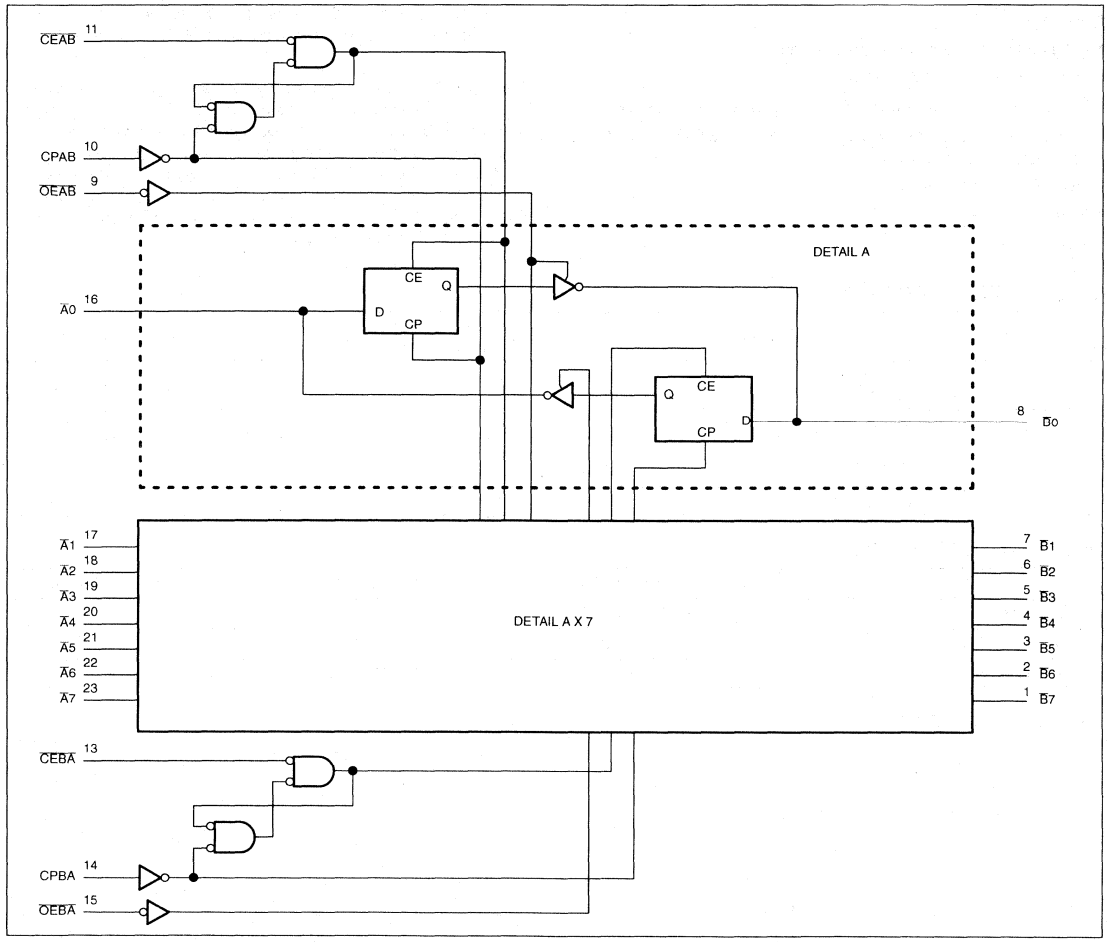
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
10, 14	CPAB / CPBA	Clock input A to B / Clock input B to A
11, 13	$\overline{CEAB}$ / $\overline{CEBA}$	Clock enable input A to B / Clock enable input B to A
16, 17, 18, 19, 20, 21, 22, 23	A0 – A7	Data inputs/outputs (A side)
1, 2, 3, 4, 5, 6, 7, 8	B0 – B7	Data outputs/outputs (B side)
9, 15	$\overline{OEAB}$ / $\overline{OEBA}$	Output enable inputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE for Register An or Bn

INPUTS			INTERNAL	OPERATING
An or Bn	CPXX	$\overline{CEXX}$	Q	MODE
X	X	H	NC	Hold data
L H	↑ ↑	L L	L H	Load data

H = High voltage level
L = Low voltage level
↑ = Low-to-High transition
X = Don't care
XX = AB or BA
NC = No change

FUNCTION TABLE for Output Enable

INPUTS	INTERNAL	An or Bn	OPERATING
$\overline{OEXX}$	Q	OUTPUTS	MODE
H	X	Z	Disable outputs
L L	L H	H L	Enable outputs

H = High voltage level
L = Low voltage level
X = Don't care
XX = AB or BA
Z = High impedance "off" state

Synchronizing dual D-type flip-flop with metastable immune characteristics

74ABT5074

FEATURES

- Metastable immune characteristics
- Pin compatible with 74F74 and 74F5074
- Typical f_{MAX} = 200MHz
- Output skew guaranteed less than 2.0ns
- High source current (I_{OH} = 15mA) ideal for clock driver applications
- Output capability: +20mA/–15mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT5074 is a dual positive edge-triggered D-type flip-flop featuring individual data, clock, set and reset inputs; also true and complementary outputs.

Set ($\overline{SD}n$) and reset ($\overline{RD}n$) are asynchronous active low inputs and operate independently of the clock (CPn) input. Data must be stable just one setup time prior to the low-to-high transition of the clock for guaranteed propagation delays.

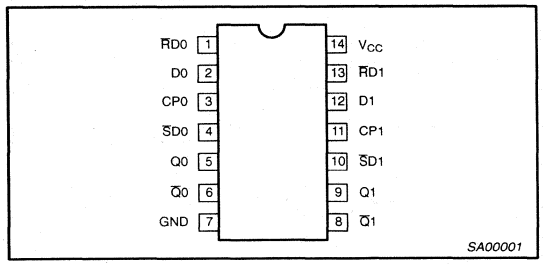
Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the Dn input may be changed without affecting the levels of the output.

The 74ABT5074 is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup time and hold time are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74ABT5074 are:

$$\tau \cong 94\text{ps and } T_0 \cong 1.3 \times 10^7 \text{ sec}$$

where τ represents a function of the rate at which a latch in a metastable state resolves that condition and T_0 represents a function of the measurement of the propensity of a latch to enter a metastable state.

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 12	D0, D1	Data inputs
3, 11	CP0, CP1	Clock inputs (active rising edge)
4, 10	$\overline{SD}0$, $\overline{SD}1$	Set inputs (active-Low)
1, 13	$\overline{RD}0$, $\overline{RD}1$	Reset inputs (active-Low)
5, 9	Q0, Q1	Data outputs (active-Low), non-inverting
6, 8	$\overline{Q}0$, $\overline{Q}1$	Data outputs (active-Low), inverting
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Qn}$	C_L = 50pF; V_{CC} = 5V	2.8 2.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
I_{CC}	Total supply current	Outputs disabled; V_{CC} =5.5V	2	µA

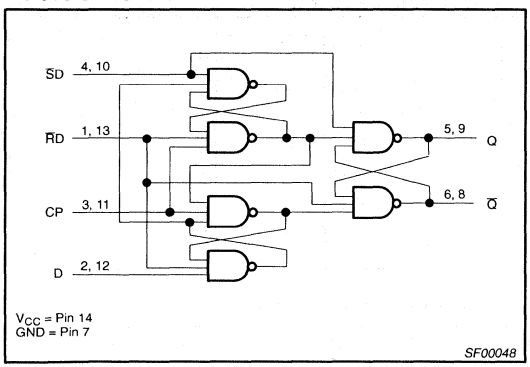
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
14-pin plastic DIP	–40°C to +85°C	74ABT5074N	SOT27-1
14-pin plastic SOL	–40°C to +85°C	74ABT5074D	SOT108-1
14-pin plastic shrink small outline SSOP Type II	–40°C to +85°C	74ABT5074DB	SOT337-1
14-pin plastic thin shrink small outline (TSSOP) Type I	–40°C to +85°C	74ABT5074PW	SOT402-1

Synchronizing dual D-type flip-flop with metastable immune characteristics

74ABT5074

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$	
L	H	X	X	H	L	Asynchronous set
H	L	X	X	L	H	Asynchronous reset
L	L	X	X	L	H	Undetermined*
H	H	↑	h	H	L	Load "1"
H	H	↑	l	L	H	Load "0"
H	H	↕	X	NC	NC	Hold

NOTES:

H = High voltage level
h = High voltage level one setup time prior to low-to-high clock transition
L = Low voltage level
l = Low voltage level one setup time prior to low-to-high clock transition
NC= No change from the previous setup
X = Don't care
↑ = Low-to-high clock transition
↕ = Not low-to-high clock transition
* = This setup is unstable and will change when either set or reset return to the high level

ABT Netlists

ABT BERKELEY SPICE MODELS

```
* ABT Test Circuit
* ABTBS.CIR
* Advanced BiCMOS Logic
* Standard Logic Product Group, Philips Semiconductors
* 12/15/94
*****************************************************************************
*
* To simulate a particular device, go to the section of the file under
* the heading "Start Running Circuit Model" and remove the comment
* statement "*" before the required device.  All other devices must have
* a "*" comment statement.  If you like to simulate with fast or slow
* parameters, go to the section of the file under heading "Process and
* Subcircuit Models" and remove the comment statement "*" before the
* required process model.  You may simulate only one device at a time.
* The load circuit may be adapted to your specific situation.  Also, pin
* inductances used in the subcircuit files use nominal values.  To more
* accurately simulate a particular device package, refer to the package
* inductance tables for a particular package type and substitute those
* values into the subcircuit file.
*
*****************************************************************************
*
* These models represent only one data input and one output of a device.
* Other control inputs such as direction, clock, and output enables are
* not modeled.  Circuitry in between the input and output are also not
* included such as gates, latches, and intermediate buffers.  The result
* is that the model does not show the exact function of the device, and
* propagation delays may not match the published AC specifications in
* the datasheet.
*
*****************************************************************************

*** Process and Subcircuit Models ***

* Nominal parameters
.INC C:\SPICE\ABT\ABTMODN.BSP
.INC C:\SPICE\ABT\ABTNOM.SUB

* Fast parameters
* .INC C:\SPICE\ABT\ABTMODF.BSP
* .INC C:\SPICE\ABT\ABTFAS.SUB


* Slow parameters
* .INC C:\SPICE\ABT\ABTMODS.BSP
* .INC C:\SPICE\ABT\ABTSLO.SUB
```

```
*** Start Running Circuit Model ***
* Parts with an "X" suffix are "-1" parts with the 30 ohm series
* termination resistors

* Part Type        In    Out   Vcc   Gnd   Subcircuit Name

* XABT125          2     4     99    0     BUFFER1
* XABT126          2     4     99    0     BUFFER1
* XABT240          2     4     99    0     INVBUFFER1
* XABT240X         2     4     99    0     INVBUFFER2
* XABT241          2     4     99    0     BUFFER2
* XABT244          2     4     99    0     BUFFER2
* XABT244X         2     4     99    0     BUFFER3
* XABT245          2     4     99    0     BUFFER2
* XABT245X         2     4     99    0     BUFFER4
* XABT273A         2     4     99    0     FLOP4
* XABT373A         2     4     99    0     FLOP4
* XABT374A         2     4     99    0     FLOP4
* XABT377          2     4     99    0     FLOP1
* XABT534          2     4     99    0     INVFLOP
* XABT540          2     4     99    0     INVBUFFER1
* XABT541          2     4     99    0     BUFFER2
* XABT543A         2     4     99    0     FLOP4
* XABT544          2     4     99    0     FLOP5
* XABT573          2     4     99    0     FLOP2
* XABT574          2     4     99    0     FLOP2
* XABT620          2     4     99    0     INVBUFFER1
* XABT623          2     4     99    0     BUFFER2
* XABT640          2     4     99    0     INVBUFFER1
* XABT646A         2     4     99    0     FLOP4
* XABT648          2     4     99    0     FLOP5
* XABT651          2     4     99    0     FLOP4
* XABT652A         2     4     99    0     FLOP4
* XABT657          2     4     99    0     BUFFER5
* XABT821          2     4     99    0     FLOP3
* XABT823          2     4     99    0     FLOP3
* XABT827          2     4     99    0     BUFFER5
* XABT833          2     4     99    0     BUFFER5
* XABT841          2     4     99    0     FLOP3
* XABT843          2     4     99    0     FLOP3
* XABT845          2     4     99    0     FLOP3
* XABT853          2     4     99    0     BUFFER5
* XABT861          2     4     99    0     BUFFER5
* XABT863          2     4     99    0     BUFFER5
* XABT899          2     4     99    0     FLOP6
* XABT2952         2     4     99    0     FLOP3
* XABT2953         2     4     99    0     FLOP5
* XABT5074         2     4     99    0     FLOP7
*** External Test Load ***
RL1   4           0     500
CL1   4           0     50PF
*****************************

VCC               99    0     DC  5.0
VIN               2     0     PULSE  0  3.0  5N  2.5N  2.5N  10N  25N
.TRAN             1N    35N
.PROBE
.END
```

ABT HSPICE MODELS

```
* ABT Test Circuit
* ABTHS.CIR
* Advanced BiCMOS Logic
* Standard Logic Product Group, Philips Semiconductors
* 12/15/94
*************************************************************************
*
* To simulate a particular device, go to the section of the file under
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* required process model.  You may simulate only one device at a time.
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* inductances used in the subcircuit files use nominal values.  To more
* accurately simulate a particular device package, refer to the package
* inductance tables for a particular package type and substitute those
* values into the subcircuit file.
*
*************************************************************************
*
* These models represent only one data input and one output of a device.
* Other control inputs such as direction, clock, and output enables are
* not modeled.  Circuitry in between the input and output are also not
* included such as gates, latches, and intermediate buffers.  The result
* is that the model does not show the exact function of the device, and
* propagation delays may not match the published AC specifications in
* the datasheet.
*
*************************************************************************

*** Process and Subcircuit Models ***

* Nominal parameters
.INC C:\SPICE\ABT\ABTMODN.HSP
.INC C:\SPICE\ABT\ABTNOM.SUB

* Fast parameters
* .INC C:\SPICE\ABT\ABTMODF.HSP
* .INC C:\SPICE\ABT\ABTFAS.SUB


* Slow parameters
* .INC C:\SPICE\ABT\ABTMODS.HSP
* .INC C:\SPICE\ABT\ABTSLO.SUB
```

```
*** Start Running Circuit Model ***
* Parts with an "X" suffix are "-1" parts with the 30 ohm series
* termination resistors

* Part Type        In     Out    Vcc    Gnd    Subcircuit Name

* XABT125          2      4      99     0      BUFFER1
* XABT126          2      4      99     0      BUFFER1
* XABT240          2      4      99     0      INVBUFFER1
* XABT240X         2      4      99     0      INVBUFFER2
* XABT241          2      4      99     0      BUFFER2
* XABT244          2      4      99     0      BUFFER2
* XABT244X         2      4      99     0      BUFFER3
* XABT245          2      4      99     0      BUFFER2
* XABT245X         2      4      99     0      BUFFER4
* XABT273A         2      4      99     0      FLOP4
* XABT373A         2      4      99     0      FLOP4
* XABT374A         2      4      99     0      FLOP4
* XABT377          2      4      99     0      FLOP1
* XABT534          2      4      99     0      INVFLOP
* XABT540          2      4      99     0      INVBUFFER1
* XABT541          2      4      99     0      BUFFER2
* XABT543A         2      4      99     0      FLOP4
* XABT544          2      4      99     0      FLOP5
* XABT573          2      4      99     0      FLOP2
* XABT574          2      4      99     0      FLOP2
* XABT620          2      4      99     0      INVBUFFER1
* XABT623          2      4      99     0      BUFFER2
* XABT640          2      4      99     0      INVBUFFER1
* XABT646A         2      4      99     0      FLOP4
* XABT648          2      4      99     0      FLOP5
* XABT651          2      4      99     0      FLOP4
* XABT652A         2      4      99     0      FLOP4
* XABT657          2      4      99     0      BUFFER5
* XABT821          2      4      99     0      FLOP3
* XABT823          2      4      99     0      FLOP3
* XABT827          2      4      99     0      BUFFER5
* XABT833          2      4      99     0      BUFFER5
* XABT841          2      4      99     0      FLOP3
* XABT843          2      4      99     0      FLOP3
* XABT845          2      4      99     0      FLOP3
* XABT853          2      4      99     0      BUFFER5
* XABT861          2      4      99     0      BUFFER5
* XABT863          2      4      99     0      BUFFER5
* XABT899          2      4      99     0      FLOP6
* XABT2952         2      4      99     0      FLOP3
* XABT2953         2      4      99     0      FLOP5
* XABT5074         2      4      99     0      FLOP7
*** External Test Load ***
RL1    4          0      500
CL1    4          0      50PF
*****************************

VCC               99     0      DC  5.0
VIN               2      0      PULSE  0  3.0  5N  2.5N  2.5N  10N  25N
.TRAN             1N     35N
.PROBE
.END
```

ABT PSPICE MODELS

```
* ABT Test Circuit
* ABTPS.CIR
* Advanced BiCMOS Logic
* Standard Logic Product Group, Philips Semiconductors
* 12/15/94
*****************************************************************************
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* required process model.  You may simulate only one device at a time.
* The load circuit may be adapted to your specific situation.  Also, pin
* inductances used in the subcircuit files use nominal values.  To more
* accurately simulate a particular device package, refer to the package
* inductance tables for a particular package type and substitute those
* values into the subcircuit file.
*
*****************************************************************************
*
* These models represent only one data input and one output of a device.
* Other control inputs such as direction, clock, and output enables are
* not modeled.  Circuitry in between the input and output are also not
* included such as gates, latches, and intermediate buffers.  The result
* is that the model does not show the exact function of the device, and
* propagation delays may not match the published AC specifications in
* the datasheet.
*
*****************************************************************************

*** Process and Subcircuit Models ***

* Nominal parameters
.LIB C:\SPICE\ABT\ABTMODN.PSP
.LIB C:\SPICE\ABT\ABTNOM.SUB

* Fast parameters
* .LIB C:\SPICE\ABT\ABTMODF.PSP
* .LIB C:\SPICE\ABT\ABTFAS.SUB


* Slow parameters
* .LIB C:\SPICE\ABT\ABTMODS.PSP
* .LIB C:\SPICE\ABT\ABTSLO.SUB
```

```
*** Start Running Circuit Model ***
* Parts with an "X" suffix are "-1" parts with the 30 ohm series
* termination resistors

* Part Type        In     Out    Vcc    Gnd    Subcircuit Name

* XABT125          2      4      99     0      BUFFER1
* XABT126          2      4      99     0      BUFFER1
* XABT240          2      4      99     0      INVBUFFER1
* XABT240X         2      4      99     0      INVBUFFER2
* XABT241          2      4      99     0      BUFFER2
* XABT244          2      4      99     0      BUFFER2
* XABT244X         2      4      99     0      BUFFER3
* XABT245          2      4      99     0      BUFFER2
* XABT245X         2      4      99     0      BUFFER4
* XABT273A         2      4      99     0      FLOP4
* XABT373A         2      4      99     0      FLOP4
* XABT374A         2      4      99     0      FLOP4
* XABT377          2      4      99     0      FLOP1
* XABT534          2      4      99     0      INVFLOP
* XABT540          2      4      99     0      INVBUFFER1
* XABT541          2      4      99     0      BUFFER2
* XABT543A         2      4      99     0      FLOP4
* XABT544          2      4      99     0      FLOP5
* XABT573          2      4      99     0      FLOP2
* XABT574          2      4      99     0      FLOP2
* XABT620          2      4      99     0      INVBUFFER1
* XABT623          2      4      99     0      BUFFER2
* XABT640          2      4      99     0      INVBUFFER1
* XABT646A         2      4      99     0      FLOP4
* XABT648          2      4      99     0      FLOP5
* XABT651          2      4      99     0      FLOP4
* XABT652A         2      4      99     0      FLOP4
* XABT657          2      4      99     0      BUFFER5
* XABT821          2      4      99     0      FLOP3
* XABT823          2      4      99     0      FLOP3
* XABT827          2      4      99     0      BUFFER5
* XABT833          2      4      99     0      BUFFER5
* XABT841          2      4      99     0      FLOP3
* XABT843          2      4      99     0      FLOP3
* XABT845          2      4      99     0      FLOP3
* XABT853          2      4      99     0      BUFFER5
* XABT861          2      4      99     0      BUFFER5
* XABT863          2      4      99     0      BUFFER5
* XABT899          2      4      99     0      FLOP6
* XABT2952         2      4      99     0      FLOP3
* XABT2953         2      4      99     0      FLOP5
* XABT5074         2      4      99     0      FLOP7
*** External Test Load ***
RL1    4          0      500
CL1    4          0      50PF
*****************************

VCC               99     0      DC  5.0
VIN               2      0      PULSE  0  3.0  5N  2.5N  2.5N  10N  25N
.TRAN             1N     35N
.PROBE
.END
```

ABTNOM.SUB Subcircuit

```
*************************************************************
* ABT Subcircuit Library
* ABTNOM.SUB
* Nominal Process Corner
* Standard Logic Product Group
* Philips Semiconductors
* 12/15/94
*************************************************************
.SUBCKT BUFFER1 IN OUT VCC GND

*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90            10          ABTINAN

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTAN

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS BUFFER1
********************
.SUBCKT BUFFER2 IN OUT VCC GND

*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90           10          ABTINBN

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTCN

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS BUFFER2
********************
```

```
.SUBCKT BUFFER3 IN OUT VCC GND

*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90           10           ABTINBN

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTDN

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS BUFFER3
********************
.SUBCKT BUFFER4 IN OUT VCC GND

*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90           10           ABTINBN

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTLN

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS BUFFER4
********************
.SUBCKT BUFFER5 IN OUT VCC GND

*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90           10           ABTINBN

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTFN

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS BUFFER5
********************
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```
.SUBCKT INVBUFFER1 IN OUT VCC GND
*      IN     OUT    SUBVCC       SUBGND
XIN    20     30     90           10          ABTINAN

*      IN     OUT    SUBVCC       SUBGND
XINV   30     50     90           10          ABTINVAN

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTAN

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS INVBUFFER1
********************
.SUBCKT INVBUFFER2 IN OUT VCC GND
*      IN     OUT    SUBVCC       SUBGND
XIN    20     30     90           10          ABTINAN

*      IN     OUT    SUBVCC       SUBGND
XINV   30     50     90           10          ABTINVAN

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTBN

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS INVBUFFER2
********************
.SUBCKT FLOP1 IN OUT VCC GND
*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90           10          ABTINAN

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTEN

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS FLOP1
********************
```

```
.SUBCKT FLOP2 IN OUT VCC GND
*      IN     OUT    SUBVCC       SUBGND
XIN    20     30     90           10          ABTINAN

*      IN     OUT    SUBVCC       SUBGND
XINV   30     50     90           10          ABTINVAN

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTCN

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS FLOP2
********************
.SUBCKT FLOP3 IN OUT VCC GND
*      IN     OUT    SUBVCC       SUBGND
XIN    20     30     90           10          ABTINAN

*      IN     OUT    SUBVCC       SUBGND
XINV   30     50     90           10          ABTINVAN

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTFN

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS FLOP3
********************
.SUBCKT FLOP4 IN OUT VCC GND
*      IN     OUT    SUBVCC       SUBGND
XIN    20     30     90           10          ABTINAN

*      IN     OUT    SUBVCC       SUBGND
XINV   30     50     90           10          ABTINVAN

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTKN

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS FLOP4
********************
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```
.SUBCKT FLOP5 IN OUT VCC GND

*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90           10          ABTINAN

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTFN

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS FLOP5
********************
.SUBCKT FLOP6 IN OUT VCC GND

*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90           10          ABTINBN

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTKN

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS FLOP6
********************
.SUBCKT FLOP7 IN OUT VCC GND

*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90           10          ABTINCN

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTHN

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS FLOP7
********************
```

```
.SUBCKT INVFLOP IN OUT VCC GND

*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90           10          ABTINAN

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTCN

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS INVFLOP
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ABTFAS.SUB Subcircuit

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**************************************************************
* ABT Subcircuit Library
* ABTFAS.SUB
* Fast Process Corner
* Standard Logic Product Group
* Philips Semiconductors
* 12/15/94
**************************************************************
.SUBCKT BUFFER1 IN OUT VCC GND

*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90            10          ABTINAF

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTAF

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS BUFFER1
********************
.SUBCKT BUFFER2 IN OUT VCC GND

*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90           10          ABTINBF

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTCF

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS BUFFER2
********************
.SUBCKT BUFFER3 IN OUT VCC GND

*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90           10          ABTINBF

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTDF

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS BUFFER3
********************
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```
.SUBCKT BUFFER4 IN OUT VCC GND

*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90           10           ABTINBF

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTLF

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS BUFFER4
********************
.SUBCKT BUFFER5 IN OUT VCC GND

*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90           10           ABTINBF

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTFF

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS BUFFER5
********************
.SUBCKT INVBUFFER1 IN OUT VCC GND
*      IN     OUT    SUBVCC       SUBGND
XIN    20     30     90           10           ABTINAF

*      IN     OUT    SUBVCC       SUBGND
XINV   30     50     90           10           ABTINVAF

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTAF

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS INVBUFFER1
********************
```

```
.SUBCKT INVBUFFER2 IN OUT VCC GND
*      IN     OUT    SUBVCC       SUBGND
XIN    20     30     90           10          ABTINAF

*      IN     OUT    SUBVCC       SUBGND
XINV   30     50     90           10          ABTINVAF

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10    ABTOUTBF

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS INVBUFFER2
********************
.SUBCKT FLOP1 IN OUT VCC GND
*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90           10          ABTINAF

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10    ABTOUTEF

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS FLOP1
********************
.SUBCKT FLOP2 IN OUT VCC GND
*      IN     OUT    SUBVCC       SUBGND
XIN    20     30     90           10          ABTINAF

*      IN     OUT    SUBVCC       SUBGND
XINV   30     50     90           10          ABTINVAF

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10    ABTOUTCF

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS FLOP2
********************
```

```
.SUBCKT FLOP3 IN OUT VCC GND
*      IN     OUT    SUBVCC       SUBGND
XIN    20     30     90           10           ABTINAF

*      IN     OUT    SUBVCC       SUBGND
XINV   30     50     90           10           ABTINVAF

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTFF

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS FLOP3
********************
.SUBCKT FLOP4 IN OUT VCC GND
*      IN     OUT    SUBVCC       SUBGND
XIN    20     30     90           10           ABTINAF

*      IN     OUT    SUBVCC       SUBGND
XINV   30     50     90           10           ABTINVAF

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTKF

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS FLOP4
********************
.SUBCKT FLOP5 IN OUT VCC GND

*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90           10           ABTINAF

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTFF

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS FLOP5
********************
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```
.SUBCKT FLOP6 IN OUT VCC GND

*      IN     OUT    SUBVCC        SUBGND
XIN    20     50     90            10            ABTINBF

*      IN     OUT    OGND   SUBVCC        SUBGND
XOUT   50     40     10     90            10     ABTOUTKF

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS FLOP6
*********************
.SUBCKT FLOP7 IN OUT VCC GND

*      IN     OUT    SUBVCC        SUBGND
XIN    20     50     90            10            ABTINCF

*      IN     OUT    OGND   SUBVCC        SUBGND
XOUT   50     40     10     90            10     ABTOUTHF

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS FLOP7
*********************
.SUBCKT INVFLOP IN OUT VCC GND

*      IN     OUT    SUBVCC        SUBGND
XIN    20     50     90            10            ABTINAF

*      IN     OUT    OGND   SUBVCC        SUBGND
XOUT   50     40     10     90            10     ABTOUTCF

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS INVFLOP
*********************
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ABTSLO.SUB Subcircuit

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************************************************************
* ABT Subcircuit Library
* ABTSLO.SUB
* Slow Process Corner
* Standard Logic Product Group
* Philips Semiconductors
* 12/15/94
************************************************************
.SUBCKT BUFFER1 IN OUT VCC GND

*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90            10          ABTINAS

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTAS

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS BUFFER1
********************
.SUBCKT BUFFER2 IN OUT VCC GND

*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90           10          ABTINBS

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTCS

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS BUFFER2
********************
.SUBCKT BUFFER3 IN OUT VCC GND

*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90           10          ABTINBS

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTDS

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS BUFFER3
********************
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```
.SUBCKT BUFFER4 IN OUT VCC GND

*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90           10          ABTINBS

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTLS

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS BUFFER4
********************
.SUBCKT BUFFER5 IN OUT VCC GND

*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90           10          ABTINBS

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTFS

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS BUFFER5
********************
.SUBCKT INVBUFFER1 IN OUT VCC GND
*      IN     OUT    SUBVCC       SUBGND
XIN    20     30     90           10          ABTINAS

*      IN     OUT    SUBVCC       SUBGND
XINV   30     50     90           10          ABTINVAS

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTAS

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS INVBUFFER1
********************
```

```
.SUBCKT INVBUFFER2 IN OUT VCC GND
*      IN     OUT    SUBVCC       SUBGND
XIN    20     30     90           10          ABTINAS

*      IN     OUT    SUBVCC       SUBGND
XINV   30     50     90           10          ABTINVAS

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTBS

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS INVBUFFER2
********************
.SUBCKT FLOP1 IN OUT VCC GND
*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90           10          ABTINAS

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTES

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS FLOP1
********************
.SUBCKT FLOP2 IN OUT VCC GND
*      IN     OUT    SUBVCC       SUBGND
XIN    20     30     90           10          ABTINAS

*      IN     OUT    SUBVCC       SUBGND
XINV   30     50     90           10          ABTINVAS

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTCS

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS FLOP2
********************
```

```
.SUBCKT FLOP3 IN OUT VCC GND
*      IN     OUT    SUBVCC       SUBGND
XIN    20     30     90           10          ABTINAS

*      IN     OUT    SUBVCC       SUBGND
XINV   30     50     90           10          ABTINVAS

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10    ABTOUTFS

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS FLOP3
********************
.SUBCKT FLOP4 IN OUT VCC GND
*      IN     OUT    SUBVCC       SUBGND
XIN    20     30     90           10          ABTINAS

*      IN     OUT    SUBVCC       SUBGND
XINV   30     50     90           10          ABTINVAS

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10    ABTOUTKS

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS FLOP4
********************
.SUBCKT FLOP5 IN OUT VCC GND

*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90           10          ABTINAS

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10    ABTOUTFS

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS FLOP5
********************
```

```
.SUBCKT FLOP6 IN OUT VCC GND

*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90           10          ABTINBS

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTKS

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS FLOP6
********************
.SUBCKT FLOP7 IN OUT VCC GND

*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90           10          ABTINCS

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTHS

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS FLOP7
********************
.SUBCKT INVFLOP IN OUT VCC GND

*      IN     OUT    SUBVCC       SUBGND
XIN    20     50     90           10          ABTINAS

*      IN     OUT    OGND   SUBVCC       SUBGND
XOUT   50     40     10     90           10     ABTOUTCS

L1   IN    20   6.87NH
C1   20   GND   1.5PF
L2   VCC   90   6.87NH
C2   90   GND   1.5PF
L3   10   GND   6.87NH
C3   10   GND   1.5PF
L4   40   OUT   6.87NH
C4   40   GND   1.5PF
.ENDS INVFLOP
********************
```

Section 3
ABT16

SPICE

CONTENTS

Each ABT16 device requires some combination of an input stage, an output stage, possibly an inverting stage, and some package parasitics. Some part types are complete, with no combination of stages. Table 3-1 shows ABT16 model combinations that correlate input, inverting, and output structures for each part type.

Table 3-1. ABT16 Model Combinations

ABT16	Input Circuit	Inverter Circuit	Output Circuit	Inverting Output	Subcircuit Name
240	INBUFF	MOSINV	OUTBUFF	Yes	INV1
240–1	INBUFF	MOSINV	OUTBUF1	Yes	INV_1
244A	–	–	–	No	A16244
244–1	–	–	–	No	A16244_1
245B	–	–	–	No	A16245
245A–1	–	–	–	No	A16245_1
273A	INBUFF	INBUFF	OUTBUFF	No	NINV
373B	INBUFF	INBUFF	OUTBUFF	No	NINV
374B	INBUFF	INBUFF	OUTBUFF	No	NINV
500	INBUFF	INBUFF	OUTBUFF	No	NINVB
501	INBUFF	INBUFF	OUTBUFF	No	NINVB
541	INBUFF	INBUFF	OUTBUFF	No	NINV
543	INBUFF	INBUFF	OUTBUFF	No	NINVB
646	INBUFF	INBUFF	OUTBUFF	No	NINVB
652	INBUFF	INBUFF	OUTBUFF	No	NINVB
821	INBUFF	INBUFF	OUTBUFF	No	NINV
823	INBUFF	INBUFF	OUTBUFF	No	NINV
825	INBUFF	INBUFF	OUTBUFF	No	NINV
827	INBUFF	INBUFF	OUTBUFF	No	NINV
841	INBUFF	INBUFF	OUTBUFF	No	NINV
899	INBUFF	INBUFF	OUTBUFF	No	NINVB
952	INBUFF	INBUFF	OUTBUFF	No	NINVB
1543	INBUFF	INBUFF	OUTBUFF	No	NINVB

The data sheet section provides information on each ABT16 part type. Each data sheet contains a part description, part features, quick reference data, ordering information, pin configuration, logic symbol or diagram, and function table.

To do simulations on a particular part type, refer to the ABT16 Netlists section of the book. That section contains files called "ABT16XX.CIR" and "ABT16XXX.CIR" that are simulation test circuits for individual device types. The files are also in the ABT16 directory in the attached diskette. The "XX" in ABT16XX.CIR refers to PS or HS for the PSPICE, and HSPICE protocols. The "XXX" in ABT16XXX.CIR refers to BSH or BSP for Berkeley SPICE programs that can be run in HSPICE or PSPICE. Figure 3-1 shows how the test circuit is assembled.

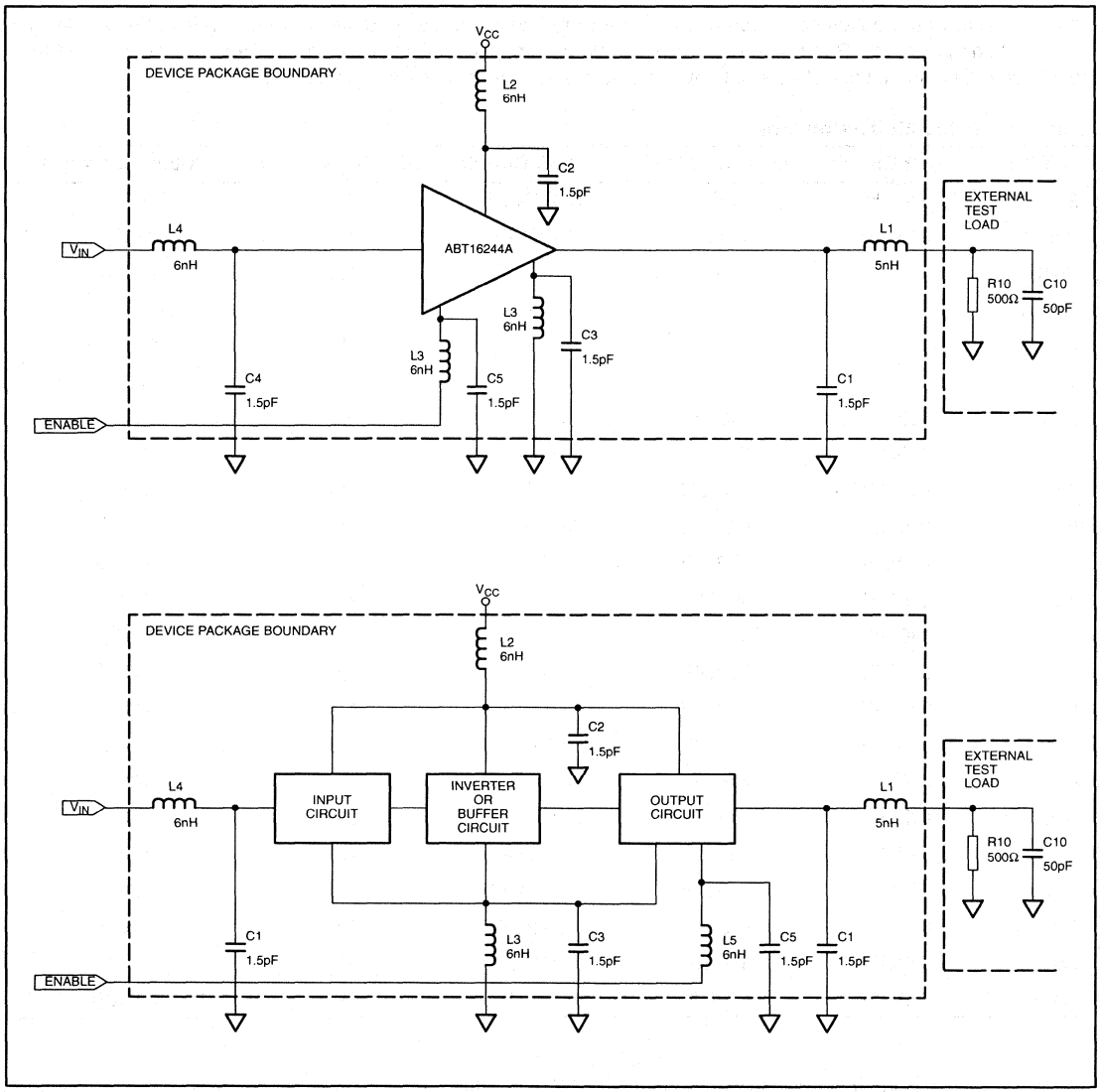


Figure 3-1. Examples of ABT16 Test Circuits

Netlists for subcircuits are in the ABT16 directory of the attached diskette and in the ABT16 Netlists section of the book. The subcircuit files are called A16XXXYY.LIB. The "XXX" in A16XXX refers to NOM, FAS, and SLO which represent the nominal, fast, and slow process corners. The "YY" refers to BS, HS, or PS for the Berkeley SPICE, HSPICE, and PSPICE protocols. The files contain the building blocks for the input, inverter, and output stages and also include package parasitic values which simulate a die in a package. These values can be changed to suit the package being used. Refer to the packaging section of the book.

The libraries for transistors, diodes, and other primitive elements are included in the attached diskette in the ABT16 directory and are not printed in the book since they are large files. They are called "A16MDLXX.LIB". The "XX" in A16MODXX refers to BS, HS, or PS for the Berkeley SPICE, HSPICE, and PSPICE protocols. Each of the three files contains the process parameters for nominal, fast, and slow process corners.

Values for package parasitics may be changed for the particular application. These values are listed in the packaging section of the book for each package type.

The following illustration shows how the three programs interact with each other:

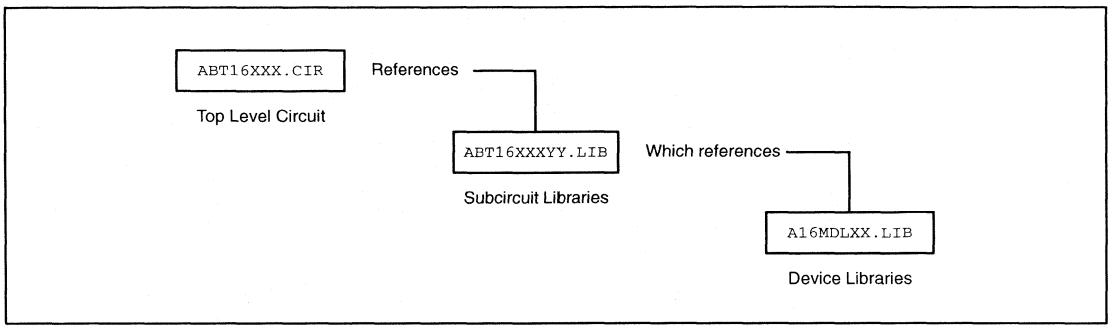


Figure 3-2. ABT16 SPICE Program Hierarchy

The top level program, ABT16XX.CIR, uses standard AC test conditions with a square wave input of 3V, rise and fall times of 2.5ns, V_{CC} of 5V, but a period of 25ns. These conditions may be modified to suit the application. Also, the ".INC" and ".LIB" commands which specify the path to reference the other two programs should be modified to reflect your disk directory structure.

ABT16 Short-form Datasheets

16-bit buffer/line driver (3-State) 74ABT16244A

FEATURES

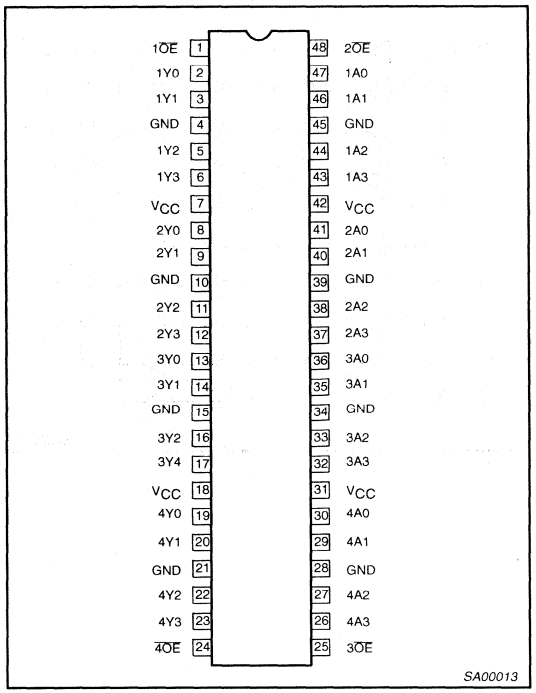
- 16-bit bus interface
- Multiple V_{CC} and GND pins minimize switching noise
- Power-up 3-State
- 3-State buffers
- Output capability: +64 mA/–32mA
- Live insertion/extraction permitted
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT16244A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16244A device is a 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$), each controlling four of the 3-State outputs.

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43 41, 40, 38, 37 36, 35, 33, 32 30, 29, 27, 26	1A0 – 1A3, 2A0 – 2A3, 3A0 – 3A3, 4A0 – 4A3	Data inputs
2, 3, 5, 6 8, 9, 11, 12 13, 14, 16, 17 19, 20, 22, 23	1Y0 – 1Y3, 2Y0 – 2Y3, 3Y0 – 3Y3, 4Y0 – 4Y3	Data outputs
1, 48 25, 24	$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	Output enables
4, 10, 15, 21 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

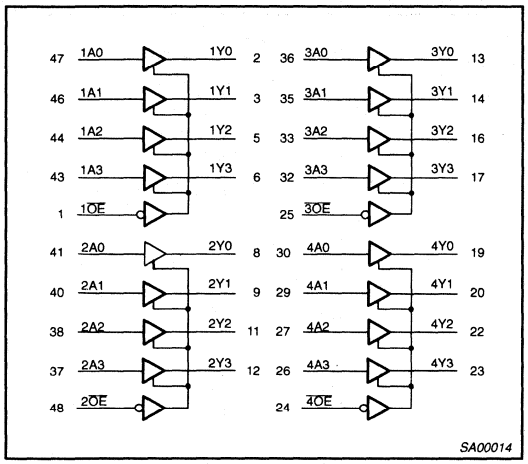
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 5V	1.7 2.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	500	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-pin SSOP Type III	–40°C to +85°C	BT16244A DL	SOT370-1
48-pin TSSOP Type II	–40°C to +85°C	BT16244A DGG	SOT362-1

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS
$n\overline{OE}$	nAx	nYx
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance "off" state

16-bit buffer/line driver with 30Ω series termination resistors (3-State)

74ABT16244-1

FEATURES

- 16-bit bus interface
- Multiple V_{CC} and GND pins minimize switching noise
- Power-up 3-State
- 3-State buffers
- Output capability: +12 mA/–32mA
- Live insertion/extraction permitted
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

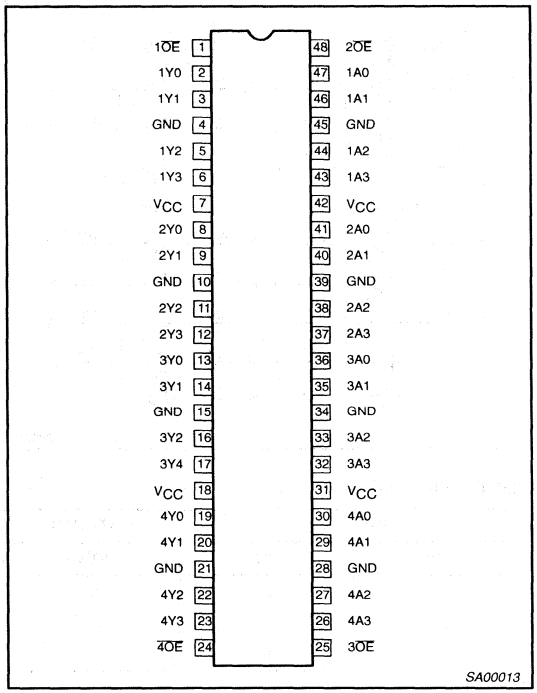
DESCRIPTION

The 74ABT16244-1 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed.

The 74ABT16244-1 device is a 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables (1$\overline{OE}$, 2$\overline{OE}$, 3$\overline{OE}$, 4$\overline{OE}$), each controlling four of the 3-State outputs.

The 74ABT16244-1 is designed with 30Ω series resistance in both the upper and lower output structures. This design reduces line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters.

PIN CONFIGURATION



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 5V	3.2	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	500	µA

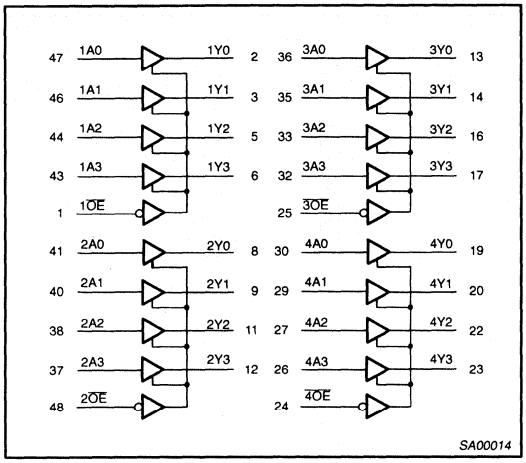
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-pin SSOP Type III	–40°C to +85°C	BT16244–1 DL	SOT370-1
48-pin TSSOP Type II	–40°C to +85°C	BT16244-1 DGG	SOT362-1

16-bit buffer/line driver with 30Ω series termination resistors (3-State)

74ABT16244-1

LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43 41, 40, 38, 37 36, 35, 33, 32 30, 29, 27, 26	1A0 – 1A3, 2A0 – 2A3, 3A0 – 3A3, 4A0 – 4A3	Data inputs
2, 3, 5, 6 8, 9, 11, 12 13, 14, 16, 17 19, 20, 22, 23	1Y0 – 1Y3, 2Y0 – 2Y3, 3Y0 – 3Y3, 4Y0 – 4Y3	Data outputs
1, 48 25, 24	$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	Output enables
4, 10, 15, 21 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUTS
$n\overline{OE}$	nAx	nYx
L	L	L
L	H	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

16-Bit bus transceiver (3-State) 74ABT16245B

FEATURES

- 16-bit bidirectional bus interface
- Power-up 3-State
- Multiple V_{CC} and GND pins minimize switching noise
- 3-State buffers
- Output capability: +64 mA/–32mA
- Latch–up protection exceeds 500mA per Jedec JC40.2 Std 17
- Live insertion/extraction permitted
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16245B high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16245B device is a dual octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features two Output Enable ($1\overline{OE}$, $2\overline{OE}$) inputs for easy cascading and two Direction (1DIR, 2DIR) inputs for direction control.

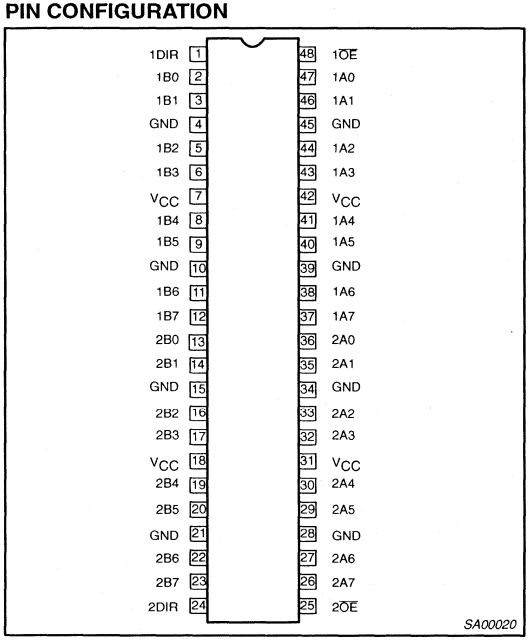
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF; V_{CC} = 5V	2.0 2.3	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O pin capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	500	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-pin SSOP Type III	–40°C to +85°C	BT16245BDL	SOT370-1
48-pin TSSOP Type II	–40°C to +85°C	BT16245DGG	SOT362-1

PIN CONFIGURATION



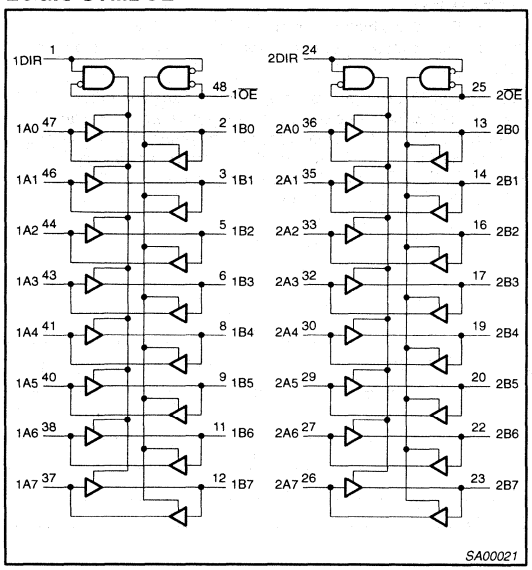
PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
1DIR, 2DIR	1, 24	Direction control inputs (Active-High)
1A0 – 1A7, 2A0 – 2A7	47, 46, 44, 43 41, 40, 38, 37 36, 35, 33, 32 30, 29, 27, 26	Data inputs/outputs (A side)
1B0 – 1B7 2B0 – 2B7	2, 3, 5, 6 8, 9, 11, 12 13, 14, 16, 17 19, 20, 22, 23	Data inputs/outputs (B side)
$1\overline{OE}$, $2\overline{OE}$	48, 25	Output enables
GND	4, 10, 15, 21 28, 34, 39, 45	Ground (0V)
V_{CC}	7, 18, 31, 42	Positive supply voltage

16-Bit bus transceiver (3-State)

74ABT16245B

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$n\overline{OE}$	nDIR	nAx	nBx
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance "off" state

16-Bit bus transceiver with 30Ω series termination (3-State)

74ABT16245A-1

FEATURES

- 16-bit bidirectional bus interface
- Power-up 3-State
- Multiple V_{CC} and GND pins minimize switching noise
- 3-State buffers
- Output capability: +12mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16245A-1 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed.

The 74ABT16245A-1 device is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features two Output Enable ($1\overline{OE}$, $2\overline{OE}$) inputs for easy cascading and two Direction (1DIR, 2DIR) inputs for direction control.

The 74ABT16245A-1 is designed with 30 ohm series resistance in both the upper and lower output structures on both A and B ports. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receiver/transmitters.

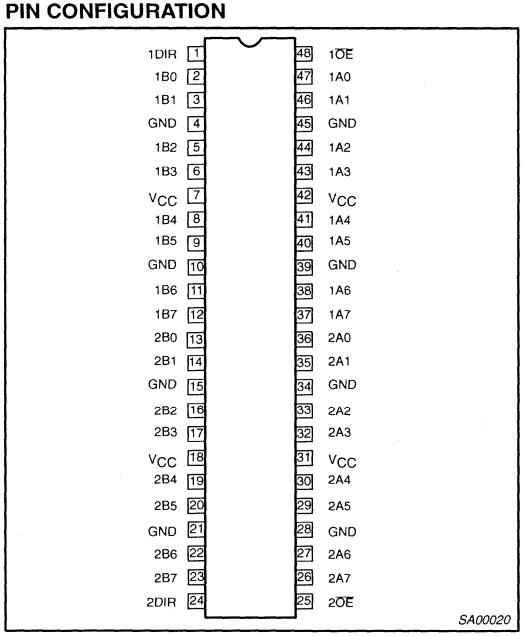
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF; V_{CC} = 5V	2.0 3.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
$C_{I/O}$	I/O pin capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-pin SSOP Type III	–40°C to +85°C	BT16245A-1 DL	SOT370-1
48-pin TSSOP Type II	–40°C to +85°C	BT16245A-1 DGG	SOT362-1

PIN CONFIGURATION

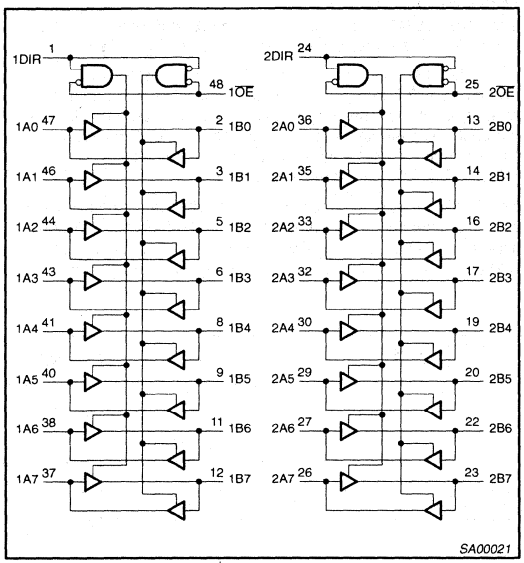


PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
1DIR, 2DIR	1, 24	Direction control inputs (Active-High)
1A0 – 1A7, 2A0 – 2A7	47, 46, 44, 43 41, 40, 38, 37 36, 35, 33, 32 30, 29, 27, 26	Data inputs/outputs (A side)
1B0 – 1B7 2B0 – 2B7	2, 3, 5, 6 8, 9, 11, 12 13, 14, 16, 17 19, 20, 22, 23	Data inputs/outputs (B side)
$1\overline{OE}$, $2\overline{OE}$	48, 25	Output enables
GND	4, 10, 15, 21 28, 34, 39, 45	Ground (0V)
V_{CC}	7, 18, 31, 42	Positive supply voltage

16-Bit bus transceiver with 30Ω series termination (3-State) 74ABT16245A-1

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$n\overline{OE}$	nDIR	nAx	nBx
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance "off" state

16-bit D-type flip-flop | 74ABT16273

FEATURES

- 16-bit D-type edge triggered flip-flops
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

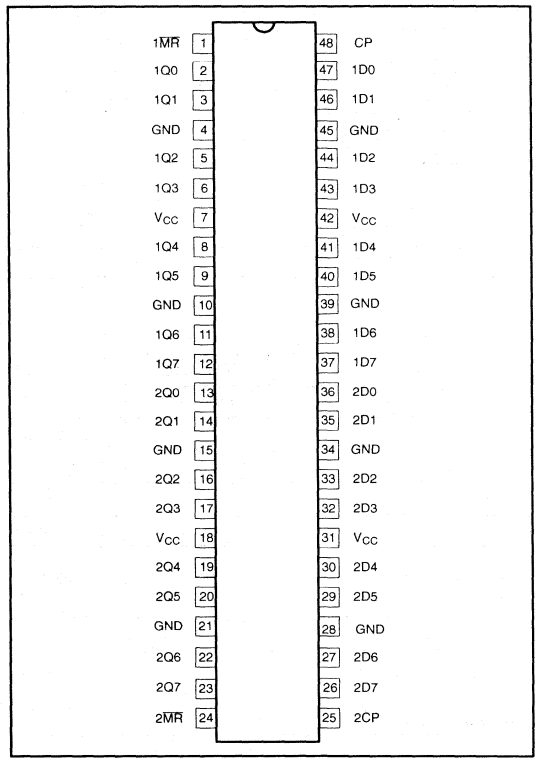
DESCRIPTION

The 74ABT16273 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

This part is a 16-bit edge triggered D-type flip-flop with non-inverting high drive outputs. This device can be used as two 8-bit flip-flops or one 16-bit flip-flop. When the clock (CP) goes High, the data on the D inputs is stored and the Q outputs display the stored data.

This device also features a master reset ($\overline{MR}$) that resets all flip-flops to the Low state when $\overline{MR}$ is set to the Low state.

PIN CONFIGURATION



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5.0V	2.5 2.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
I_{CCH}	Quiescent supply current	Outputs High; V_{CC} = 5.5V	200	mA
I_{CCL}		Outputs Low; V_{CC} = 5.5V	8	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic Shrink Small Outline (SSOP) Type III	–40°C to +85°C	BT16273ADL	SOT370-1
48-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	BT16273ADGG	SOT362-1

PIN DESCRIPTION

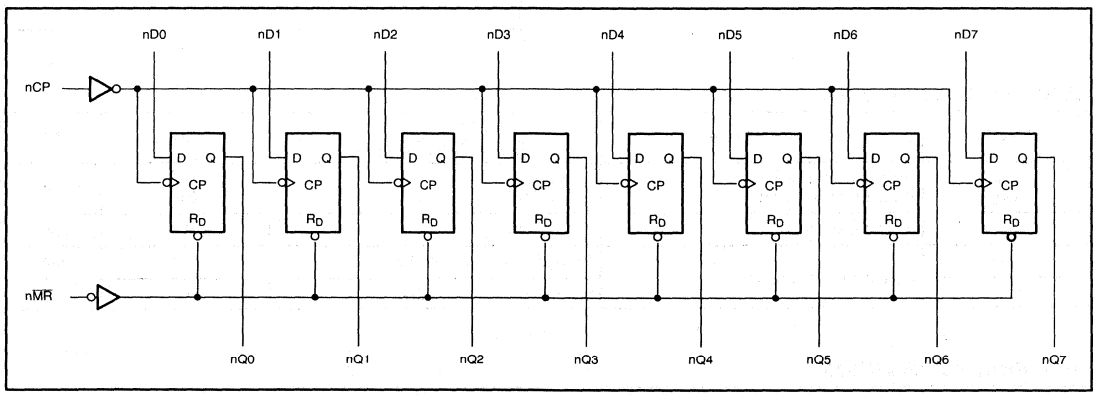
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 24	$1\overline{MR}$, $2\overline{MR}$	Master reset input (active-Low)
2, 3, 5, 6, 8, 9, 11, 12,13, 14, 16, 17, 19, 20, 22, 23	1Q0-1Q7 2Q0-2Q7	Data outputs
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1D0-1D7 2D0-2D-7	Data inputs
25, 48	1CP, 2CP	Clock pulse input (active rising edge)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

FUNCTION TABLE

Inputs			Outputs	operating mode
$n\overline{MR}$	nCP	nDX	nQ0-nQ7	
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"
H	L	X	Q_0	Retain state

H = High voltage level
h = high voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
Q_0 = Output as it was

LOGIC DIAGRAM



16-bit transparent latch (3-State)

74ABT16373B
74ABTH16373B

FEATURES

- 16-bit transparent latch
- Multiple V_{CC} and GND pins minimize switching noise
- Power-up 3-State
- Live insertion/extraction permitted
- Power-up reset
- 3-State output buffers
- 74ABTH16373B incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64mA/–32mA
- I_{CCL} –19 mA maximum
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16373B high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16373B device is a dual octal transparent latch coupled to two sets of eight 3-State output buffers. The two sections of the device are controlled independently by Enable (nE) and Output Enable ($n\overline{OE}$) control gates.

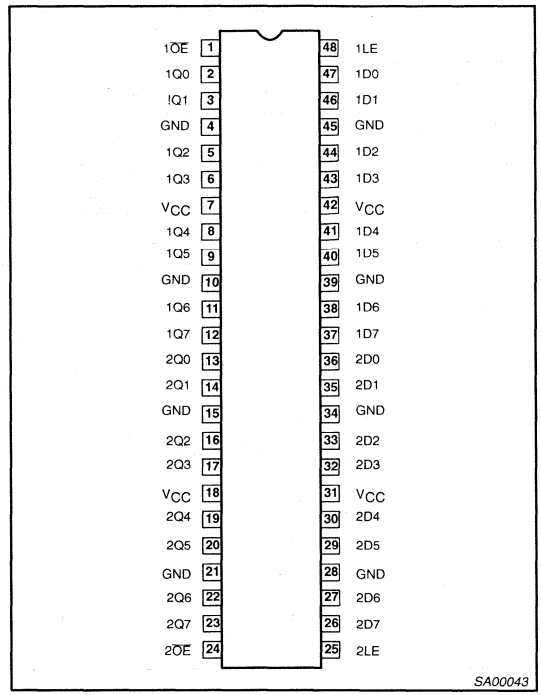
The data on each set of D inputs are transferred to the latch outputs when the Latch Enable (nE) input is High. The latch remains transparent to the data inputs while nE is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. Each active-Low Output Enable ($n\overline{OE}$) controls eight 3-State buffers independent of the latch operation.

When $n\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $n\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

Two options are available, 74ABT16373B which does not have the bus-hold feature and 74ABTH16373B which incorporates the bus-hold feature.

PIN CONFIGURATION



SA00043

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	500	nA

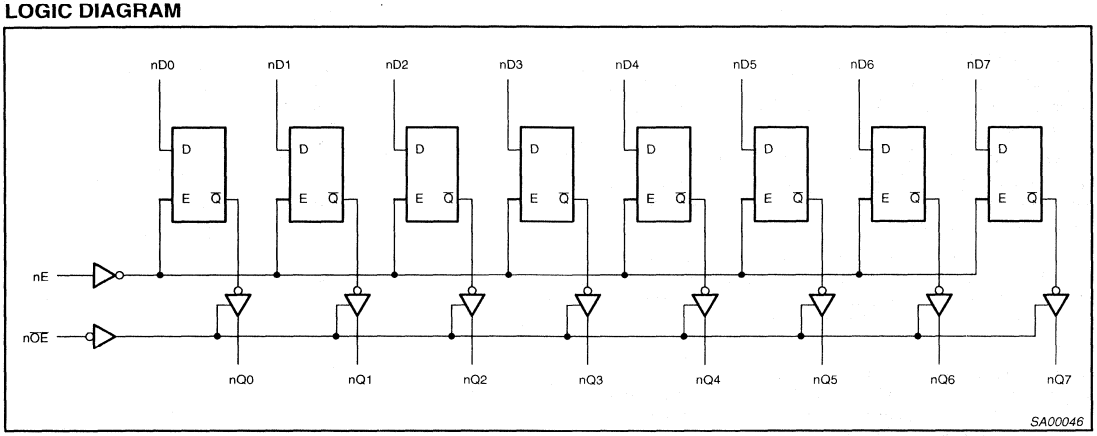
ORDERING INFORMATION

PACKAGES	PART NUMBER	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-pin SSOP type III	74ABT16373B	–40°C to +85°C	BT16373B DL	SOT370-1
48-pin TSSOP type II	74ABT16373B	–40°C to +85°C	BT16373B DGG	SOT362-1
48-pin SSOP type III	74ABTH16373B	–40°C to +85°C	BH16373B DL	SOT370-1
48-pin TSSOP type II	74ABTH16373B	–40°C to +85°C	BH16373B DGG	SOT362-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1D0 – 1D7 2D0 – 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Q0 – 1Q7 2Q0 – 2Q7	Data outputs
1, 24	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
48, 25	1E, 2E	Enable inputs (active-High)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$n\overline{OE}$	nE	nDx		nQ0 – nQ7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	i h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

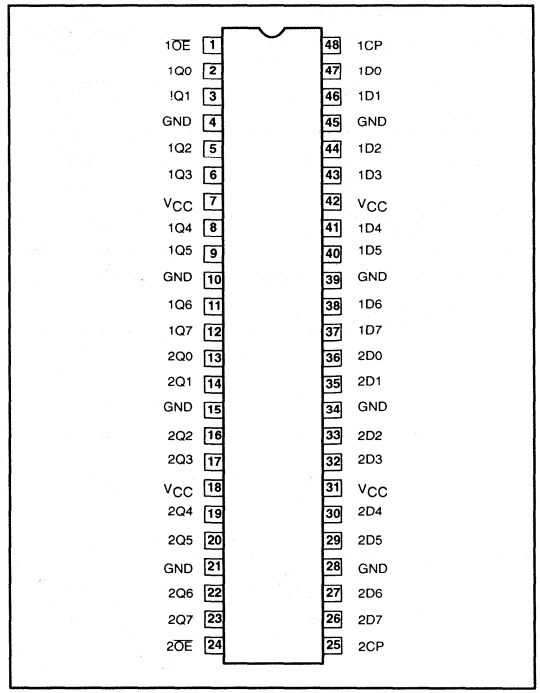
Dual octal D-type flip-flop; positive-edge trigger (3-State)

74ABT16374B

FEATURES

- Two 8-bit positive edge triggered registers
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Multiple V_{CC} and GND pins minimize switching noise
- 3-State output buffers
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

PIN CONFIGURATION



DESCRIPTION

The 74ABT16374B high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16374B has two 8-bit, edge triggered registers, with each register coupled to eight 3-State output buffers. The two sections of each register are controlled independently by the clock (nCP) and Output Enable ($n\overline{OE}$) control gates.

Each register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. Each active-Low Output Enable ($n\overline{OE}$) controls all eight 3-State buffers for its register independent of the clock operation.

When $n\overline{OE}$ is Low, the stored data appears at the outputs for that register. When $n\overline{OE}$ is High, the outputs for that register are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	C_L = 50pF; V_{CC} = 5V	3.6	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	120	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-pin plastic SSOP	–40°C to +85°C	BT16374B DL	SOT370-1
48-pin plastic TSSOP	–40°C to +85°C	BT16374B DGG	SOT362-1

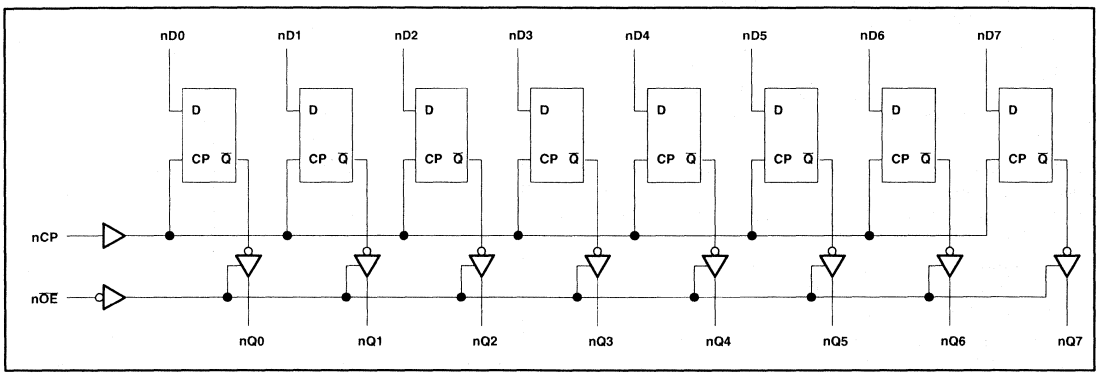
Dual octal D-type flip-flop; positive-edge trigger (3-State)

74ABT16374B

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37 36, 35, 33, 32, 30, 29, 27, 26	1D0 – 1D7 2D0 – 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12 13, 14, 16, 17, 19, 20, 22, 23	1Q0 – 1Q7 2Q0 – 2Q7	Data outputs
1, 24	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
48, 25	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$n\overline{OE}$	nCP	nDx		nQ0 – nQ7	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↥	X	NC	NC	Hold
H H	↥ ↑	X nDx	NC nDx	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↥ = Not a Low-to-High clock transition

18-bit universal bus transceiver (3-State) 74ABT16501A

FEATURES

- 18-bit bidirectional bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Negative edge-triggered clock inputs
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- Positive edge-triggered clock inputs
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

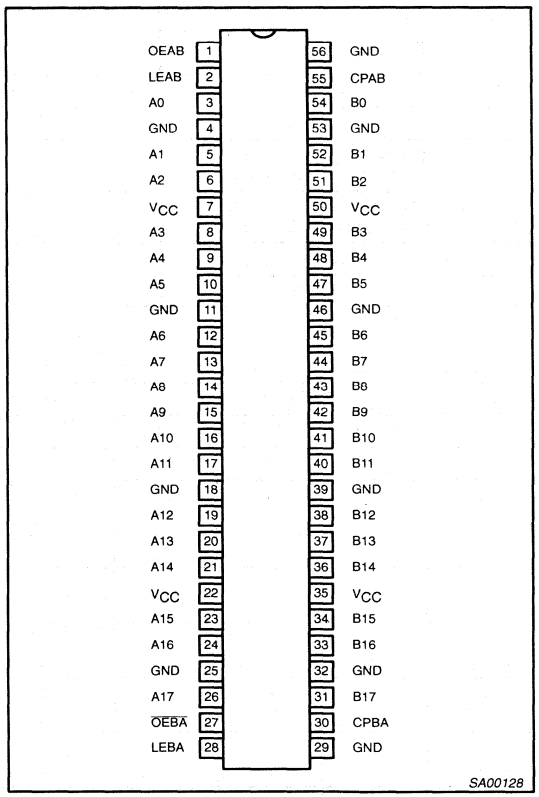
The 74ABT16501A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable (OEAB and $\overline{\text{OEBA}}$), latch enable (LEAB and LEBA), and clock (CPAB and CPBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is High. When LEAB is Low, the A data is latched if CPAB is held at a High or Low logic level. If EAB is Low, the A-bus data is stored in the latch/flip-flop on the Low-to-High transition of CPAB. When OEAB is High, the outputs are active. When OEAB is Low, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{\text{OEBA}}$, LEBA and CPBA. The output enables are complimentary (OEAB is active High, and $\overline{\text{OEBA}}$ is active Low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

PIN CONFIGURATION



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	2.2 1.8	ns
C_{IN}	Input capacitance (Control pins)	V_I = 0V or V_{CC}	3	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or V_{CC}	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5V	500	µA
I_{CCL}		Outputs low; V_{CC} = 5.5V	9	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-Pin Plastic Shrink Small Outline (SSOP) Type III	–40°C to +85°C	BT16501ADL	SOT371-1
56-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	BT16501ADGG	SOT364-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	A-to-B Output enable input
27	$\overline{OEBA}$	B-to-A Output enable input (active low)
2, 28	LEAB/LEBA	A-to-B/B-to-A Latch enable input
55,30	CPAB/CPBA	A-to-B/B-to-A Clock input (active rising edge)
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0-A17	Data inputs/outputs (A side)
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0-B17	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

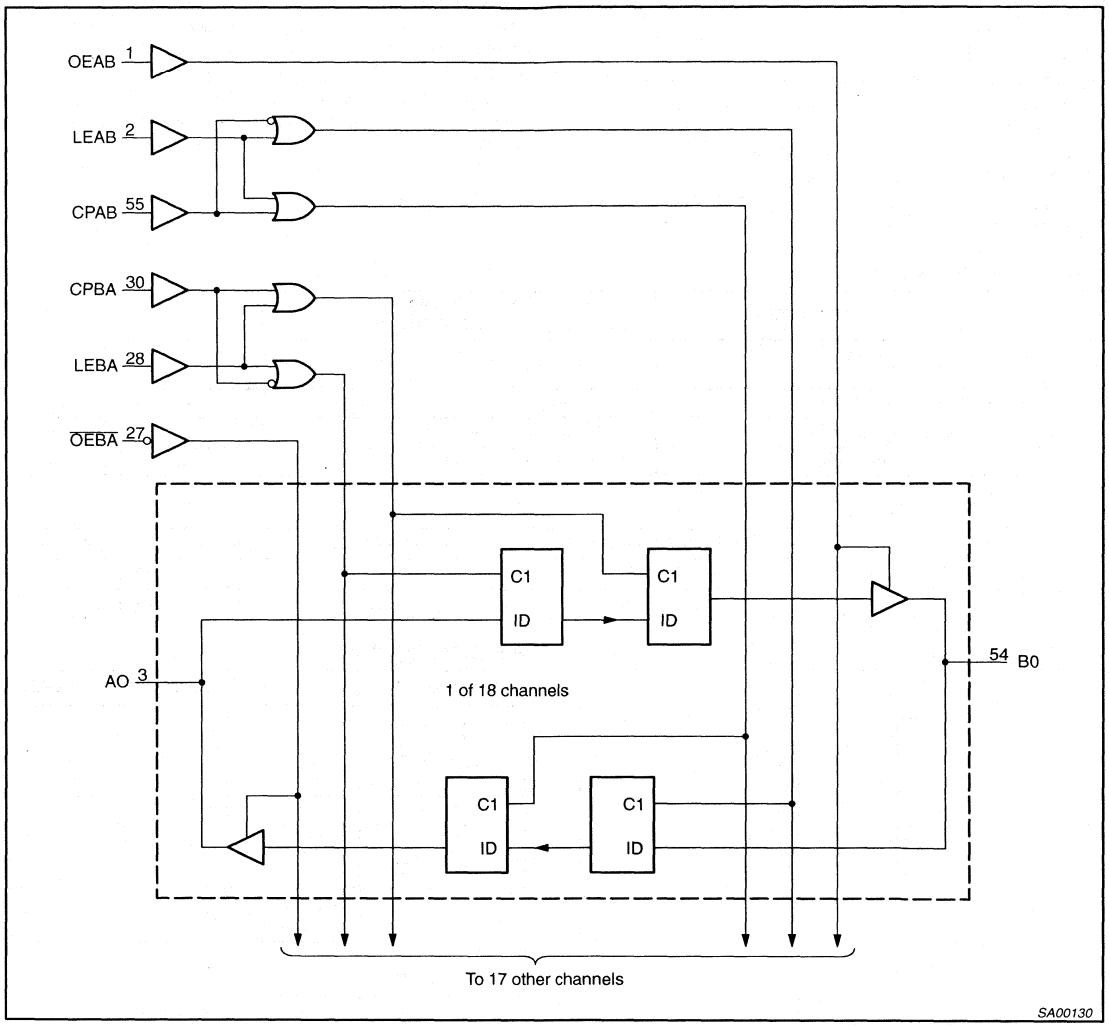
FUNCTION TABLE

INPUTS				Internal Registers	OUTPUTS	OPERATING MODE
OEAB	LEAB	CPAB	An		Bn	
L	H	X	X	X	Z	Disabled
L L	↓ ↓	X X	h l	H L	Z Z	Disabled, Latch data
L	L	H or L	X	NC	Z	Disabled, Hold data
L L	L L	↑ ↑	h l	H L	Z Z	Disabled, Clock data
H H	H H	X X	H L	H L	H L	Transparent
H H	↓ ↓	X X	h l	H L	H L	Latch data & display
H H	L L	↑ ↑	h l	H L	H L	Clock data & display
H H	L L	H or L H or L	X X	H L	H L	Hold data & display

NOTE: A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and CPBA.

H = High voltage level
h = High voltage level one set-up time prior to the Enable or Clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Enable or Clock transition
NC= No Change
X = Don't care
Z = High Impedance "off" state
↓ = High-to-Low Enable or Clock transition

LOGIC DIAGRAM



16-bit buffer/line driver (3-State) 74ABT16541

FEATURES

- Two 8-bit bus interfaces
- Power-up 3-State
- Multiple V_{CC} and GND pins minimize switching noise
- Provides ideal interface and increases fan-out of MOS Microprocessors
- 3-State buffers sink 64mA and source 32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT16541 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16541 has two octal buffers that are ideal for driving bus lines. The outputs are all capable of sinking 64mA and sourcing 32mA.

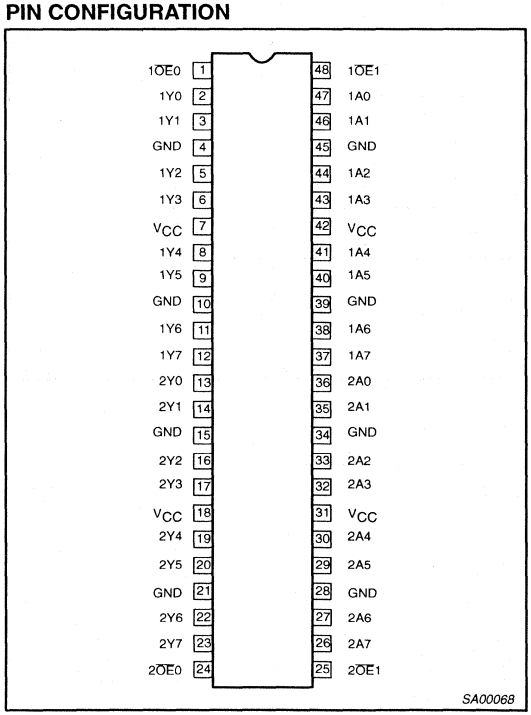
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nIx to nYx	C_L = 50pF; V_{CC} = 5V	3.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	50	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-pin SSOP Type III	–40°C to +85°C	BT16541DL	SOT370-1
48-pin TSSOP Type II	–40°C to +85°C	BT16541DGG	SOT362-1

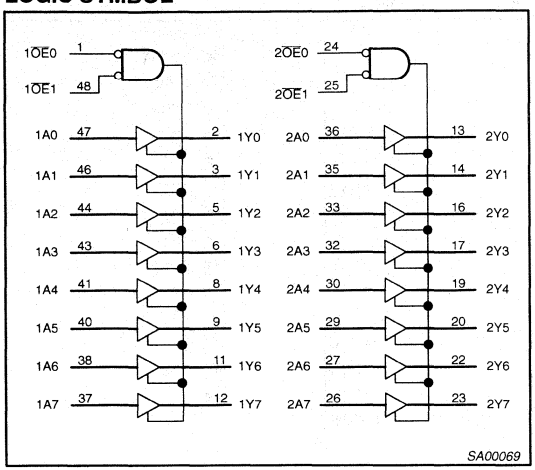
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0 - 1A7 2A0 - 2A7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17 19, 20, 22, 23	1Y0 - 1Y7, 2Y0 - 2Y7	Data outputs
1, 48 24, 25	$1\overline{OE}0$, $1\overline{OE}1$, $2\overline{OE}0$, $2\overline{OE}1$	Output enables
4, 10, 15, 21 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUTS			OUTPUTS
$n\overline{OE0}$	$n\overline{OE1}$	nIx	nYx
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance "off" state

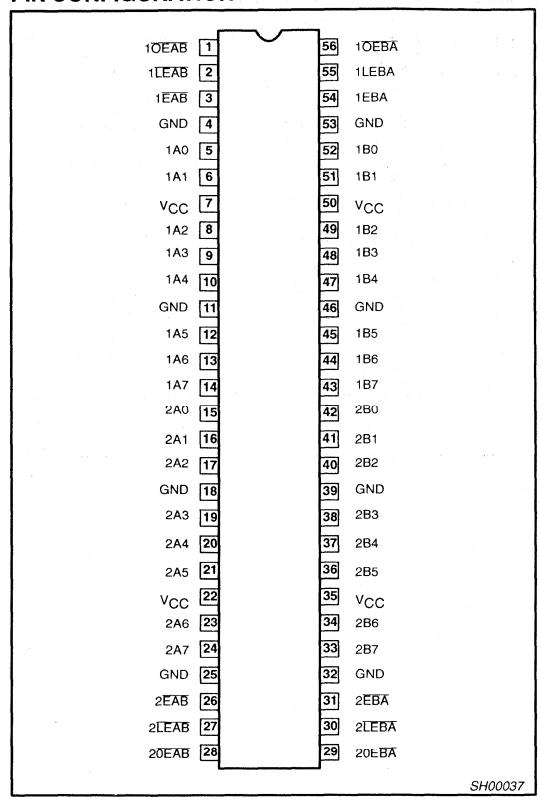
16-bit octal latched transceivers with dual enable (3-State)

74ABT16543

FEATURES

- Two 8-bit octal transceivers with D–type latch
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Multiple V_{CC} and GND pins minimize switching noise
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

PIN CONFIGURATION



DESCRIPTION

The 74ABT16543 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16543 dual octal registered transceiver contains two sets of D–type latches for temporary storage of data flowing in either direction. Separate Latch Enable (n$\overline{\text{LEAB}}$, n$\overline{\text{LEBA}}$) and Output Enable (n$\overline{\text{OEAB}}$, n$\overline{\text{OEBA}}$) inputs are provided for each register to permit independent control of data transfer in either direction. The outputs are guaranteed to sink 64mA.

FUNCTIONAL DESCRIPTION

The 74ABT16543 contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable (n$\overline{\text{EAB}}$) input and the A-to-B Latch Enable (n$\overline{\text{LEAB}}$) input are Low the A-to-B path is transparent.

A subsequent Low-to-High transition of the n$\overline{\text{LEAB}}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{\text{EAB}}$ and n$\overline{\text{OEAB}}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the n$\overline{\text{EBA}}$, n$\overline{\text{LEBA}}$, and n$\overline{\text{OEBA}}$ inputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx	C_L = 50pF; V_{CC} = 5V	2.5 2.2	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
$C_{I/O}$	I/O capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	550	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-pin plastic SSOP Type I	–40°C to +85°C	BT16543DL	SOT371-1
56-pin plastic TSSOP Type II	–40°C to +85°C	BT16543DGG	SOT364-1

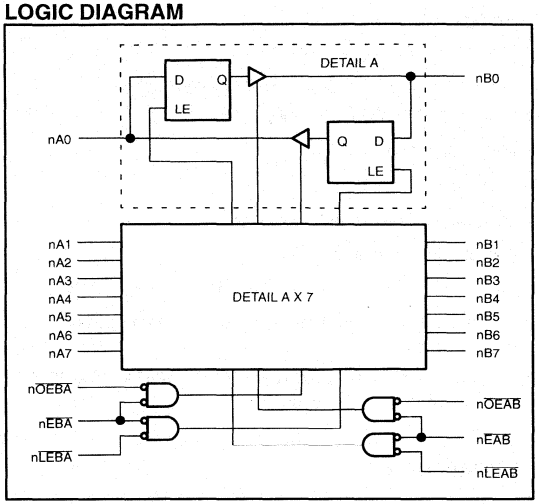
16-bit octal latched transceivers with dual enable (3-State)

74ABT16543

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40,38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	Data inputs/outputs
1, 56 28, 29	$1\overline{OEAB}$, $1\overline{OEBA}$, $2\overline{OEAB}$, $2\overline{OEBA}$	A to B / B to A Output Enable inputs (active-Low)
3, 54 26, 31	$1\overline{EAB}$, $1\overline{EBA}$, $2\overline{EAB}$, $2\overline{EBA}$	A to B / B to A Enable inputs (active-Low)
2, 55 27, 30	$1\overline{LEAB}$, $1\overline{LEBA}$, $2\overline{LEAB}$, $2\overline{LEBA}$	A to B / B to A Latch Enable inputs (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$n\overline{OEXX}$	$n\overline{EXX}$	$n\overline{LEXX}$	nAx or nBx	nBx or nAx	
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	H L	Latch + Display
L L	L L	L L	H L	H L	Transparent
L	L	H	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High transition of $n\overline{LEXX}$ or $n\overline{EXX}$ (XX = AB or BA)
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High transition of $n\overline{LEXX}$ or $n\overline{EXX}$ (XX = AB or BA)
X = Don't care
↑ = Low-to-High transition of $n\overline{LEXX}$ or $n\overline{EXX}$ (XX = AB or BA)
NC= No change
Z = High impedance or "off" state

16-bit bus transceiver/register (3-State) 74ABT16646

FEATURES

- Independent registers for A and B buses
- Multiple Vcc and GND pins minimize switching noise
- Live insertion/extraction permitted
- Power–up 3-State
- Power–up reset
- Multiplexed real-time and stored data
- Outputs sink 64mA and source 32mA
- Latch–up protection exceeds 500mA per Jedec JC40.2 Std 17
- Bus hold data inputs eliminate the need for external pull-up to hold unused inputs
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16646 high–performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16646 16-bit transceiver/register consists of two sets of bus transceiver circuits with 3–State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable ($n\overline{OE}$) and Direction (nDIR) pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The select (nSAB, nSBA) pins determine whether data is stored or transferred through the device in real-time. The nDIR determines which bus will receive data when the $n\overline{OE}$ is active Low. In the isolation mode ($n\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time.

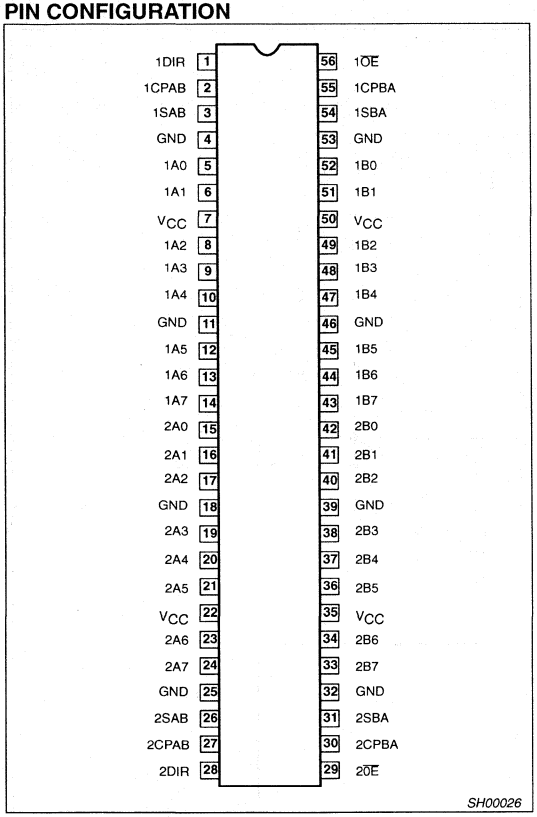
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx	C_L = 50pF; V_{CC} = 5V	2.3 2.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
$C_{I/O}$	I/O capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	550	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-pin plastic SSOP Type III	–40°C to +85°C	BT16646DL	SOT371-1
56-pin plastic TSSOP Type II	–40°C to +85°C	BT16646DGG	SOT364-1

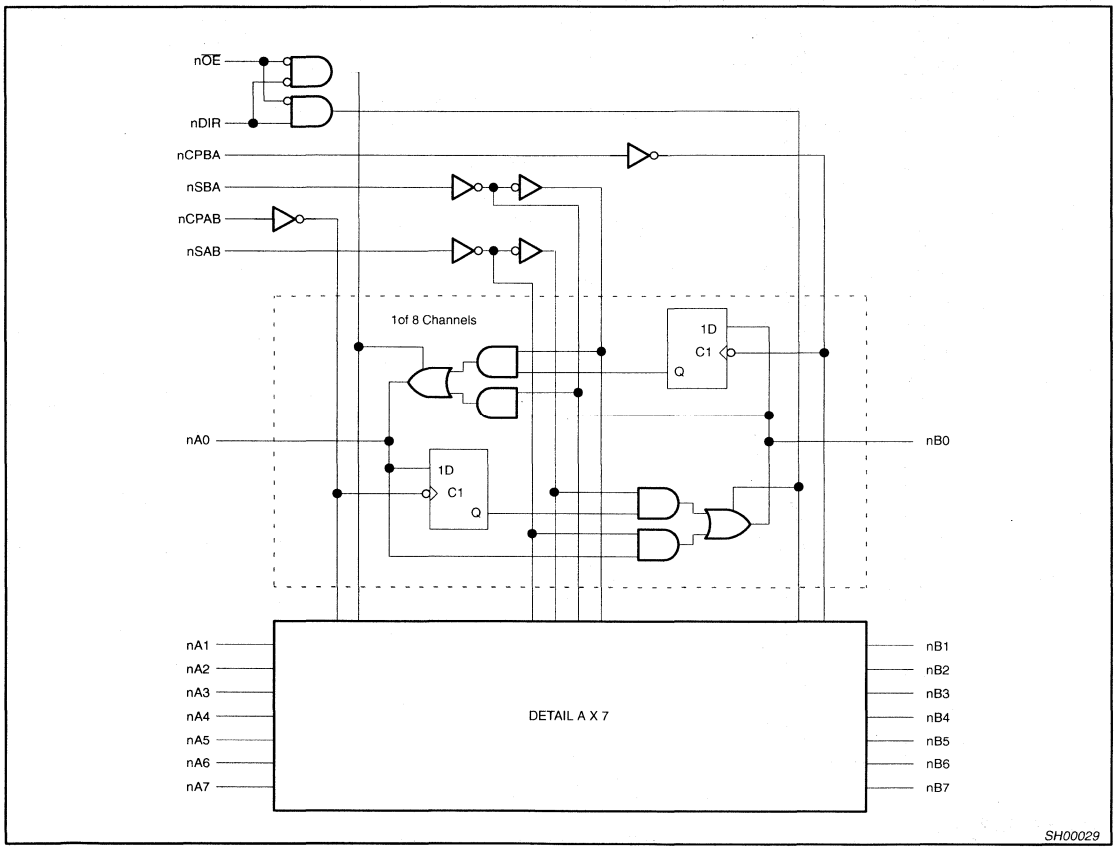
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 55, 27, 30	1CPAB, 1CPBA, 2CPAB, 2CPBA	Clock input A to B / Clock input B to A
3, 54, 26, 31	1SAB, 1SBA, 2SAB, 2SBA	Select input A to B / Select input B to A
1, 28	1DIR, 2DIR	Direction control inputs
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs (A side)
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	Data inputs/outputs (B side)
56, 29	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
nOE	nDIR	nCPAB	nCPBA	nSAB	nSBA	nAx	nBx	
X	X	↑	X	X	X	input	Unspecified output*	Store A, B unspecified
X	X	X	↑	X	X	Unspecified output*	Input	Store B, A unspecified
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Stored A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the nOE input. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low–to–High transition of the clock.

16-bit transceiver/register, non-inverting (3-State) 74ABT16652

FEATURES

- Independent registers for A and B buses
- Multiple V_{CC} and GND pins minimize switching noise
- Power-up 3-State
- Power-up reset
- Live insertion/extraction permitted
- Multiplexed real-time and stored data
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16652 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16652 transceiver/register consists of two sets of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable (nOEAB, n$\overline{OEBA}$) and Select (n$\overline{SAB}$, n$\overline{SBA}$) pins are provided for bus management.

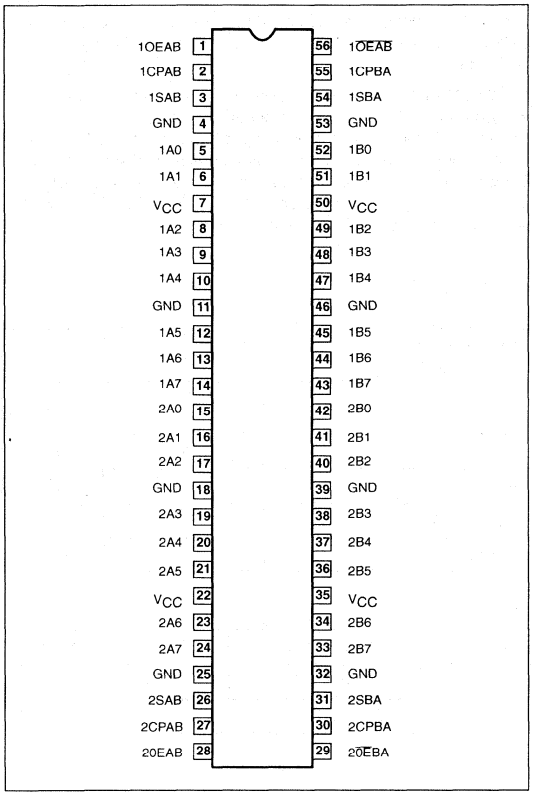
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx	C_L = 50pF; V_{CC} = 5V	2.3 1.8	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5V	500	µA
I_{CCL}		Outputs low; V_{CC} = 5.5V	8	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-pin plastic SSOP, Type III	–40°C to +85°C	BT16652DL	SOT371-1
56-pin plastic TSSOP, Type II	–40°C to +85°C	BT16652DGG	SOT364-1

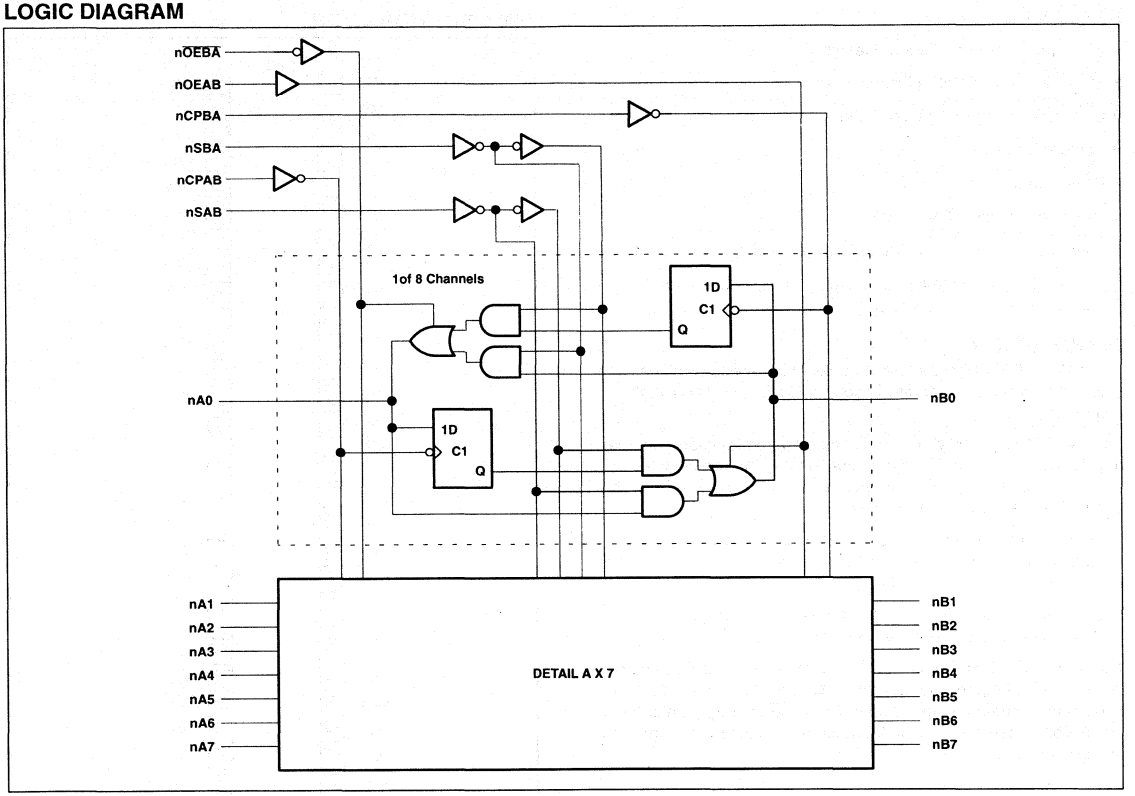
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 55, 27, 30	1CPAB, 1CPBA, 2CPAB, 2CPBA	Clock input A to B / Clock input B to A
3, 54, 26, 31	1SAB, 1SBA, 2SAB, 2SBA	Select input A to B / Select input B to A
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs (A side)
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	Data inputs/outputs (B side)
1, 56, 28, 29	1OEAB, 1$\overline{\text{OEBA}}$, 2OEAB, 2$\overline{\text{OEBA}}$	Output enable inputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
nOEAB	$\overline{\text{nOEBA}}$	nCPAB	nCPBA	nSAB	nSBA	nAx	nBx	
L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B data
X H	H H	↑ ↑	H or L ↑	X **	X X	Input	Unspecified output*	Store A, Hold B Store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X **	Unspecified output*	Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Store A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus Stored B data to A bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the $\overline{\text{nOEBA}}$ and nOEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low–to–High transition of the clock.
** If both Select controls (nSAB and nSBA) are Low, then clocks can occur simultaneously. If either Select control is High, the clocks must be staggered in order to load both registers.

20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

74ABT16821A

FEATURES

- 20-bit positive-edge triggered register
- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16821 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

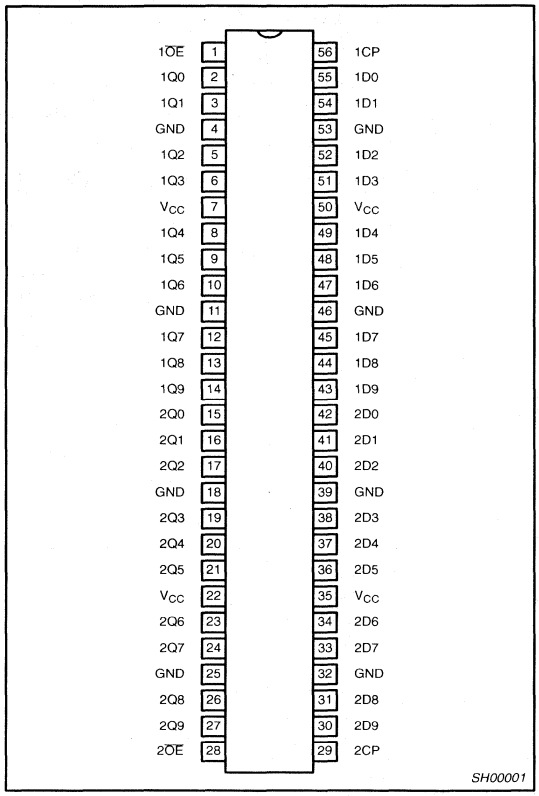
The 74ABT16821 has two 10-bit, edge triggered registers, with each register coupled to ten 3-State output buffers. The two sections of each register are controlled independently by the clock (nCP) and Output Enable ($n\overline{OE}$) control gates.

Each register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active Low Output Enable ($n\overline{OE}$) controls all ten 3-State buffers independent of the register operation. When $n\overline{OE}$ is Low, the data in the register appears at the outputs. When $n\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

PIN CONFIGURATION



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	C_L = 50pF; V_{CC} = 5V	2.4 2.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5V	500	µA
I_{CCL}		Outputs LOW; V_{CC} = 5.5V	10	mA

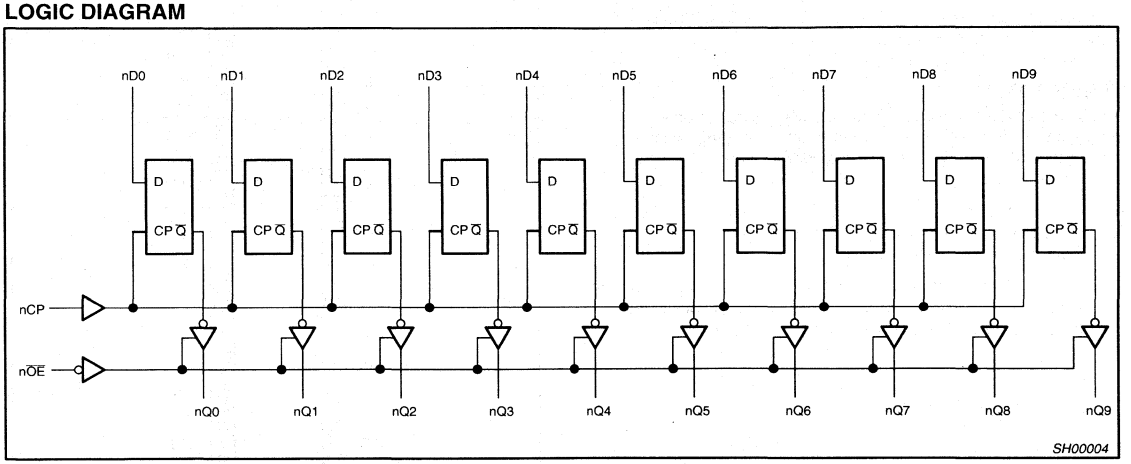
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-Pin plastic SSOP	-40°C to +85°C	BT16821DL	SOT371-1
56-Pin plastic TSSOP	-40°C to +85°C	BT16821DGG	SOT364-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
56, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1D0 - 1D9 2D0 - 2D9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Q0 - 1Q9 2Q0 - 2Q9	Data outputs
1, 28	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
56, 29	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$n\overline{OE}$	nCP	nDx		nQ0 - nQ9	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↕	X	NC	NC	Hold
H H	↕ ↑	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low to High clock transition
↕ = Not a Low-to-High clock transition

18-bit bus-interface D-type flip-flop with reset and enable (3-State)

74ABT16823

FEATURES

- Two sets of high speed parallel registers with positive edge-triggered D-type flip-flops
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up Reset
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

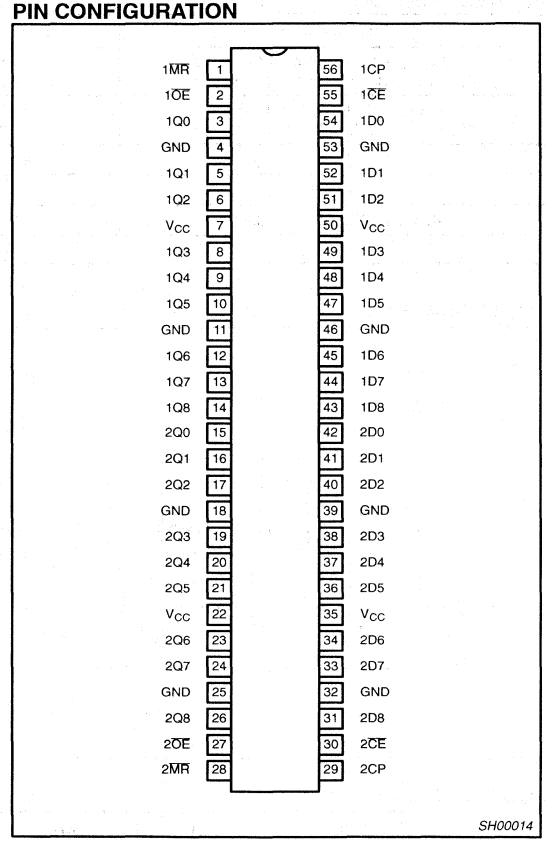
DESCRIPTION

The 74ABT16823 18-bit bus interface register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 74ABT16823 has two 9-bit wide buffered registers with Clock Enable ($n\overline{CE}$) and Master Reset ($n\overline{MR}$) which are ideal for parity bus interfacing in high microprogrammed systems.

The registers are fully edge-triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

PIN CONFIGURATION



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	C_L = 50pF; V_{CC} = 5V	4.6	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-Pin SSOP Type III	–40°C to +85°C	BT16823DL	SOT 371-1
56-Pin TSSOP Type II	–40°C to +85°C	BT16823DGG	SOT 364-1

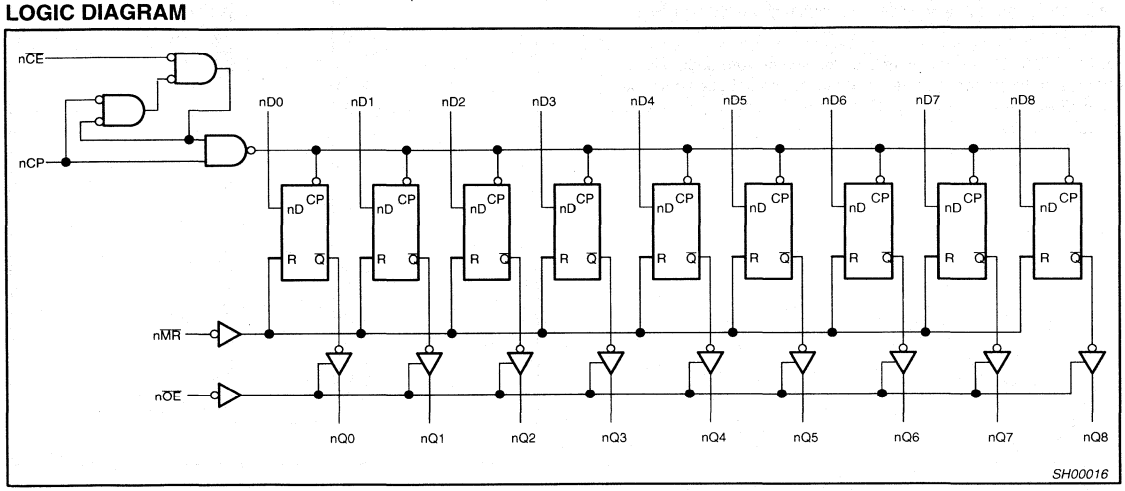
18-bit bus-interface D-type flip-flop with reset and enable (3-State)

74ABT16823

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
2, 27	$1\overline{OE}$, $2\overline{OE}$	Output enable input (active–Low)
54, 52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33, 31	1D0-1D8 2D0-2D8	Data inputs
3, 5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24, 26	1Q0-1Q8 2Q0-2Q8	Data outputs
56, 29	1CP, 2CP	Clock pulse input (active rising edge)
55, 30	$1\overline{CE}$, $2\overline{CE}$	Clock enable input (active–Low)
1, 28	$1\overline{MR}$, $2\overline{MR}$	Master reset input (active–Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
$n\overline{OE}$	$n\overline{MR}$	$n\overline{CE}$	nCP	nDx	nQ0 – nQ8	
L	L	X	X	X	L	Clear
L	H	L	↑	h	H	Load and read data
L	H	L	↑	l	L	
L	H	H	↕	X	NC	Hold
H	X	X	X	X	Z	High impedance

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low to High clock transition
↕ = Not a Low-to-High clock transition

18-bit buffer/line driver; non-inverting (3-State) 74ABT16825

FEATURES

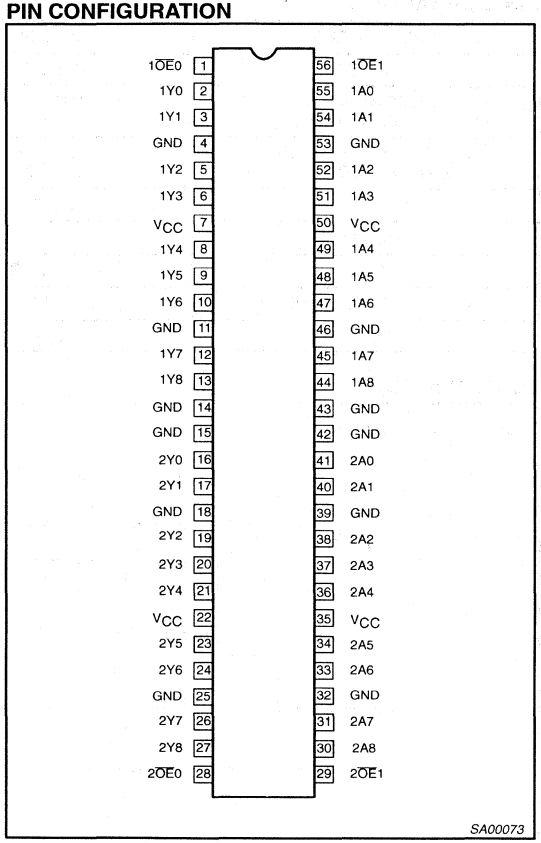
- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- 3-State output buffers
- Power–up 3-State
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The74ABT16825 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The74ABT16825 18-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables ($n\overline{OE}1$, $n\overline{OE}2$) for maximum control flexibility.

PIN CONFIGURATION



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 5V	3.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	80	µA

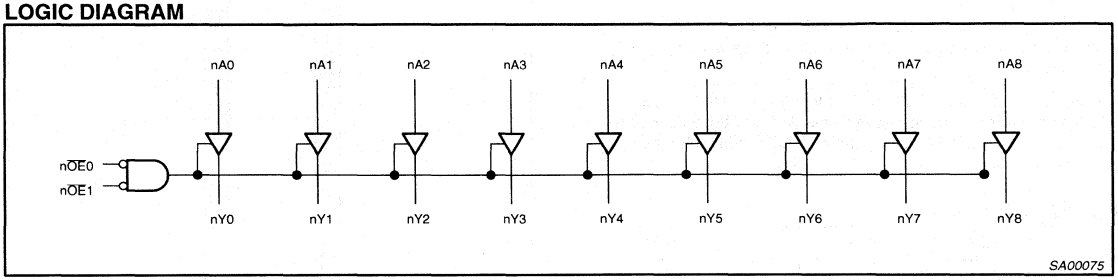
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-pin SSOP Type III	–40°C to +85°C	BT16825DL	SOT371-1
56-pin TSSOP Type II	–40°C to +85°C	BT16825DGG	SOT364-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 41, 40, 38, 37, 36, 34, 33, 31, 30	1A0 – 1A9 2A0 – 2A9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13 16, 17, 19, 20, 21, 23, 24, 26, 27	1Y0 – 1Y9 2Y0 – 2Y9	Data outputs
1, 56 28, 29	$1\overline{OE}0$, $1\overline{OE}1$ $2\overline{OE}0$, $2\overline{OE}1$	Output enable inputs (active–Low)
4, 11, 14, 15, 18, 25, 32, 39, 42, 43, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS	OPERATING MODE
$n\overline{OE}x$	nAx	nYx	
L	L	L	Transparent
L	H	H	Transparent
H	X	Z	High impedance

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

20-bit buffer/line driver, non-inverting (3-State) 74ABT16827

FEATURES

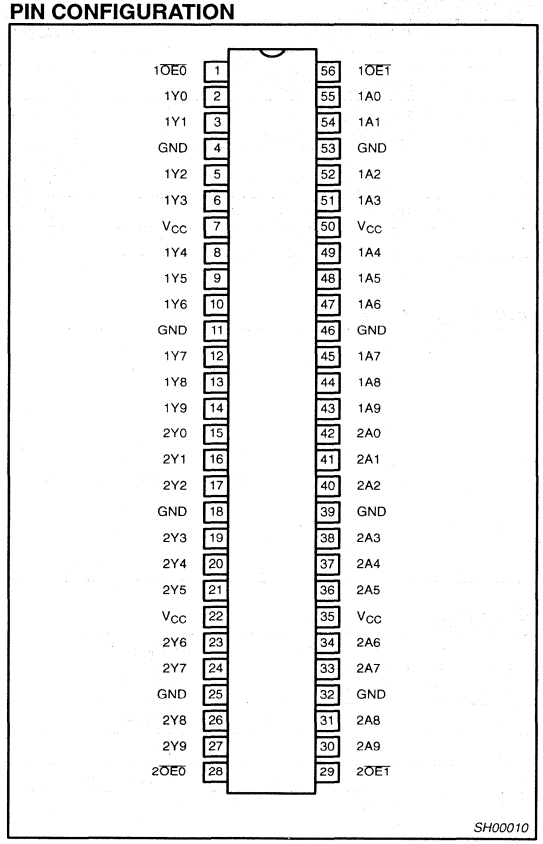
- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- 3-State output buffers
- Power-up 3-State
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT16827 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16827 20-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables ($n\overline{OE}1$, $n\overline{OE}2$) for maximum control flexibility.

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1A0 - 1A9 2A0 - 2A9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Y0 - 1Y9 2Y0 - 2Y9	Data outputs
1, 56, 28, 29	$1\overline{OE}0$, $1\overline{OE}1$ $2\overline{OE}0$, $2\overline{OE}1$	Output enable inputs (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

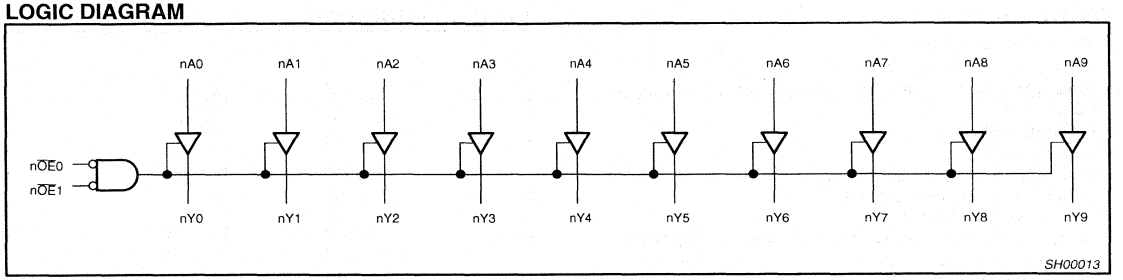
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 5V	3.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	80	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-Pin plastic SSOP Type III	-40°C to +85°C	BT16827DL	SOT370-1
56-Pin plastic TSSOP Type II	-40°C to +85°C	BT16827DGG	SOT364-1

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS	OPERATING MODE
nŌEx	nAx	nYx	
L	L	L	Transparent
L	H	H	Transparent
H	X	Z	High impedance

X = Don't care
Z = High impedance "off" state
H = High voltage level
L = Low voltage level

20-bit bus interface latch (3-State) — 74ABT16841A

FEATURES

- High speed parallel latches
- Live insertion/extraction permitted
- Extra data width for wide address/data paths or buses carrying parity
- Power-up 3-State
- Power-up reset
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

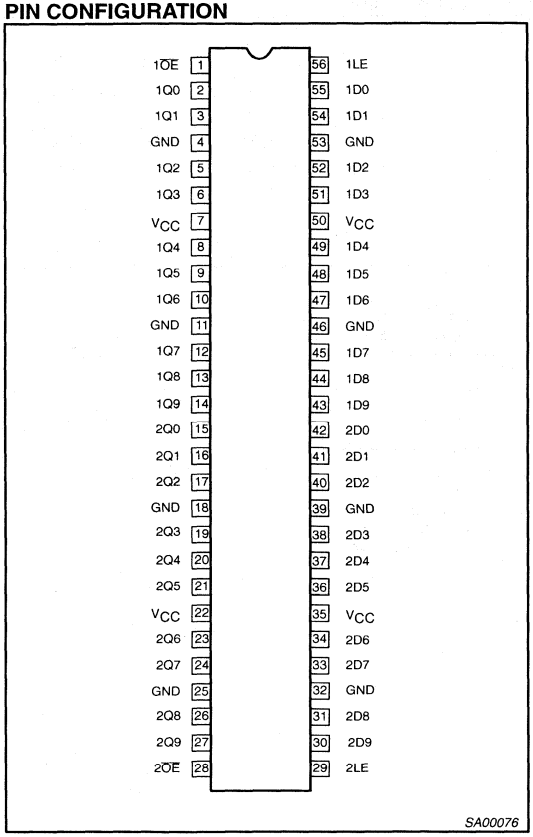
DESCRIPTION

The 74ABT16841 Bus interface register is designed to provide extra data width for wider data/address paths of buses carrying parity.

The 74ABT16841 consists of two sets of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (nLE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the nLE High-to-Low transition, the data that meets the setup and hold time is latched.

Data appears on the bus when the Output Enable ($n\overline{OE}$) is Low. When $n\overline{OE}$ is High the output is in the High-impedance state.

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1D0 – 1D9 2D0 – 2D9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Q0 – 1Q9 2Q0 – 2Q9	Data outputs
1, 28	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
56, 29	1LE, 2LE	Latch enable inputs (active rising edge)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

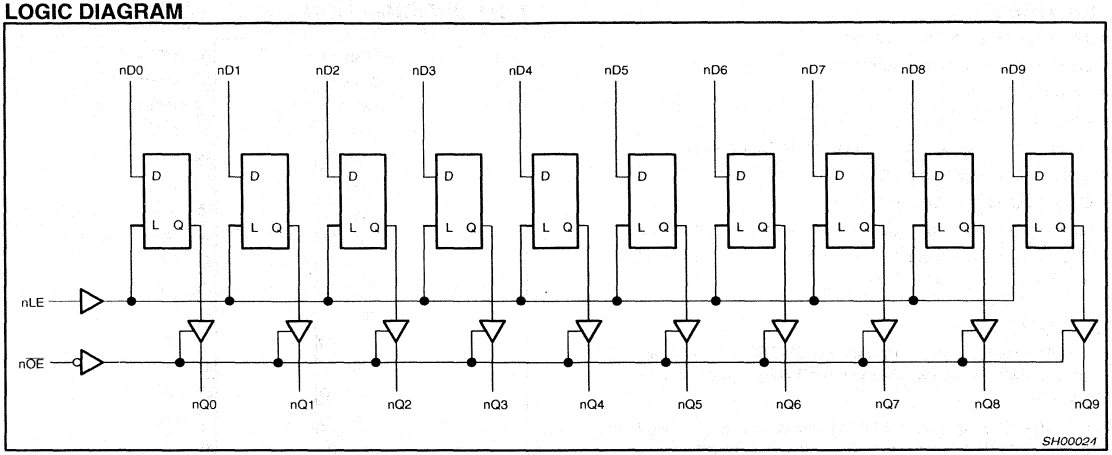
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	C_L = 50pF; V_{CC} = 5V	3.1 2.2	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5V	500	µA
I_{CCL}		Outputs LOW; V_{CC} = 5.5V	10	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-pin SSOP Type III	-40°C to +85°C	BT16841DL	SOT371-1
56-pin TSSOP Type II	-40°C to +85°C	BT16841DGG	SOT364-1

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$n\overline{OE}$	nLE	nDx	nQ0 – nQ9	
L L	H H	L H	L H	Transparent
L L	↓ ↓	l h	L H	Latched
H	X	X	Z	High impedance
L	L	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low LE transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low LE transition
↓ = High-to-Low LE transition
NC= No change
X = Don't care
Z = High impedance "off" state

Dual octal registered transceiver (3-State) 74ABT16952

FEATURES

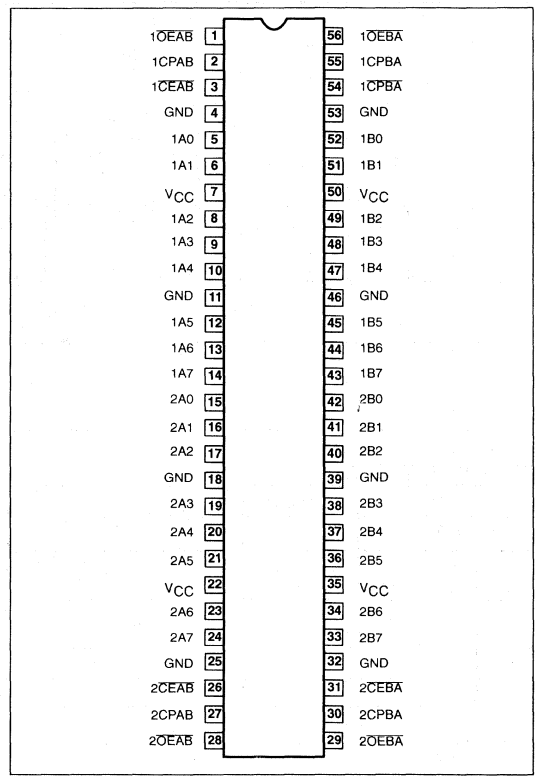
- Two 8-bit registered transceivers
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Multiple V_{CC} and GND pins minimize switching noise
- Independent registers for A and B buses
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16952 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16952 is a dual octal registered transceiver. Two 8-bit registers store data flowing in both directions between two bidirectional buses. Data applied to the inputs is entered and stored on the rising edge of the Clock (nCPXX) provided that the Clock Enable ($n\overline{CEXX}$) is Low. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable ($n\overline{OEXX}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 55 18, 22	1CPAB / 1CPBA 2CPAB / 2CPBA	Clock input A to B / Clock input B to A
3, 54, 26, 31	$1\overline{CEAB}$ / $1\overline{CEBA}$ $2\overline{CEAB}$ / $2\overline{CEBA}$	Clock enable input A to B / Clock enable input B to A
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1A0 – 1A7 2A0 – 2A7	Data inputs/outputs (A side)
1, 56 8, 29	1B0 – 1B7 2B0 – 2B7	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 45, 53	$1\overline{OEAB}$ / $1\overline{OEBA}$ $2\overline{OEAB}$ / $2\overline{OEBA}$	Output enable inputs
4, 17, 30, 43	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

ORDERING INFORMATION

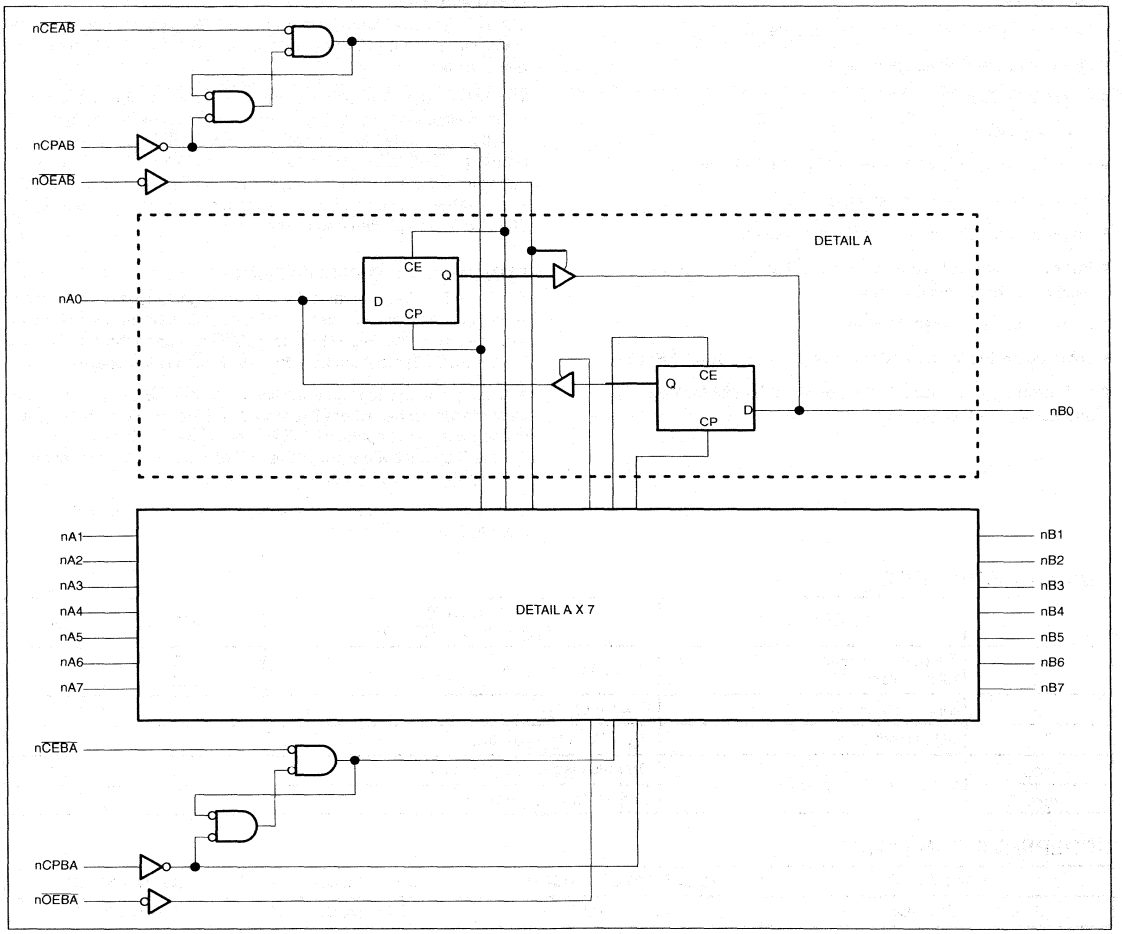
PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
52-pin plastic Quad Flat Pack	–40°C to +85°C	74ABT16952DL	TBD

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCPBA to nAx or nCPAB to nBx	C_L = 50pF; V_{CC} = 5V	5.7	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	120	nA

Dual octal registered transceiver (3-State) 74ABT16952

LOGIC DIAGRAM



FUNCTION TABLE for Register nAx or nBx

INPUTS			INTERNAL	OPERATING
nAx or nBx	nCPXX	nCEXX	Q	MODE
X	X	H	NC	Hold data
L H	↑ ↑	L L	L H	Load data

H = High voltage level
L = Low voltage level
↑ = Low-to-High transition
X = Don't care
XX = AB or BA
NC = No change

FUNCTION TABLE for Output Enable

INPUTS	INTERNAL	nAx or nBx	OPERATING
nOEXX	Q	OUTPUTS	MODE
H	X	Z	Disable outputs
L L	L H	L H	Enable outputs

H = High voltage level
L = Low voltage level
X = Don't care
XX = AB or BA
Z = High impedance "off" state

16-bit latched transceivers with dual enable and Master Reset (3-State)

74ABT16543

FEATURES

- Two 8-bit octal transceivers with D-type latch
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Multiple V_{CC} and GND pins minimize switching noise
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT161543 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT161543 16-bit registered transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable (n$\overline{\text{LEAB}}$, n$\overline{\text{LEBA}}$) and Output Enable (n$\overline{\text{OEAB}}$, n$\overline{\text{OEBA}}$) inputs are provided for each register to permit independent control of data transfer in either direction. Master Reset ($\overline{\text{MR}}$) clears all registers simultaneously and sets them LOW. The outputs are guaranteed to sink 64mA.

FUNCTIONAL DESCRIPTION

The 74ABT161543 contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable (n$\overline{\text{EAB}}$) input and the A-to-B Latch Enable (n$\overline{\text{LEAB}}$) input are Low the A-to-B path is transparent.

A subsequent Low-to-High transition of the n$\overline{\text{LEAB}}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{\text{EAB}}$ and n$\overline{\text{OEAB}}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the n$\overline{\text{EBA}}$, n$\overline{\text{LEBA}}$, and n$\overline{\text{OEBA}}$ inputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx	C_L = 50pF; V_{CC} = 5V	2.5 2.2	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
$C_{I/O}$	I/O capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5V	500	µA
I_{CCZ}		Outputs low; V_{CC} = 5.5V	9	mA

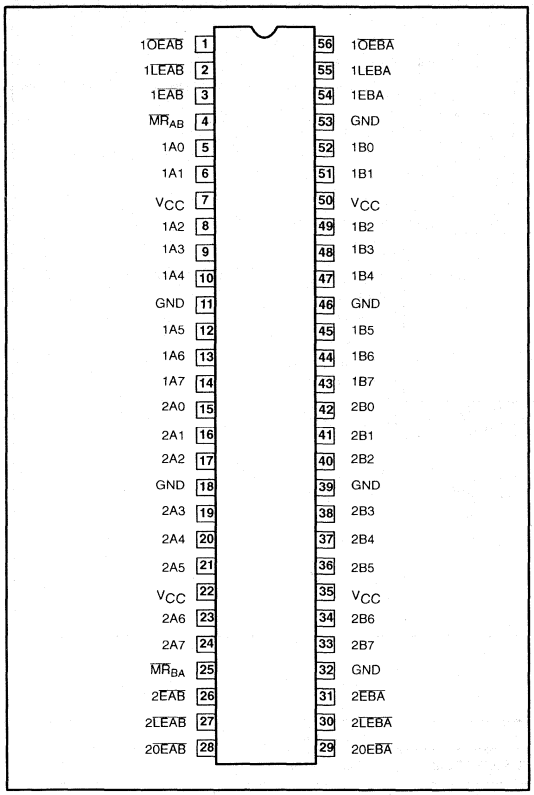
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-pin plastic SSOP Type I	–40°C to +85°C	BT16543DL	SOT371-1
56-pin plastic TSSOP Type II	–40°C to +85°C	BT16543DGG	SOT364-1

16-bit latched transceivers with dual enable and Master Reset (3-State)

74ABT16543

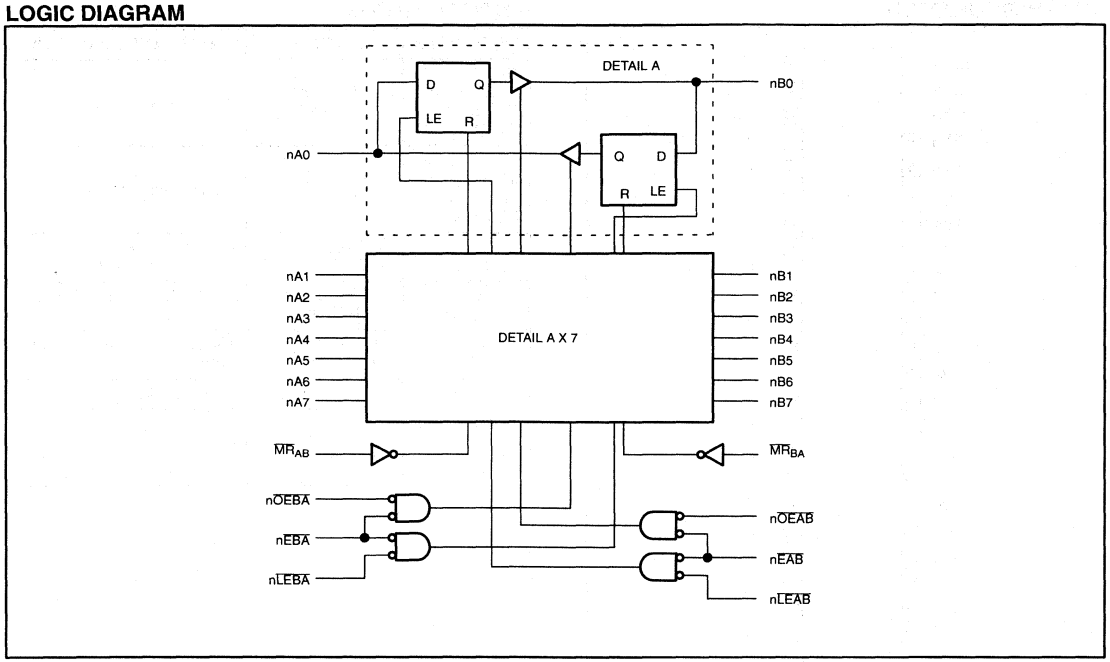
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40,38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	Data inputs/outputs
1, 56 28, 29	1$\overline{OEAB}$, 1$\overline{OEBA}$, 2$\overline{OEAB}$, 2$\overline{OEBA}$	A to B / B to A Output Enable inputs (active-Low)
3, 54 26, 31	1$\overline{EAB}$, 1$\overline{EBA}$, 2$\overline{EAB}$, 2$\overline{EBA}$	A to B / B to A Enable inputs (active-Low)
2, 55 27, 30	1$\overline{LEAB}$, 1$\overline{LEBA}$, 2$\overline{LEAB}$, 2$\overline{LEBA}$	A to B / B to A Latch Enable inputs (active-Low)
4, 25	$\overline{MR}_{AB}$, $\overline{MR}_{BA}$	Master Reset
11, 18, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS	STATUS
$n\overline{OEXX}$	$n\overline{MRXX}$	$n\overline{EXX}$	$n\overline{LEXX}$	nAx or nBx	nBx or nAx	
L	L	L	X	X	L	Clear
H	X	X	X	X	Z	Disabled
X	X	H	X	X	Z	Disabled
L L	H H	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	H H	L L	↑ ↑	h l	H L	Latch + Display
L L	H H	L L	L L	H L	H L	Transparent
L	H	L	H	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High transition of $n\overline{LEXX}$ or $n\overline{EXX}$ (XX = AB or BA)
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High transition of $n\overline{LEXX}$ or $n\overline{EXX}$ (XX = AB or BA)
X = Don't care
↑ = Low-to-High transition of $n\overline{LEXX}$ or $n\overline{EXX}$ (XX = AB or BA)
NC= No change
Z = High impedance or "off" state

ABT16 Netlists

ABT16 BERKELEY SPICE MODELS (for HSPICE Simulation)

```
*****************************************************************************
* ABT16BSH.CIR
* Advanced BiCMOS Logic
* Standard Logic Product Group
* Philips Semiconductors
* 3/31/1995
*****************************************************************************
* To simulate a particular device, locate the device in the section of
* this file titled "ABT16 Circuit Models".  Delete the comment mark "*"
* in the leading column for that device only.  Make sure the "*" is
* present for all other devices on the list.  Also, for the particular
* device chosen, make certain that the suffix is N or S or F to select
* the model type, nominal (N),slow (S) or fast (F), and also remove the
* "*" for the .LIB files just below this statement.  Insure that the
* other parameters in the set are remarked out with the "*" added.  You
* may also wish to adjust the values of the load capacitor and parasitic
* inductors found in the A16XXXBS.LIB files according to the package
* chosen and application being run.  The basic files use nominal values.
*****************************************************************************
*
*
* Common Models for Nominal, Slow and Fast
* (Do not comment out this INCLUDE line)
.INCLUDE "C:\SPICE\ABT16\BSPICE\A16MDLBS.LIB"

* Pick one of the following three:

* Nominal Parameters
.INCLUDE "C:\SPICE\ABT16\BSPICE\A16NOMBS.LIB"

* Slow Parameters
* .INCLUDE "C:\SPICE\ABT16\BSPICE\A16SLOBS.LIB"

* Fast Parameters
* .INCLUDE "C:\SPICE\BSPICE\BSPICE\A16FASBS.LIB"

*** ABT16 Circuit Models

* Select one and only one part type by removing the '* '.

** Under 'Part Type' keep or change XAnnnN to XAnnnF or XAnnnS to retain
** N or F or S designation on the plot.

** The "_1" after the part type denotes a "-1" part type with 30 ohm
** termination resistors on the output.

* Part Type    In En Out  Vcc   Subckt Name
* XA240N        5  7  4   100   INV1

* XA273N        5  7  4   100   NINV

* XA244N        5  7  4   100   A16244

* XA245N        5  7  4   100   A16245

XA240_1N       5  7  4   100   INV1_1

* XA244_1N      5  7  4   100   A16244_1

* XA245-1N      5  7  4   100   A16245_1
```

```
* XA373N       5  7  4   100   NINV

* XA374N       5  7  4   100   NINV

* XA500N       5  7  4   100   NINVB

* XA501N       5  7  4   100   NINVB

* XA541N       5  7  4   100   NINV

* XA543N       5  7  4   100   NINVB

* XA646N       5  7  4   100   NINVB

* XA652N       5  7  4   100   NINVB

* XA821N       5  7  4   100   NINV

* XA823N       5  7  4   100   NINV

* XA825N       5  7  4   100   NINV

* XA827N       5  7  4   100   NINV

* XA841N       5  7  4   100   NINV

* XA899N       5  7  4   100   NINVB

* XA952N       5  7  4   100   NINVB

* XA1543N      5  7  4   100   NINVB

* EXTERNAL LOAD
R10 4 0 500
C10 4 0 50PF

* POWER
VCC 100 0 5.0

* DRIVE
VIN 5 0 PULSE 0.0 3.0 2N 2.5N 2.5N 10N 25N
VOE 7 0 0.0

.TRAN   1.000000E-11  3.500000E-08
.TEMP  .2500E+02
.OPTION  ACCT NODE OPTS LIST LIMTIM=50
+         GMIN=1.00E-12 RELTOL=1.00E-03 ABSTOL=1.00E-12
+         VNTOL=1.00E-06 TRTOL=7.00E+00
+         ITL1=1.00E+02 ITL2=1.00E+02 ITL3=4.00E+00 ITL4=2.50E+01
+         ITL5=1.00E+06 LVLTIM=2.00E+00 TNOM=+2.50E+01 LIMPTS=99999
+         CHGTOL=1.00E-14
+         MAXORD= .20E+01
+         METHOD=TRAP
+         DELMAX= 6.00E-10
+         POST
.END
```

ABT16 BSPICE MODELS (for PSPICE Simulation)

```
**************************************************************************
* ABT16BSP.CIR
* Advanced BiCMOS Logic
* Standard Logic Product Group
* Philips Semiconductors
* 3/31/1995
**************************************************************************
* To simulate a particular device, locate the device in the section of
* this file titled "ABT16 Circuit Models".  Delete the comment mark "*"
* in the leading column for that device only.  Make sure the "*" is
* present for all other devices on the list.  Also, for the particular
* device chosen, make certain that the suffix is N or S or F to select
* the model type, nominal (N),slow (S) or fast (F), and also remove the
* "*" for the .LIB files just below this statement.  Insure that the
* other parameters in the set are remarked out with the "*" added.  You
* may also wish to adjust the values of the load capacitor and parasitic
* inductors found in the A16XXXBS.LIB files according to the package
* chosen and application being run.  The basic files use nominal values.
**************************************************************************
*
*
* Common Models for Nominal, Slow and Fast
* (Do not comment out this .LIB line)
.LIB "C:\SPICE\ABT16\BSPICE\A16MDLBS.LIB"

* Pick one of the following three:

* Nominal Parameters
.LIB "C:\SPICE\ABT16\BSPICE\A16NOMBS.LIB"

* Slow Parameters
* .LIB "C:\SPICE\ABT16\BSPICE\A16SLOBS.LIB"

* Fast Parameters
.LIB "C:\SPICE\ABT16\BSPICE\A16FASBS.LIB"

*** ABT16 Circuit Models

* Select one and only one part type by removing the '* '.

** Under 'Part Type' keep or change XAnnnN to XAnnnF or XAnnnS to retain
** N or F or S designation on the plot.

** The "_1" after the part type denotes a "-1" part type with 30 ohm
** termination resistors on the output.

* Part Type    In En Out  Vcc  Subckt Name
* XA240N        5  7  4   100   INV1

* XA273N        5  7  4   100   NINV

* XA244N        5  7  4   100   A16244

* XA245N        5  7  4   100   A16245

XA240_1N       5  7  4   100   INV1_1

* XA244_1N      5  7  4   100   A16244_1

* XA245_1N      5  7  4   100   A16245_1
```

```
* XA373N       5  7  4   100   NINV
* XA374N       5  7  4   100   NINV
* XA500N       5  7  4   100   NINVB
* XA501N       5  7  4   100   NINVB
* XA541N       5  7  4   100   NINV
* XA543N       5  7  4   100   NINVB
* XA646F       5  7  4   100   NINVB
* XA652N       5  7  4   100   NINVB
* XA821N       5  7  4   100   NINV
* XA823N       5  7  4   100   NINV
* XA825N       5  7  4   100   NINV
* XA827N       5  7  4   100   NINV
* XA841N       5  7  4   100   NINV
* XA899N       5  7  4   100   NINVB
* XA952N       5  7  4   100   NINVB
* XA1543N      5  7  4   100   NINVB

* EXTERNAL LOAD
R10 4 0 500
C10 4 0 50PF

* POWER
VCC 100 0 5.0

* DRIVE
VIN 5 0 PULSE 0.0 3.0 2N 2.5N 2.5N 10N 25N
VOE 7 0 0.0

.TRAN   1N  35N  ; 0 1P
.OPTIONS ITL4=50
.TEMP  25
.PROBE
.END
```

ABT16 HSPICE MODELS

```
*****************************************************************************
* ABT16HS.CIR
* Advanced BiCMOS Logic
* Standard Logic Product Group
* Philips Semiconductors
* 3/31/1995
*****************************************************************************
* To simulate a particular device, locate the device in the section of
* this file titled "ABT16 Circuit Models".  Delete the comment mark "*"
* in the leading column for that device only.  Make sure the "*" is
* present for all other devices on the list.  Also, for the particular
* device chosen, make certain that the suffix is N or S or F to select
* the model type, nominal (N),slow (S) or fast (F), and also remove the
* "*" for the .LIB files just below this statement.  Insure that the
* other parameters in the set are remarked out with the "*" added.  You
* may also wish to adjust the values of the load capacitor and parasitic
* inductors found in the A16XXXHS.LIB files according to the package
* chosen and application being run.  The basic files use nominal values.
*****************************************************************************
*
*
* Common Models for Nominal, Slow and Fast
* (Do not comment out this INCLUDE line)
.INCLUDE "C:\SPICE\ABT16\HSPICE\A16MDLHS.LIB"

* Pick one of the following three:

* Nominal Parameters
.INCLUDE "C:\SPICE\ABT16\HSPICE\A16NOMHS.LIB"

* Slow Parameters
* .INCLUDE "C:\SPICE\ABT16\HSPICE\A16SLOHS.LIB"

* Fast Parameters
.INCLUDE "C:\SPICE\ABT16\HSPICE\A16FASHS.LIB"

*** ABT16 Circuit Models

* Select one and only one part type by removing the '*'.

** Under 'Part Type' keep or change XAnnnN to XAnnnF or XAnnnS
** to retain N or F or S designation on the plot.

** The "_1" after the part type denotes a "-1" part type with 30 ohm
** termination resistors on the output.

* Part Type    In En Out  Vcc   Subckt Name
* XA240N        5  7   4   100   INV1

* XA273N        5  7   4   100   NINV

* XA244N        5  7   4   100   A16244

XA245N         5  7   4   100   A16245

* XA240_1N      5  7   4   100   INV1_1

* XA244_1N      5  7   4   100   A16244_1

* XA245-1N      5  7   4   100   A16245_1
```

```
* XA373N        5   7   4    100    NINV
* XA374N        5   7   4    100    NINV
* XA500N        5   7   4    100    NINVB
* XA501N        5   7   4    100    NINVB
* XA541N        5   7   4    100    NINV
* XA543N        5   7   4    100    NINVB
* XA646N        5   7   4    100    NINVB
* XA652N        5   7   4    100    NINVB
* XA821N        5   7   4    100    NINV
* XA823N        5   7   4    100    NINV
* XA825N        5   7   4    100    NINV
* XA827N        5   7   4    100    NINV
* XA841N        5   7   4    100    NINV
* XA899N        5   7   4    100    NINVB
* XA952N        5   7   4    100    NINVB
* XA1543N       5   7   4    100    NINVB

* EXTERNAL LOAD
R10  4  0  500
C10  4  0  50PF

* POWER
VCC  100  0  5.0

* DRIVE
VIN  5  0  PULSE  0.0  3.0  2N  2.5N  2.5N  10N  25N
VOE  7  0  0.0

.TRAN    1.000000E-11   3.500000E-08
.TEMP   .2500E+02
.OPTION  ACCT NODE OPTS LIST LIMTIM=50
+         GMIN=1.00E-12 RELTOL=1.00E-03 ABSTOL=1.00E-12
+         VNTOL=1.00E-06 TRTOL=7.00E+00
+         ITL1=1.00E+02 ITL2=1.00E+02 ITL3=4.00E+00 ITL4=2.50E+01
+         ITL5=1.00E+06 LVLTIM=2.00E+00 TNOM=+2.50E+01 LIMPTS=99999
+         CHGTOL=1.00E-14
+         MAXORD= .20E+01
+         METHOD=TRAP
+         DELMAX= 6.00E-10
+         POST
.END
```

ABT16 PSPICE MODELS

```
**************************************************************************
* ABT16PS.CIR
* Advanced BiCMOS Logic
* Standard Logic Product Group
* Philips Semiconductors
* 3/31/1995
**************************************************************************
* To simulate a particular device, locate the device in the section of
* this file titled "ABT16 Circuit Models".  Delete the comment mark "*"
* in the leading column for that device only.  Make sure the "*" is
* present for all other devices on the list.  Also, for the particular
* device chosen, make certain that the suffix is N or S or F to select
* the model type, nominal (N),slow (S) or fast (F), and also remove the
* "*" for the .LIB files just below this statement.  Insure that the
* other parameters in the set are remarked out with the "*" added.  You
* may also wish to adjust the values of the load capacitor and parasitic
* inductors found in the A16XXXPS.LIB files according to the package
* chosen and application being run.  The basic files use nominal values.
**************************************************************************
*
*
* Common Models for Nominal, Slow and Fast
* (Do not comment out this INCLUDE line)
.LIB "C:\SPICE\ABT16\PSPICE\A16MDLPS.LIB"

* Pick one of the following three:

* Nominal Parameters
.LIB "C:\SPICE\ABT16\PSPICE\A16NOMPS.LIB"

* Slow Parameters
* .LIB "C:\SPICE\ABT16\PSPICE\A16SLOPS.LIB"

* Fast Parameters
* .LIB "C:\SPICE\ABT16\PSPICE\A16FASPS.LIB"

*** ABT16 Circuit Models

* Select one and only one part type by removing the '* '.

** Under 'Part Type' keep or change XAnnnN to XAnnnF or XAnnnS to retain
** N or F or S designation on the plot.

** The "_1" after the part type denotes a "-1" part type with 30 ohm
** termination resistors on the output.

* Part Type    In En Out  Vcc  Subckt Name
* XA240N        5  7  4   100   INV1

* XA273N        5  7  4   100   NINV

* XA244N        5  7  4   100   A16244

* XA245N        5  7  4   100   A16245

XA240_1N       5  7  4   100   INV1_1

* XA244_1N      5  7  4   100   A16244_1

* XA245_1N      5  7  4   100   A16245_1
```

```
* XA373N       5  7  4   100   NINV
* XA374N       5  7  4   100   NINV
* XA500N       5  7  4   100   NINVB
* XA501N       5  7  4   100   NINVB
* XA541N       5  7  4   100   NINV
* XA543N       5  7  4   100   NINVB
* XA646N       5  7  4   100   NINVB
* XA652N       5  7  4   100   NINVB
* XA821N       5  7  4   100   NINV
* XA823N       5  7  4   100   NINV
* XA825N       5  7  4   100   NINV
* XA827N       5  7  4   100   NINV
* XA841N       5  7  4   100   NINV
* XA899N       5  7  4   100   NINVB
* XA952N       5  7  4   100   NINVB
* XA1543N      5  7  4   100   NINVB

* EXTERNAL LOAD
R10 4 0 500
C10 4 0 50PF

* POWER
VCC 100 0 5.0

* DRIVE
VIN 5 0 PULSE 0.0 3.0 2N 2.5N 2.5N 10N 25N
VOE 7 0 0.0

.TRAN   1N  35N  ; 0 1P
.OPTIONS ITL4=50
.TEMP  25
.PROBE
.END
```

A16NOMBS.LIB Subcircuit

```
*****************************************************************************
* ABT16 BERKELEY SPICE SUBCIRCUIT LIBRARY
* A16NOMBS.LIB
* NOMINAL PROCESS CORNER
* STANDARD LOGIC PRODUCT GROUP
* PHILIPS SEMICONDUCTORS
* 3/31/1995
*****************************************************************************
.SUBCKT INV1 D E Q VCC
* USE THIS MODEL FOR ABT16240 (INVERTING PART)
*    IN   OUT   INTVCC   INTGND    (ENABLE)
X1   3     90     99        6           INBUFFN
*    IN   OUT   INTVCC   INTGND    (SIGNAL)
X2   1     91     99        6           MOSINVN
*    D     EN    OUT    INTVCC   INTGND
X3   91    90     2       99        6      OUTBUFFN
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1
*
.SUBCKT INV1_1 D E Q VCC
* USE THIS MODEL FOR ABT16240-1 (INVERTING PART)
*    IN   OUT   INTVCC   INTGND    (ENABLE)
X1   3     90     99        6           INBUFFN
*    IN   OUT   INTVCC   INTGND    (SIGNAL)
X2   1     91     99        6           MOSINVN
*    D     EN    OUT    INTVCC   INTGND
X3   91    90     2       99        6      OUTBUF1N
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1_1
.SUBCKT INV2 D E Q VCC
*
*    IN   OUT   INTVCC   INTGND    (ENABLE)
X1   3     90     99        6           INBUFFN
*    IN   OUT   INTVCC   INTGND    (SIGNAL)
X2   1     91     99        6           MOSINVN
*    D     EN    OUT    INTVCC   INTGND
X3   91    90     2       99        6      OUTBUFFN
*    IN   OUT   INTVCC   INTGND
X4    2    1      99        6           BCKLOADN
```

```
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV2
.SUBCKT NINV D E Q VCC
* USE THIS MODEL FOR ABT16273  -373B  -374B  -541
*  -821  -823  -825  -827  -841  (NON-INVERTING)
*   IN  OUT  INTVCC  INTGND  (ENABLE)
X1  3    90    99       6          INBUFFN
*   IN  OUT  INTVCC  INTGND  (SIGNAL)
X2  1    91    99       6          INBUFFN
*   D    EN   OUT   INTVCC  INTGND
X3  91   90    2      99       6     OUTBUFFN
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINV
*
.SUBCKT NINVB D E Q VCC
* USE THIS MODEL FOR ABT16500  -501  -543  -646  -652  -899
* -952  -1543
*   IN  OUT  INTVCC  INTGND  (ENABLE)
X1  3    90    99       6          INBUFFN
*   IN  OUT  INTVCC  INTGND  (SIGNAL)
X2  1    91    99       6          INBUFFN
*   D    EN   OUT   INTVCC  INTGND
X3  91   90    2      99       6     OUTBUFFN
*   IN  OUT  INTVCC  INTGND
X4   2    1    99       6          BCKLOADN
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINVB
*
```

```
.SUBCKT A16244 D E Q VCC
* USE THIS MODEL FOR ABT16244A
*    D     EN    OUT    INTVCC   INTGND
X3   1      3     2        99       6      A16244N
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16244
*
.SUBCKT A16245 D E Q VCC
* USE THIS MODEL FOR ABT16245B
*    D     EN    OUT    INTVCC   INTGND
X3   1      3     2        99       6      A16245N
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16245
*
.SUBCKT A16244_1 D E Q VCC
* USE THIS MODEL FOR ABT16244-1
*    D     EN    OUT    INTVCC   INTGND
X3   1      3     2        99       6      A162441N
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16244_1
*
```

```
.SUBCKT A16245_1 D E Q VCC
* USE THIS MODEL FOR ABT16245A-1
*   D     EN    OUT    INTVCC   INTGND
X3  1      3     2       99       6      A162451N
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16245_1
*
* Philips Semiconductors - MOSINVN
.SUBCKT MOSINVN   9913 9902 9903 9901
MM1      9903 9913 1 9903 MHS4XPEN L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
MM2      1 9913 9901 9901 MHS4XNEN L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
MM3      9902 1 9901 9901 MHS4XNEN L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
MM4      9903 1 9902 9903 MHS4XPEN L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.ENDS MOSINVN
* Philips Semiconductors - INBUFFN
.SUBCKT INBUFFN   9913 9902 9903 9901
MM1      9902 9913 9901 9901 MHS4XNEN L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
MM2      9903 9913 1 9903 MHS4XPEN L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
QQ1      9913 9901 9901 ESDXXXXN
RR1      1 9902 100
.ENDS INBUFFN
* Philips Semiconductors - OUTBUFFN
.SUBCKT OUTBUFFN 9912 9917 9902 9903 9901
MM2      2 3 1 9903 MHS4XPEN L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
MM3      1 4 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 5 9901 9901 MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 9901 9901 MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM13     7 4 2 9903 MHS4XPEN L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
QQ1      9903 8 5 DA04CASN
QQ2      1 1 9 DA0ACBSN
QQ3      9902 6 9901 DE283ASN
QQ4      11 10 12 DE283ASN
XQ5      11 13 10 9901 DB14CASN
XD1      9 9902 9901 DB0814AN
RR7      6 9901 1K
```

```
XD3      12 9902 9901 DB3002AN
RR8      9903 11 15
MM43     9903 4 14 9903 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     14 9912 13 9903 MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     13 4 9901 9901 MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM46     13 9912 9901 9901 MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     9903 4 15 9903 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     15 9912 10 9903 MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     10 4 9901 9901 MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM58     10 9912 9901 9901 MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
RR9      9903 7 10K
QQ6      11 10 12 DE283ASN
XD5      12 9902 9901 DB3002AN
XD6      12 9902 9901 DB3002AN
XD7      12 9902 9901 DB3002AN
XD8      12 9902 9901 DB3002AN
QQ7      9902 6 9901 DE283ASN
QQ8      9902 6 9901 DE283ASN
QQ9      9902 6 9901 DE283ASN
MM61     9903 17 16 9903 MHS4XPEN L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
MM62     16 9917 18 9901 MHS4XNEN L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
MM63     18 9912 6 9901 MHS4XNEN L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
MM64     17 9902 9901 9901 MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM65     9903 9902 17 9903 MHS4XPEN L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
MM66     9902 9917 19 9901 MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM67     19 9912 9901 9901 MHS4XNEN L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM68     3 9912 9901 9901 MHS4XNEN L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
MM69     9903 9912 3 9903 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM70     8 9912 9901 9901 MHS4XNEN L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
MM71     9903 9912 8 9903 MHS4XPEN L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM72     5 9912 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM73     9903 9912 5 9903 MHS4XPEN L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
QQ14     9903 1 6 DA0ACBSN
QQ15     9902 9901 9901 ESDXXXXN
MM74     4 9917 9901 9901 MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM75     9903 9917 4 9903 MHS4XPEN L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
.ENDS OUTBUFFN
```

```
* Philips Semiconductors - OUTBUF1N
.SUBCKT OUTBUF1N 9912 9917 9902 9903 9901
MM2     2 3 1 9903 MHS4XPEN L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
MM3     1 4 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4     1 5 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5     6 5 9901 9901 MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6     6 4 9901 9901 MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM13    7 4 2 9903 MHS4XPEN L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
QQ1     9903 8 5 DA04CASN
QQ2     1 1 9 DA0ACBSN
QQ3     9952 6 9901 DE283ASN
RR22    9902 9952 22.5
QQ4     11 10 12 DE283ASN
XQ5     11 13 10 9901 DB14CASN
XD1     9 9952 9901 DB0814AN
RR7     6 9901 1K
XD3     12 9902 9901 DB3002AN
RR8     9903 11 15
MM43    9903 4 14 9903 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44    14 9912 13 9903 MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45    13 4 9901 9901 MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM46    13 9912 9901 9901 MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55    9903 4 15 9903 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56    15 9912 10 9903 MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57    10 4 9901 9901 MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM58    10 9912 9901 9901 MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
RR9     9903 7 10K
QQ6     11 10 12 DE283ASN
XD5     12 9902 9901 DB3002AN
XD6     12 9902 9901 DB3002AN
XD7     12 9902 9901 DB3002AN
XD8     12 9902 9901 DB3002AN
QQ7     9952 6 9901 DE283ASN
QQ8     9952 6 9901 DE283ASN
QQ9     9952 6 9901 DE283ASN
MM61    9903 17 16 9903 MHS4XPEN L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
MM62    16 9917 18 9901 MHS4XNEN L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
MM63    18 9912 6 9901 MHS4XNEN L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
MM64    17 9902 9901 9901 MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM65    9903 9902 17 9903 MHS4XPEN L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
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MM66     9902 9917 19 9901 MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM67     19 9912 9901 9901 MHS4XNEN L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM68     3 9912 9901 9901 MHS4XNEN L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
MM69     9903 9912 3 9903 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM70     8 9912 9901 9901 MHS4XNEN L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
MM71     9903 9912 8 9903 MHS4XPEN L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM72     5 9912 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM73     9903 9912 5 9903 MHS4XPEN L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
QQ14     9903 1 6 DA0ACBSN
QQ15     9902 9901 9901 ESDXXXXN
MM74     4 9917 9901 9901 MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM75     9903 9917 4 9903 MHS4XPEN L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
.ENDS OUTBUF1N
* Philips Semiconductors - BCKLOADN
.SUBCKT BCKLOADN 9913 9902 9903 9901
XD9      9901 9913 9901 DB3002AN
XD10     9901 9913 9901 DB3002AN
XD11     9901 9913 9901 DB3002AN
XD12     9901 9913 9901 DB3002AN
XD13     9901 9913 9901 DB3002AN
MM60     9913 9901 9901 9901 MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
XD14     9913 9903 9901 DB0814AN
QQ10     9913 9901 9901 DE283ASN
QQ11     9913 9901 9901 DE283ASN
QQ12     9913 9901 9901 DE283ASN
QQ13     9913 9901 9901 DE283ASN
MM61     9903 9902 1 1 MHS4XPEN L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
MM62     1 9902 9901 9901 MHS4XNEN L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
.ENDS BCKLOADN
* Philips Semiconductors - BUSHLD1N
.SUBCKT BUSHLD1N 9921 9903 9901
XD1      1 2 9901 DB3002AN
QQ1      3 3 1 DE283ASN
RR1      2 9921 2K
RR2      9921 4 5K
MM4      4 5 9901 9901 MHS4XNEN L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
MM1      5 9921 9901 9901 MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM2      9903 9921 5 5 MHS4XPEN L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM3      9903 5 3 3 MHS4XPEN L=1.0U W=8.298U
+ AD=16.596P AS=16.596P PD=20.596U PS=20.596U NRD=0.241 NRS=0.241
.ENDS BUSHLD1N
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* Philips Semiconductors - ABT16244N
.SUBCKT A16244N   9912 9917 9902 9903 9901
MM1      1 26 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM2      3 4 2 9903 MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM3      1 4 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 26 9901 9901 MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 9901 9901 MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM7      5 7 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM8      9 7 8 9901 MHS4XNEN L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
MM9      8 7 6 9901 MHS4XNEN L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
MM10     9902 7 10 9901 MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM11     10 7 9901 9901 MHS4XNEN L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM12     2 26 11 9903 MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM13     12 5 3 9903 MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM14     9903 7 5 9903 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
QQ1      9903 11 6 DA0ACBSN
QQ2      11 11 13 DA06CBSN
QQ3      9902 6 9901 DE283ASN
QQ4      15 14 16 DE283ASN
XQ5      15 17 14 9901 DB14CASN
MM15     9903 9917 18 9903 MHS4XPEN L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM16     9903 18 4 9903 MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM17     18 9917 9901 9901 MHS4XNEN L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
MM18     4 18 9901 9901 MHS4XNEN L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
XD1      13 9902 9901 DB0308AN
RR7      6 9901 1K
XD2      9902 9 9901 DB0814AN
XD3      16 9902 9901 DB3002AN
RR8      9903 15 15
MM19     9903 4 19 9903 MHS4XPEN L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM20     19 26 7 9903 MHS4XPEN L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM21     7 4 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM22     7 26 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM23     21 18 20 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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MM24     20 26 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM25     9903 18 21 9903 MHS4XPEN L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM26     9903 26 21 9903 MHS4XPEN L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM43     9903 4 22 9903 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     22 21 17 9903 MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     17 4 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM46     17 21 9901 9901 MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     9903 4 23 9903 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     23 21 14 9903 MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     14 4 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM58     14 21 9901 9901 MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
RR9      9903 12 10K
QQ6      15 14 16 DE283ASN
XD5      16 9902 9901 DB3002AN
XD6      16 9902 9901 DB3002AN
XD7      16 9902 9901 DB3002AN
XD8      16 9902 9901 DB3002AN
QQ7      9902 6 9901 DE283ASN
QQ8      9902 6 9901 DE283ASN
QQ9      9902 6 9901 DE283ASN
QQ14     9917 9901 9901 ESDXXXXN
QQ15     26 9901 9901 ESDXXXXN
QQ16     9902 9901 9901 ESDXXXXN
M3M1   9903 9912 25 9903 MHS4XPEN L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3M2   25 9912 9901 9901 MHS4XNEN L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3M3   26 25 9901 9901 MHS4XNEN L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3M4   9903 25 26 9903 MHS4XPEN L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
XD15     24 1 9901 DB0814AN
XD16     11 24 9901 DB0814AN
RR13     9901 9912 10MEG
.ENDS A16244N
* Philips Semiconductors - ABT16245N
.SUBCKT A16245N    9912 9917 9902 9903 9901
MM1      1 28 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM2      3 4 2 9903 MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM3      1 4 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 28 9901 9901 MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
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MM6     6 4 9901 9901 MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM7     5 7 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM8     8 7 9 9901 MHS4XNEN L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
MM9     9 7 6 9901 MHS4XNEN L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
MM10    9902 7 10 9901 MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM11    10 7 9901 9901 MHS4XNEN L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM12    2 28 11 9903 MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM13    12 5 3 9903 MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM14    9903 7 5 9903 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
QQ1     9903 11 6 DA0ACBSN
QQ2     11 11 13 DA06CBSN
QQ3     9902 6 9901 DE283ASN
QQ4     15 14 16 DE283ASN
XQ5     15 17 14 9901 DB14CASN
MM15    9903 9908 18 9903 MHS4XPEN L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM16    9903 18 4 9903 MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM17    18 9908 9901 9901 MHS4XNEN L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
MM18    4 18 9901 9901 MHS4XNEN L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
XD1     13 9902 9901 DB0308AN
RR7     6 9901 1K
XD2     9902 8 9901 DB0814AN
XD3     16 9902 9901 DB3002AN
RR8     9903 15 15
MM19    9903 4 19 9903 MHS4XPEN L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM20    19 28 7 9903 MHS4XPEN L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM21    7 4 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM22    7 28 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM23    20 18 21 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM24    21 28 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM25    9903 18 20 9903 MHS4XPEN L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM26    9903 28 20 9903 MHS4XPEN L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM43    9903 4 22 9903 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44    22 20 17 9903 MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45    17 4 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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MM46    17 20 9901 9901 MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55    9903 4 23 9903 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56    23 20 14 9903 MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57    14 4 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM58    14 20 9901 9901 MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
RR9     9903 12 10K
QQ6     15 14 16 DE283ASN
XD5     16 9902 9901 DB3002AN
XD6     16 9902 9901 DB3002AN
XD7     16 9902 9901 DB3002AN
XD8     16 9902 9901 DB3002AN
QQ7     9902 6 9901 DE283ASN
QQ8     9902 6 9901 DE283ASN
QQ9     9902 6 9901 DE283ASN
XD9     9901 28 9901 DB3002AN
XD10    9901 28 9901 DB3002AN
XD11    9901 28 9901 DB3002AN
XD12    9901 28 9901 DB3002AN
XD13    9901 28 9901 DB3002AN
MM60    28 9901 9901 9901 MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
XD14    28 9903 9901 DB0814AN
QQ10    24 9901 9901 DE283ASN
QQ11    24 9901 9901 DE283ASN
QQ12    24 9901 9901 DE283ASN
QQ13    24 9901 9901 DE283ASN
RR11    28 24 22.5
QQ14    9908 9901 9901 ESDXXXXN
QQ15    28 9901 9901 ESDXXXXN
QQ16    9902 9901 9901 ESDXXXXN
MM61    9903 9902 25 9903 MHS4XPEN L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
MM62    25 9902 9901 9901 MHS4XNEN L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
XD15    11 26 9901 DB0814AN
XD16    26 1 9901 DB0814AN
M3M1  9903 9912 27 9903 MHS4XPEN L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3M2  27 9912 9901 9901 MHS4XNEN L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3M3  28 27 9901 9901 MHS4XNEN L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3M4  9903 27 28 9903 MHS4XPEN L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.ENDS A16245N
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* Philips Semiconductors - ABT162441N
.SUBCKT A162441N  9912 9917 9902 9903 9901
MM1      1 26 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM2      3 4 2 9903 MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM3      1 4 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 26 9901 9901 MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 9901 9901 MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM7      5 7 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM8      9 7 8 9901 MHS4XNEN L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
MM9      8 7 6 9901 MHS4XNEN L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
MM10     9902 7 10 9901 MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM11     10 7 9901 9901 MHS4XNEN L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM12     2 26 11 9903 MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM13     12 5 3 9903 MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM14     9903 7 5 9903 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
QQ1      9903 11 6 DA0ACBSN
QQ2      11 11 13 DA06CBSN
QQ3      9952 6 9901 DE283ASN
RR22     OUT OUTA 22.5
QQ4      15 14 16 DE283ASN
XQ5      15 17 14 9901 DB14CASN
MM15     9903 9917 18 9903 MHS4XPEN L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM16     9903 18 4 9903 MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM17     18 9917 9901 9901 MHS4XNEN L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
MM18     4 18 9901 9901 MHS4XNEN L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
XD1      13 9952 9901 DB0308AN
RR7      6 9901 1K
XD2      9902 9 9901 DB0814AN
XD3      16 9902 9901 DB3002AN
RR8      9903 15 15
MM19     9903 4 19 9903 MHS4XPEN L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM20     19 26 7 9903 MHS4XPEN L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM21     7 4 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM22     7 26 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM23     21 18 20 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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MM24     20 26 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM25     9903 18 21 9903 MHS4XPEN L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM26     9903 26 21 9903 MHS4XPEN L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM43     9903 4 22 9903 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     22 21 17 9903 MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     17 4 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM46     17 21 9901 9901 MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     9903 4 23 9903 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     23 21 14 9903 MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     14 4 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM58     14 21 9901 9901 MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
RR9      9903 12 10K
QQ6      15 14 16 DE283ASN
XD5      16 9902 9901 DB3002AN
XD6      16 9902 9901 DB3002AN
XD7      16 9902 9901 DB3002AN
XD8      16 9902 9901 DB3002AN
QQ7      9952 6 9901 DE283ASN
QQ8      9952 6 9901 DE283ASN
QQ9      9952 6 9901 DE283ASN
QQ14     9917 9901 9901 ESDXXXXN
QQ15     26 9901 9901 ESDXXXXN
QQ16     9902 9901 9901 ESDXXXXN
M3M1   9903 9912 25 9903 MHS4XPEN L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3M2   25 9912 9901 9901 MHS4XNEN L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3M3   26 25 9901 9901 MHS4XNEN L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3M4   9903 25 26 9903 MHS4XPEN L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
XD15     24 1 9901 DB0814AN
XD16     11 24 9901 DB0814AN
RR13     9901 9912 10MEG
.ENDS A162441N
* Philips Semiconductors - ABT162451N
.SUBCKT A162451N  9912 9917 9902 9903 9901
MM1      1 28 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM2      3 4 2 9903 MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM3      1 4 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 28 9901 9901 MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
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MM6      6 4 9901 9901 MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM7      5 7 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM8      8 7 9 9901 MHS4XNEN L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
MM9      9 7 6 9901 MHS4XNEN L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
MM10     9902 7 10 9901 MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM11     10 7 9901 9901 MHS4XNEN L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM12     2 28 11 9903 MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM13     12 5 3 9903 MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM14     9903 7 5 9903 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
QQ1      9903 11 6 DA0ACBSN
QQ2      11 11 13 DA06CBSN
QQ3      9952 6 9901 DE283ASN
RR22     9902 9952 22.5
QQ4      15 14 16 DE283ASN
XQ5      15 17 14 9901 DB14CASN
MM15     9903 9908 18 9903 MHS4XPEN L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM16     9903 18 4 9903 MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM17     18 9908 9901 9901 MHS4XNEN L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
MM18     4 18 9901 9901 MHS4XNEN L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
XD1      13 9952 9901 DB0308AN
RR7      6 9901 1K
XD2      9902 8 9901 DB0814AN
XD3      16 9902 9901 DB3002AN
RR8      9903 15 15
MM19     9903 4 19 9903 MHS4XPEN L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM20     19 28 7 9903 MHS4XPEN L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM21     7 4 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM22     7 28 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM23     20 18 21 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM24     21 28 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM25     9903 18 20 9903 MHS4XPEN L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM26     9903 28 20 9903 MHS4XPEN L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM43     9903 4 22 9903 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     22 20 17 9903 MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     17 4 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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MM46     17 20 9901 9901 MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     9903 4 23 9903 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     23 20 14 9903 MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     14 4 9901 9901 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM58     14 20 9901 9901 MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
RR9      9903 12 10K
QQ6      15 14 16 DE283ASN
XD5      16 9902 9901 DB3002AN
XD6      16 9902 9901 DB3002AN
XD7      16 9902 9901 DB3002AN
XD8      16 9902 9901 DB3002AN
QQ7      9952 6 9901 DE283ASN
QQ8      9952 6 9901 DE283ASN
QQ9      9952 6 9901 DE283ASN
XD9      9901 28 9901 DB3002AN
XD10     9901 28 9901 DB3002AN
XD11     9901 28 9901 DB3002AN
XD12     9901 28 9901 DB3002AN
XD13     9901 28 9901 DB3002AN
MM60     28 9901 9901 9901 MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
XD14     28 9903 9901 DB0814AN
QQ10     24 9901 9901 DE283ASN
QQ11     24 9901 9901 DE283ASN
QQ12     24 9901 9901 DE283ASN
QQ13     24 9901 9901 DE283ASN
RR11     28 24 22.5
QQ14     9908 9901 9901 ESDXXXXN
QQ15     28 9901 9901 ESDXXXXN
QQ16     9902 9901 9901 ESDXXXXN
MM61     9903 9902 25 9903 MHS4XPEN L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
MM62     25 9902 9901 9901 MHS4XNEN L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
XD15     11 26 9901 DB0814AN
XD16     26 1 9901 DB0814AN
M3M1   9903 9912 27 9903 MHS4XPEN L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3M2   27 9912 9901 9901 MHS4XNEN L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3M3   28 27 9901 9901 MHS4XNEN L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3M4   9903 27 28 9903 MHS4XPEN L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.ENDS A162451N
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A16FASBS.LIB Subcircuit

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*****************************************************************************
* ABT16 BERKELEY SPICE SUBCIRCUIT LIBRARY
* A16FASBS.LIB
* FAST PROCESS CORNER
* STANDARD LOGIC PRODUCT GROUP
* PHILIPS SEMICONDUCTORS
* 3/31/1995
*****************************************************************************
.SUBCKT INV1 D E Q VCC
* USE THIS MODEL FOR ABT16240 (INVERTING PART)
*    IN   OUT   INTVCC   INTGND    (ENABLE)
X1   3     90     99        6           INBUFFF
*    IN   OUT   INTVCC   INTGND    (SIGNAL)
X2   1     91     99        6           MOSINVF
*    D    EN    OUT    INTVCC   INTGND
X3   91    90     2       99        6      OUTBUFFF
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1
*
.SUBCKT INV1_1 D E Q VCC
* USE THIS MODEL FOR ABT16240-1 (INVERTING PART)
*    IN   OUT   INTVCC   INTGND    (ENABLE)
X1   3     90     99        6           INBUFFF
*    IN   OUT   INTVCC   INTGND    (SIGNAL)
X2   1     91     99        6           MOSINVF
*    D    EN    OUT    INTVCC   INTGND
X3   91    90     2       99        6      OUTBUF1F
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1_1
.SUBCKT INV2 D E Q VCC
*
*    IN   OUT   INTVCC   INTGND    (ENABLE)
X1   3     90     99        6           INBUFFF
*    IN   OUT   INTVCC   INTGND    (SIGNAL)
X2   1     91     99        6           MOSINVF
*    D    EN    OUT    INTVCC   INTGND
X3   91    90     2       99        6      OUTBUFFF
*    IN   OUT   INTVCC   INTGND
X4    2    1      99        6           BCKLOADF
```

```
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV2
.SUBCKT NINV D E Q VCC
* USE THIS MODEL FOR ABT16273  -373B  -374B  -541
*  -821  -823  -825  -827  -841  (NON-INVERTING)
*   IN  OUT  INTVCC  INTGND  (ENABLE)
X1  3    90    99       6         INBUFFF
*   IN  OUT  INTVCC  INTGND  (SIGNAL)
X2  1    91    99       6         INBUFFF
*   D    EN   OUT   INTVCC  INTGND
X3  91   90    2      99       6     OUTBUFFF
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINV
*
.SUBCKT NINVB D E Q VCC
* USE THIS MODEL FOR ABT16500  -501  -543  -646  -652  -899
* -952  -1543
*   IN  OUT  INTVCC  INTGND  (ENABLE)
X1  3    90    99       6         INBUFFF
*   IN  OUT  INTVCC  INTGND  (SIGNAL)
X2  1    91    99       6         INBUFFF
*   D    EN   OUT   INTVCC  INTGND
X3  91   90    2      99       6     OUTBUFFF
*   IN  OUT  INTVCC  INTGND
X4   2    1    99       6           BCKLOADF
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINVB
*
```

```
.SUBCKT A16244 D E Q VCC
* USE THIS MODEL FOR ABT16244A
*   D     EN    OUT    INTVCC   INTGND
X3  1      3     2        99       6     A16244F
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16244
*
.SUBCKT A16245 D E Q VCC
* USE THIS MODEL FOR ABT16245B
*   D     EN    OUT    INTVCC   INTGND
X3  1      3     2       99       6     A16245F
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16245
*
.SUBCKT A16244_1 D E Q VCC
* USE THIS MODEL FOR ABT16244-1
*   D     EN    OUT    INTVCC   INTGND
X3  1      3     2        99       6     A162441F
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16244_1
*
```

```
.SUBCKT A16245_1 D E Q VCC
* USE THIS MODEL FOR ABT16245A-1
*   D     EN    OUT    INTVCC   INTGND
X3  1      3     2       99       6      A162451F
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16245_1
*
* Philips Semiconductors - MOSINVF
.SUBCKT MOSINVF    9913 9902 9903 9901
MM1      9903 9913 1 9903 MHS4XPEF L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
MM2      1 9913 9901 9901 MHS4XNEF L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
MM3      9902 1 9901 9901 MHS4XNEF L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
MM4      9903 1 9902 9903 MHS4XPEF L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.ENDS MOSINVF
* Philips Semiconductors - INBUFFF
.SUBCKT INBUFFF    9913 9902 9903 9901
MM1      9902 9913 9901 9901 MHS4XNEF L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
MM2      9903 9913 1 9903 MHS4XPEF L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
QQ1      9913 9901 9901 ESDXXXXF
RR1      1 9902 100
.ENDS INBUFFF
* Philips Semiconductors - OUTBUFFF
.SUBCKT OUTBUFFF 9912 9917 9902 9903 9901
MM2      2 3 1 9903 MHS4XPEF L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
MM3      1 4 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 5 9901 9901 MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 9901 9901 MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM13     7 4 2 9903 MHS4XPEF L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
QQ1      9903 8 5 DA04CASF
QQ2      1 1 9 DA0ACBSF
QQ3      9902 6 9901 DE283ASF
QQ4      11 10 12 DE283ASF
XQ5      11 13 10 9901 DB14CASF
XD1      9 9902 9901 DB0814AF
RR7      6 9901 1K
XD3      12 9902 9901 DB3002AF
RR8      9903 11 15
```

```
MM43     9903 4 14 9903 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     14 9912 13 9903 MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     13 4 9901 9901 MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM46     13 9912 9901 9901 MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     9903 4 15 9903 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     15 9912 10 9903 MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     10 4 9901 9901 MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM58     10 9912 9901 9901 MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
RR9      9903 7 10K
QQ6      11 10 12 DE283ASF
XD5      12 9902 9901 DB3002AF
XD6      12 9902 9901 DB3002AF
XD7      12 9902 9901 DB3002AF
XD8      12 9902 9901 DB3002AF
QQ7      9902 6 9901 DE283ASF
QQ8      9902 6 9901 DE283ASF
QQ9      9902 6 9901 DE283ASF
MM61     9903 17 16 9903 MHS4XPEF L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
MM62     16 9917 18 9901 MHS4XNEF L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
MM63     18 9912 6 9901 MHS4XNEF L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
MM64     17 9902 9901 9901 MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM65     9903 9902 17 9903 MHS4XPEF L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
MM66     9902 9917 19 9901 MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM67     19 9912 9901 9901 MHS4XNEF L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM68     3 9912 9901 9901 MHS4XNEF L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
MM69     9903 9912 3 9903 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM70     8 9912 9901 9901 MHS4XNEF L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
MM71     9903 9912 8 9903 MHS4XPEF L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM72     5 9912 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM73     9903 9912 5 9903 MHS4XPEF L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
QQ14     9903 1 6 DA0ACBSF
QQ15     9902 9901 9901 ESDXXXXF
MM74     4 9917 9901 9901 MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM75     9903 9917 4 9903 MHS4XPEF L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
.ENDS OUTBUFFF
```

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* Philips Semiconductors - OUTBUF1F
.SUBCKT OUTBUF1F 9912 9917 9902 9903 9901
MM2     2 3 1 9903 MHS4XPEF L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
MM3     1 4 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4     1 5 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5     6 5 9901 9901 MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6     6 4 9901 9901 MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM13    7 4 2 9903 MHS4XPEF L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
QQ1     9903 8 5 DA04CASF
QQ2     1 1 9 DA0ACBSF
QQ3     9952 6 9901 DE283ASF
RR22    9902 9952 22.5
QQ4     11 10 12 DE283ASF
XQ5     11 13 10 9901 DB14CASF
XD1     9 9952 9901 DB0814AF
RR7     6 9901 1K
XD3     12 9902 9901 DB3002AF
RR8     9903 11 15
MM43    9903 4 14 9903 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44    14 9912 13 9903 MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45    13 4 9901 9901 MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM46    13 9912 9901 9901 MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55    9903 4 15 9903 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56    15 9912 10 9903 MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57    10 4 9901 9901 MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM58    10 9912 9901 9901 MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
RR9     9903 7 10K
QQ6     11 10 12 DE283ASF
XD5     12 9902 9901 DB3002AF
XD6     12 9902 9901 DB3002AF
XD7     12 9902 9901 DB3002AF
XD8     12 9902 9901 DB3002AF
QQ7     9952 6 9901 DE283ASF
QQ8     9952 6 9901 DE283ASF
QQ9     9952 6 9901 DE283ASF
MM61    9903 17 16 9903 MHS4XPEF L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
MM62    16 9917 18 9901 MHS4XNEF L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
MM63    18 9912 6 9901 MHS4XNEF L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
MM64    17 9902 9901 9901 MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
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MM65     9903 9902 17 9903 MHS4XPEF L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
MM66     9902 9917 19 9901 MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM67     19 9912 9901 9901 MHS4XNEF L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM68     3 9912 9901 9901 MHS4XNEF L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
MM69     9903 9912 3 9903 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM70     8 9912 9901 9901 MHS4XNEF L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
MM71     9903 9912 8 9903 MHS4XPEF L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM72     5 9912 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM73     9903 9912 5 9903 MHS4XPEF L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
QQ14     9903 1 6 DA0ACBSF
QQ15     9902 9901 9901 ESDXXXXF
MM74     4 9917 9901 9901 MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM75     9903 9917 4 9903 MHS4XPEF L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
.ENDS OUTBUF1F
* Philips Semiconductors - BCKLOADF
.SUBCKT BCKLOADF 9913 9902 9903 9901
XD9      9901 9913 9901 DB3002AF
XD10     9901 9913 9901 DB3002AF
XD11     9901 9913 9901 DB3002AF
XD12     9901 9913 9901 DB3002AF
XD13     9901 9913 9901 DB3002AF
MM60     9913 9901 9901 9901 MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
XD14     9913 9903 9901 DB0814AF
QQ10     9913 9901 9901 DE283ASF
QQ11     9913 9901 9901 DE283ASF
QQ12     9913 9901 9901 DE283ASF
QQ13     9913 9901 9901 DE283ASF
MM61     9903 9902 1 1 MHS4XPEF L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
MM62     1 9902 9901 9901 MHS4XNEF L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
.ENDS BCKLOADF
* Philips Semiconductors - BUSHLD1F
.SUBCKT BUSHLD1F 9921 9903 9901
XD1      1 2 9901 DB3002AF
QQ1      3 3 1 DE283ASF
RR1      2 9921 2K
RR2      9921 4 5K
MM4      4 5 9901 9901 MHS4XNEF L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
MM1      5 9921 9901 9901 MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM2      9903 9921 5 5 MHS4XPEF L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM3      9903 5 3 3 MHS4XPEF L=1.0U W=8.298U
+ AD=16.596P AS=16.596P PD=20.596U PS=20.596U NRD=0.241 NRS=0.241
.ENDS BUSHLD1F
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* Philips Semiconductors - ABT16244F
.SUBCKT A16244F   9912 9917 9902 9903 9901
MM1      1 26 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM2      3 4 2 9903 MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM3      1 4 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 26 9901 9901 MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 9901 9901 MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM7      5 7 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM8      9 7 8 9901 MHS4XNEF L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
MM9      8 7 6 9901 MHS4XNEF L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
MM10     9902 7 10 9901 MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM11     10 7 9901 9901 MHS4XNEF L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM12     2 26 11 9903 MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM13     12 5 3 9903 MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM14     9903 7 5 9903 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
QQ1      9903 11 6 DA0ACBSF
QQ2      11 11 13 DA06CBSF
QQ3      9902 6 9901 DE283ASF
QQ4      15 14 16 DE283ASF
XQ5      15 17 14 9901 DB14CASF
MM15     9903 9917 18 9903 MHS4XPEF L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM16     9903 18 4 9903 MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM17     18 9917 9901 9901 MHS4XNEF L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
MM18     4 18 9901 9901 MHS4XNEF L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
XD1      13 9902 9901 DB0308AF
RR7      6 9901 1K
XD2      9902 9 9901 DB0814AF
XD3      16 9902 9901 DB3002AF
RR8      9903 15 15
MM19     9903 4 19 9903 MHS4XPEF L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM20     19 26 7 9903 MHS4XPEF L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM21     7 4 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM22     7 26 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM23     21 18 20 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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MM24     20 26 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM25     9903 18 21 9903 MHS4XPEF L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM26     9903 26 21 9903 MHS4XPEF L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM43     9903 4 22 9903 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     22 21 17 9903 MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     17 4 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM46     17 21 9901 9901 MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     9903 4 23 9903 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     23 21 14 9903 MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     14 4 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM58     14 21 9901 9901 MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
RR9      9903 12 10K
QQ6      15 14 16 DE283ASF
XD5      16 9902 9901 DB3002AF
XD6      16 9902 9901 DB3002AF
XD7      16 9902 9901 DB3002AF
XD8      16 9902 9901 DB3002AF
QQ7      9902 6 9901 DE283ASF
QQ8      9902 6 9901 DE283ASF
QQ9      9902 6 9901 DE283ASF
QQ14     9917 9901 9901 ESDXXXXF
QQ15     26 9901 9901 ESDXXXXF
QQ16     9902 9901 9901 ESDXXXXF
M3M1   9903 9912 25 9903 MHS4XPEF L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3M2   25 9912 9901 9901 MHS4XNEF L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3M3   26 25 9901 9901 MHS4XNEF L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3M4   9903 25 26 9903 MHS4XPEF L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
XD15     24 1 9901 DB0814AF
XD16     11 24 9901 DB0814AF
RR13     9901 9912 10MEG
.ENDS A16244F
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* Philips Semiconductors - ABT16245F
.SUBCKT A16245F   9912 9917 9902 9903 9901
MM1     1 28 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM2     3 4 2 9903 MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM3     1 4 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4     1 5 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5     6 28 9901 9901 MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6     6 4 9901 9901 MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM7     5 7 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM8     8 7 9 9901 MHS4XNEF L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
MM9     9 7 6 9901 MHS4XNEF L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
MM10    9902 7 10 9901 MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM11    10 7 9901 9901 MHS4XNEF L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM12    2 28 11 9903 MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM13    12 5 3 9903 MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM14    9903 7 5 9903 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
QQ1     9903 11 6 DA0ACBSF
QQ2     11 11 13 DA06CBSF
QQ3     9902 6 9901 DE283ASF
QQ4     15 14 16 DE283ASF
XQ5     15 17 14 9901 DB14CASF
MM15    9903 9908 18 9903 MHS4XPEF L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM16    9903 18 4 9903 MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM17    18 9908 9901 9901 MHS4XNEF L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
MM18    4 18 9901 9901 MHS4XNEF L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
XD1     13 9902 9901 DB0308AF
RR7     6 9901 1K
XD2     9902 8 9901 DB0814AF
XD3     16 9902 9901 DB3002AF
RR8     9903 15 15
MM19    9903 4 19 9903 MHS4XPEF L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM20    19 28 7 9903 MHS4XPEF L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM21    7 4 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM22    7 28 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM23    20 18 21 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM24    21 28 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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MM25     9903 18 20 9903 MHS4XPEF L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM26     9903 28 20 9903 MHS4XPEF L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM43     9903 4 22 9903 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     22 20 17 9903 MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     17 4 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM46     17 20 9901 9901 MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     9903 4 23 9903 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     23 20 14 9903 MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     14 4 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM58     14 20 9901 9901 MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
RR9      9903 12 10K
QQ6      15 14 16 DE283ASF
XD5      16 9902 9901 DB3002AF
XD6      16 9902 9901 DB3002AF
XD7      16 9902 9901 DB3002AF
XD8      16 9902 9901 DB3002AF
QQ7      9902 6 9901 DE283ASF
QQ8      9902 6 9901 DE283ASF
QQ9      9902 6 9901 DE283ASF
XD9      9901 28 9901 DB3002AF
XD10     9901 28 9901 DB3002AF
XD11     9901 28 9901 DB3002AF
XD12     9901 28 9901 DB3002AF
XD13     9901 28 9901 DB3002AF
MM60     28 9901 9901 9901 MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
XD14     28 9903 9901 DB0814AF
QQ10     24 9901 9901 DE283ASF
QQ11     24 9901 9901 DE283ASF
QQ12     24 9901 9901 DE283ASF
QQ13     24 9901 9901 DE283ASF
RR11     28 24 22.5
QQ14     9908 9901 9901 ESDXXXXF
QQ15     28 9901 9901 ESDXXXXF
QQ16     9902 9901 9901 ESDXXXXF
MM61     9903 9902 25 9903 MHS4XPEF L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
MM62     25 9902 9901 9901 MHS4XNEF L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
XD15     11 26 9901 DB0814AF
XD16     26 1 9901 DB0814AF
M3M1   9903 9912 27 9903 MHS4XPEF L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3M2   27 9912 9901 9901 MHS4XNEF L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3M3   28 27 9901 9901 MHS4XNEF L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3M4   9903 27 28 9903 MHS4XPEF L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.ENDS A16245F
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* Philips Semiconductors - ABT162441F
.SUBCKT A162441F  9912 9917 9902 9903 9901
MM1     1 26 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM2     3 4 2 9903 MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM3     1 4 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4     1 5 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5     6 26 9901 9901 MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6     6 4 9901 9901 MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM7     5 7 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM8     9 7 8 9901 MHS4XNEF L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
MM9     8 7 6 9901 MHS4XNEF L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
MM10    9902 7 10 9901 MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM11    10 7 9901 9901 MHS4XNEF L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM12    2 26 11 9903 MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM13    12 5 3 9903 MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM14    9903 7 5 9903 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
QQ1     9903 11 6 DA0ACBSF
QQ2     11 11 13 DA06CBSF
QQ3     9952 6 9901 DE283ASF
RR22    9902 9952 22.5
QQ4     15 14 16 DE283ASF
XQ5     15 17 14 9901 DB14CASF
MM15    9903 9917 18 9903 MHS4XPEF L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM16    9903 18 4 9903 MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM17    18 9917 9901 9901 MHS4XNEF L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
MM18    4 18 9901 9901 MHS4XNEF L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
XD1     13 9952 9901 DB0308AF
RR7     6 9901 1K
XD2     9902 9 9901 DB0814AF
XD3     16 9902 9901 DB3002AF
RR8     9903 15 15
MM19    9903 4 19 9903 MHS4XPEF L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM20    19 26 7 9903 MHS4XPEF L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM21    7 4 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM22    7 26 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM23    21 18 20 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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MM24     20 26 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM25     9903 18 21 9903 MHS4XPEF L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM26     9903 26 21 9903 MHS4XPEF L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM43     9903 4 22 9903 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     22 21 17 9903 MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     17 4 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM46     17 21 9901 9901 MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     9903 4 23 9903 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     23 21 14 9903 MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     14 4 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM58     14 21 9901 9901 MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
RR9      9903 12 10K
QQ6      15 14 16 DE283ASF
XD5      16 9902 9901 DB3002AF
XD6      16 9902 9901 DB3002AF
XD7      16 9902 9901 DB3002AF
XD8      16 9902 9901 DB3002AF
QQ7      9952 6 9901 DE283ASF
QQ8      9952 6 9901 DE283ASF
QQ9      9952 6 9901 DE283ASF
QQ14     9917 9901 9901 ESDXXXXF
QQ15     26 9901 9901 ESDXXXXF
QQ16     9902 9901 9901 ESDXXXXF
M3M1   9903 9912 25 9903 MHS4XPEF L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3M2   25 9912 9901 9901 MHS4XNEF L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3M3   26 25 9901 9901 MHS4XNEF L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3M4   9903 25 26 9903 MHS4XPEF L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
XD15     24 1 9901 DB0814AF
XD16     11 24 9901 DB0814AF
RR13     9901 9912 10MEG
.ENDS A162441F
```

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* Philips Semiconductors - ABT162451F
.SUBCKT A162451F  9912 9917 9902 9903 9901
MM1      1 28 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM2      3 4 2 9903 MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM3      1 4 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 28 9901 9901 MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 9901 9901 MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM7      5 7 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM8      8 7 9 9901 MHS4XNEF L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
MM9      9 7 6 9901 MHS4XNEF L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
MM10     9902 7 10 9901 MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM11     10 7 9901 9901 MHS4XNEF L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM12     2 28 11 9903 MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM13     12 5 3 9903 MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM14     9903 7 5 9903 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
QQ1      9903 11 6 DA0ACBSF
QQ2      11 11 13 DA06CBSF
QQ3      9952 6 9901 DE283ASF
RR22     9902 9952 22.5
QQ4      15 14 16 DE283ASF
XQ5      15 17 14 9901 DB14CASF
MM15     9903 9908 18 9903 MHS4XPEF L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM16     9903 18 4 9903 MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM17     18 9908 9901 9901 MHS4XNEF L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
MM18     4 18 9901 9901 MHS4XNEF L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
XD1      13 9952 9901 DB0308AF
RR7      6 9901 1K
XD2      9902 8 9901 DB0814AF
XD3      16 9902 9901 DB3002AF
RR8      9903 15 15
MM19     9903 4 19 9903 MHS4XPEF L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM20     19 28 7 9903 MHS4XPEF L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM21     7 4 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM22     7 28 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM23     20 18 21 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM24     21 28 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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MM25     9903 18 20 9903 MHS4XPEF L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM26     9903 28 20 9903 MHS4XPEF L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM43     9903 4 22 9903 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     22 20 17 9903 MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     17 4 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM46     17 20 9901 9901 MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     9903 4 23 9903 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     23 20 14 9903 MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     14 4 9901 9901 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM58     14 20 9901 9901 MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
RR9      9903 12 10K
QQ6      15 14 16 DE283ASF
XD5      16 9902 9901 DB3002AF
XD6      16 9902 9901 DB3002AF
XD7      16 9902 9901 DB3002AF
XD8      16 9902 9901 DB3002AF
QQ7      9952 6 9901 DE283ASF
QQ8      9952 6 9901 DE283ASF
QQ9      9952 6 9901 DE283ASF
XD9      9901 28 9901 DB3002AF
XD10     9901 28 9901 DB3002AF
XD11     9901 28 9901 DB3002AF
XD12     9901 28 9901 DB3002AF
XD13     9901 28 9901 DB3002AF
MM60     28 9901 9901 9901 MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
XD14     28 9903 9901 DB0814AF
QQ10     24 9901 9901 DE283ASF
QQ11     24 9901 9901 DE283ASF
QQ12     24 9901 9901 DE283ASF
QQ13     24 9901 9901 DE283ASF
RR11     28 24 22.5
QQ14     9908 9901 9901 ESDXXXXF
QQ15     28 9901 9901 ESDXXXXF
QQ16     9902 9901 9901 ESDXXXXF
MM61     9903 9902 25 9903 MHS4XPEF L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
MM62     25 9902 9901 9901 MHS4XNEF L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
XD15     11 26 9901 DB0814AF
XD16     26 1 9901 DB0814AF
M3M1   9903 9912 27 9903 MHS4XPEF L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3M2   27 9912 9901 9901 MHS4XNEF L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3M3   28 27 9901 9901 MHS4XNEF L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3M4   9903 27 28 9903 MHS4XPEF L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.ENDS A162451F
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A16SLOBS.LIB Subcircuit

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*****************************************************************************
* ABT16 BERKELEY SPICE SUBCIRCUIT LIBRARY
* A16SLOBS.LIB
* SLOW PROCESS CORNER
* STANDARD LOGIC PRODUCT GROUP
* PHILIPS SEMICONDUCTORS
* 3/31/1995
*****************************************************************************
.SUBCKT INV1 D E Q VCC
* USE THIS MODEL FOR ABT16240 (INVERTING PART)
*   IN  OUT  INTVCC  INTGND   (ENABLE)
X1  3    90    99       6          INBUFFS
*   IN  OUT  INTVCC  INTGND   (SIGNAL)
X2  1    91    99       6          MOSINVS
*   D    EN   OUT   INTVCC  INTGND
X3  91   90    2      99       6     OUTBUFFS
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1
*
.SUBCKT INV1_1 D E Q VCC
* USE THIS MODEL FOR ABT16240-1 (INVERTING PART)
*   IN  OUT  INTVCC  INTGND   (ENABLE)
X1  3    90    99       6          INBUFFS
*   IN  OUT  INTVCC  INTGND   (SIGNAL)
X2  1    91    99       6          MOSINVS
*   D    EN   OUT   INTVCC  INTGND
X3  91   90    2      99       6     OUTBUF1S
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1_1
.SUBCKT INV2 D E Q VCC
*
*   IN  OUT  INTVCC  INTGND   (ENABLE)
X1  3    90    99       6          INBUFFS
*   IN  OUT  INTVCC  INTGND   (SIGNAL)
X2  1    91    99       6          MOSINVS
*   D    EN   OUT   INTVCC  INTGND
X3  91   90    2      99       6     OUTBUFFS
*   IN  OUT  INTVCC  INTGND
X4   2   1     99       6          BCKLOADS
```

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*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV2
.SUBCKT NINV D E Q VCC
* USE THIS MODEL FOR ABT16273  -373B  -374B  -541
*  -821  -823  -825  -827  -841  (NON-INVERTING)
*   IN  OUT  INTVCC  INTGND  (ENABLE)
X1  3    90    99       6         INBUFFS
*   IN  OUT  INTVCC  INTGND  (SIGNAL)
X2  1    91    99       6         INBUFFS
*   D    EN   OUT   INTVCC  INTGND
X3  91   90    2      99       6     OUTBUFFS
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINV
*
.SUBCKT NINVB D E Q VCC
* USE THIS MODEL FOR ABT16500  -501  -543  -646  -652  -899
* -952  -1543
*   IN  OUT  INTVCC  INTGND  (ENABLE)
X1  3    90    99       6         INBUFFS
*   IN  OUT  INTVCC  INTGND  (SIGNAL)
X2  1    91    99       6         INBUFFS
*   D    EN   OUT   INTVCC  INTGND
X3  91   90    2      99       6     OUTBUFFS
*   IN  OUT  INTVCC  INTGND
X4   2    1    99       6         BCKLOADS
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINVB
*
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.SUBCKT A16244 D E Q VCC
* USE THIS MODEL FOR ABT16244A
*   D     EN    OUT    INTVCC   INTGND
X3  1      3     2        99       6      A16244S
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16244
*
.SUBCKT A16245 D E Q VCC
* USE THIS MODEL FOR ABT16245B
*   D     EN    OUT    INTVCC   INTGND
X3  1      3     2        99       6      A16245S
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16245
*
.SUBCKT A16244_1 D E Q VCC
* USE THIS MODEL FOR ABT16244-1
*   D     EN    OUT    INTVCC   INTGND
X3  1      3     2        99       6      A162441S
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16244_1
*
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```
.SUBCKT A16245_1 D E Q VCC
* USE THIS MODEL FOR ABT16245A-1
*   D     EN    OUT    INTVCC   INTGND
X3  1      3     2       99       6      A162451S
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16245_1
*
* Philips Semiconductors - MOSINVS
.SUBCKT MOSINVS   9913 9902 9903 9901
MM1      9903 9913 1 9903 MHS4XPES L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
MM2      1 9913 9901 9901 MHS4XNES L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
MM3      9902 1 9901 9901 MHS4XNES L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
MM4      9903 1 9902 9903 MHS4XPES L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.ENDS MOSINVS
* Philips Semiconductors - INBUFFS
.SUBCKT INBUFFS   9913 9902 9903 9901
MM1      9902 9913 9901 9901 MHS4XNES L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
MM2      9903 9913 1 9903 MHS4XPES L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
QQ1      9913 9901 9901 ESDXXXXS
RR1      1 9902 100
.ENDS INBUFFS
* Philips Semiconductors - OUTBUFFS
.SUBCKT OUTBUFFS 9912 9917 9902 9903 9901
MM2      2 3 1 9903 MHS4XPES L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
MM3      1 4 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 5 9901 9901 MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 9901 9901 MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM13     7 4 2 9903 MHS4XPES L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
QQ1      9903 8 5 DA04CASS
QQ2      1 1 9 DA0ACBSS
QQ3      9902 6 9901 DE283ASS
QQ4      11 10 12 DE283ASS
XQ5      11 13 10 9901 DB14CASS
XD1      9 9902 9901 DB0814AS
RR7      6 9901 1K
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XD3      12 9902 9901 DB3002AS
RR8      9903 11 15
MM43     9903 4 14 9903 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     14 9912 13 9903 MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     13 4 9901 9901 MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM46     13 9912 9901 9901 MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     9903 4 15 9903 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     15 9912 10 9903 MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     10 4 9901 9901 MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM58     10 9912 9901 9901 MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
RR9      9903 7 10K
QQ6      11 10 12 DE283ASS
XD5      12 9902 9901 DB3002AS
XD6      12 9902 9901 DB3002AS
XD7      12 9902 9901 DB3002AS
XD8      12 9902 9901 DB3002AS
QQ7      9902 6 9901 DE283ASS
QQ8      9902 6 9901 DE283ASS
QQ9      9902 6 9901 DE283ASS
MM61     9903 17 16 9903 MHS4XPES L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
MM62     16 9917 18 9901 MHS4XNES L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
MM63     18 9912 6 9901 MHS4XNES L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
MM64     17 9902 9901 9901 MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM65     9903 9902 17 9903 MHS4XPES L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
MM66     9902 9917 19 9901 MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM67     19 9912 9901 9901 MHS4XNES L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM68     3 9912 9901 9901 MHS4XNES L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
MM69     9903 9912 3 9903 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM70     8 9912 9901 9901 MHS4XNES L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
MM71     9903 9912 8 9903 MHS4XPES L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM72     5 9912 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM73     9903 9912 5 9903 MHS4XPES L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
QQ14     9903 1 6 DA0ACBSS
QQ15     9902 9901 9901 ESDXXXXS
MM74     4 9917 9901 9901 MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM75     9903 9917 4 9903 MHS4XPES L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
.ENDS OUTBUFFS
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* Philips Semiconductors - OUTBUF1S
.SUBCKT OUTBUF1S 9912 9917 9902 9903 9901
MM2     2 3 1 9903 MHS4XPES L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
MM3     1 4 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4     1 5 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5     6 5 9901 9901 MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6     6 4 9901 9901 MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM13    7 4 2 9903 MHS4XPES L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
QQ1     9903 8 5 DA04CASS
QQ2     1 1 9 DA0ACBSS
QQ3     9952 6 9901 DE283ASS
RR22    9902 9952 22.5
QQ4     11 10 12 DE283ASS
XQ5     11 13 10 9901 DB14CASS
XD1     9 9952 9901 DB0814AS
RR7     6 9901 1K
XD3     12 9902 9901 DB3002AS
RR8     9903 11 15
MM43    9903 4 14 9903 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44    14 9912 13 9903 MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45    13 4 9901 9901 MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM46    13 9912 9901 9901 MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55    9903 4 15 9903 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56    15 9912 10 9903 MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57    10 4 9901 9901 MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM58    10 9912 9901 9901 MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
RR9     9903 7 10K
QQ6     11 10 12 DE283ASS
XD5     12 9902 9901 DB3002AS
XD6     12 9902 9901 DB3002AS
XD7     12 9902 9901 DB3002AS
XD8     12 9902 9901 DB3002AS
QQ7     9952 6 9901 DE283ASS
QQ8     9952 6 9901 DE283ASS
QQ9     9952 6 9901 DE283ASS
MM61    9903 17 16 9903 MHS4XPES L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
MM62    16 9917 18 9901 MHS4XNES L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
MM63    18 9912 6 9901 MHS4XNES L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
MM64    17 9902 9901 9901 MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM65    9903 9902 17 9903 MHS4XPES L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
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MM66     9902 9917 19 9901 MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM67     19 9912 9901 9901 MHS4XNES L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM68     3 9912 9901 9901 MHS4XNES L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
MM69     9903 9912 3 9903 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM70     8 9912 9901 9901 MHS4XNES L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
MM71     9903 9912 8 9903 MHS4XPES L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM72     5 9912 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM73     9903 9912 5 9903 MHS4XPES L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
QQ14     9903 1 6 DA0ACBSS
QQ15     9902 9901 9901 ESDXXXXS
MM74     4 9917 9901 9901 MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM75     9903 9917 4 9903 MHS4XPES L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
.ENDS OUTBUF1S
* Philips Semiconductors - BCKLOADS
.SUBCKT BCKLOADS 9913 9902 9903 9901
XD9      9901 9913 9901 DB3002AS
XD10     9901 9913 9901 DB3002AS
XD11     9901 9913 9901 DB3002AS
XD12     9901 9913 9901 DB3002AS
XD13     9901 9913 9901 DB3002AS
MM60     9913 9901 9901 9901 MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
XD14     9913 9903 9901 DB0814AS
QQ10     9913 9901 9901 DE283ASS
QQ11     9913 9901 9901 DE283ASS
QQ12     9913 9901 9901 DE283ASS
QQ13     9913 9901 9901 DE283ASS
MM61     9903 9902 1 1 MHS4XPES L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
MM62     1 9902 9901 9901 MHS4XNES L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
.ENDS BCKLOADS
* Philips Semiconductors - BUSHLD1S
.SUBCKT BUSHLD1S 9921 9903 9901
XD1      1 2 9901 DB3002AS
QQ1      3 3 1 DE283ASS
RR1      2 9921 2K
RR2      9921 4 5K
MM4      4 5 9901 9901 MHS4XNES L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
MM1      5 9921 9901 9901 MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM2      9903 9921 5 5 MHS4XPES L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM3      9903 5 3 3 MHS4XPES L=1.0U W=8.298U
+ AD=16.596P AS=16.596P PD=20.596U PS=20.596U NRD=0.241 NRS=0.241
.ENDS BUSHLD1S
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* Philips Semiconductors - ABT16244S
.SUBCKT A16244S   9912 9917 9902 9903 9901
MM1      1 26 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM2      3 4 2 9903 MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM3      1 4 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 26 9901 9901 MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 9901 9901 MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM7      5 7 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM8      9 7 8 9901 MHS4XNES L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
MM9      8 7 6 9901 MHS4XNES L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
MM10     9902 7 10 9901 MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM11     10 7 9901 9901 MHS4XNES L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM12     2 26 11 9903 MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM13     12 5 3 9903 MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM14     9903 7 5 9903 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
QQ1      9903 11 6 DA0ACBSS
QQ2      11 11 13 DA06CBSS
QQ3      9902 6 9901 DE283ASS
QQ4      15 14 16 DE283ASS
XQ5      15 17 14 9901 DB14CASS
MM15     9903 9917 18 9903 MHS4XPES L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM16     9903 18 4 9903 MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM17     18 9917 9901 9901 MHS4XNES L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
MM18     4 18 9901 9901 MHS4XNES L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
XD1      13 9902 9901 DB0308AS
RR7      6 9901 1K
XD2      9902 9 9901 DB0814AS
XD3      16 9902 9901 DB3002AS
RR8      9903 15 15
MM19     9903 4 19 9903 MHS4XPES L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM20     19 26 7 9903 MHS4XPES L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM21     7 4 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM22     7 26 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM23     21 18 20 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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MM24     20 26 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM25     9903 18 21 9903 MHS4XPES L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM26     9903 26 21 9903 MHS4XPES L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM43     9903 4 22 9903 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     22 21 17 9903 MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     17 4 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM46     17 21 9901 9901 MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     9903 4 23 9903 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     23 21 14 9903 MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     14 4 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM58     14 21 9901 9901 MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
RR9      9903 12 10K
QQ6      15 14 16 DE283ASS
XD5      16 9902 9901 DB3002AS
XD6      16 9902 9901 DB3002AS
XD7      16 9902 9901 DB3002AS
XD8      16 9902 9901 DB3002AS
QQ7      9902 6 9901 DE283ASS
QQ8      9902 6 9901 DE283ASS
QQ9      9902 6 9901 DE283ASS
QQ14     9917 9901 9901 ESDXXXXS
QQ15     26 9901 9901 ESDXXXXS
QQ16     9902 9901 9901 ESDXXXXS
M3M1   9903 9912 25 9903 MHS4XPES L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3M2   25 9912 9901 9901 MHS4XNES L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3M3   26 25 9901 9901 MHS4XNES L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3M4   9903 25 26 9903 MHS4XPES L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
XD15     24 1 9901 DB0814AS
XD16     11 24 9901 DB0814AS
RR13     9901 9912 10MEG
.ENDS A16244S
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* Philips Semiconductors - ABT16245S
.SUBCKT A16245S   9912 9917 9902 9903 9901
MM1      1 28 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM2      3 4 2 9903 MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM3      1 4 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 28 9901 9901 MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 9901 9901 MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM7      5 7 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM8      8 7 9 9901 MHS4XNES L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
MM9      9 7 6 9901 MHS4XNES L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
MM10     9902 7 10 9901 MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM11     10 7 9901 9901 MHS4XNES L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM12     2 28 11 9903 MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM13     12 5 3 9903 MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM14     9903 7 5 9903 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
QQ1      9903 11 6 DA0ACBSS
QQ2      11 11 13 DA06CBSS
QQ3      9902 6 9901 DE283ASS
QQ4      15 14 16 DE283ASS
XQ5      15 17 14 9901 DB14CASS
MM15     9903 9908 18 9903 MHS4XPES L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM16     9903 18 4 9903 MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM17     18 9908 9901 9901 MHS4XNES L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
MM18     4 18 9901 9901 MHS4XNES L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
XD1      13 9902 9901 DB0308AS
RR/      6 9901 1K
XD2      9902 8 9901 DB0814AS
XD3      16 9902 9901 DB3002AS
RR8      9903 15 15
MM19     9903 4 19 9903 MHS4XPES L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM20     19 28 7 9903 MHS4XPES L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM21     7 4 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM22     7 28 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM23     20 18 21 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM24     21 28 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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MM25     9903 18 20 9903 MHS4XPES L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM26     9903 28 20 9903 MHS4XPES L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM43     9903 4 22 9903 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     22 20 17 9903 MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     17 4 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM46     17 20 9901 9901 MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     9903 4 23 9903 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     23 20 14 9903 MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     14 4 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM58     14 20 9901 9901 MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
RR9      9903 12 10K
QQ6      15 14 16 DE283ASS
XD5      16 9902 9901 DB3002AS
XD6      16 9902 9901 DB3002AS
XD7      16 9902 9901 DB3002AS
XD8      16 9902 9901 DB3002AS
QQ7      9902 6 9901 DE283ASS
QQ8      9902 6 9901 DE283ASS
QQ9      9902 6 9901 DE283ASS
XD9      9901 28 9901 DB3002AS
XD10     9901 28 9901 DB3002AS
XD11     9901 28 9901 DB3002AS
XD12     9901 28 9901 DB3002AS
XD13     9901 28 9901 DB3002AS
MM60     28 9901 9901 9901 MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
XD14     28 9903 9901 DB0814AS
QQ10     24 9901 9901 DE283ASS
QQ11     24 9901 9901 DE283ASS
QQ12     24 9901 9901 DE283ASS
QQ13     24 9901 9901 DE283ASS
RR11     28 24 22.5
QQ14     9908 9901 9901 ESDXXXXS
QQ15     28 9901 9901 ESDXXXXS
QQ16     9902 9901 9901 ESDXXXXS
MM61     9903 9902 25 9903 MHS4XPES L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
MM62     25 9902 9901 9901 MHS4XNES L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
XD15     11 26 9901 DB0814AS
XD16     26 1 9901 DB0814AS
M3M1   9903 9912 27 9903 MHS4XPES L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3M2   27 9912 9901 9901 MHS4XNES L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3M3   28 27 9901 9901 MHS4XNES L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3M4   9903 27 28 9903 MHS4XPES L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.ENDS A16245S
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* Philips Semiconductors - ABT162441S
.SUBCKT A162441S  9912 9917 9902 9903 9901
MM1      1 26 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM2      3 4 2 9903 MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM3      1 4 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 26 9901 9901 MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 9901 9901 MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM7      5 7 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM8      9 7 8 9901 MHS4XNES L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
MM9      8 7 6 9901 MHS4XNES L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
MM10     9902 7 10 9901 MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM11     10 7 9901 9901 MHS4XNES L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM12     2 26 11 9903 MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM13     12 5 3 9903 MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM14     9903 7 5 9903 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
QQ1      9903 11 6 DA0ACBSS
QQ2      11 11 13 DA06CBSS
QQ3      9952 6 9901 DE283ASS
RR22     9902 9952 22.5
QQ4      15 14 16 DE283ASS
XQ5      15 17 14 9901 DB14CASS
MM15     9903 9917 18 9903 MHS4XPES L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM16     9903 18 4 9903 MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM17     18 9917 9901 9901 MHS4XNES L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
MM18     4 18 9901 9901 MHS4XNES L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
XD1      13 9952 9901 DB0308AS
RR7      6 9901 1K
XD2      9902 9 9901 DB0814AS
XD3      16 9902 9901 DB3002AS
RR8      9903 15 15
MM19     9903 4 19 9903 MHS4XPES L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM20     19 26 7 9903 MHS4XPES L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM21     7 4 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM22     7 26 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM23     21 18 20 9901 MHS4XNES L=1.0U W=19.926U
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+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM24     20 26 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM25     9903 18 21 9903 MHS4XPES L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM26     9903 26 21 9903 MHS4XPES L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM43     9903 4 22 9903 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     22 21 17 9903 MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     17 4 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM46     17 21 9901 9901 MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     9903 4 23 9903 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     23 21 14 9903 MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     14 4 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM58     14 21 9901 9901 MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
RR9      9903 12 10K
QQ6      15 14 16 DE283ASS
XD5      16 9902 9901 DB3002AS
XD6      16 9902 9901 DB3002AS
XD7      16 9902 9901 DB3002AS
XD8      16 9902 9901 DB3002AS
QQ7      9952 6 9901 DE283ASS
QQ8      9952 6 9901 DE283ASS
QQ9      9952 6 9901 DE283ASS
QQ14     9917 9901 9901 ESDXXXXS
QQ15     26 9901 9901 ESDXXXXS
QQ16     9902 9901 9901 ESDXXXXS
M3M1  9903 9912 25 9903 MHS4XPES L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3M2  25 9912 9901 9901 MHS4XNES L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3M3  26 25 9901 9901 MHS4XNES L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3M4  9903 25 26 9903 MHS4XPES L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
XD15     24 1 9901 DB0814AS
XD16     11 24 9901 DB0814AS
RR13     9901 9912 10MEG
.ENDS A162441S
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* Philips Semiconductors - ABT162451S
.SUBCKT A162451S  9912 9917 9902 9903 9901
MM1      1 28 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM2      3 4 2 9903 MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM3      1 4 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 28 9901 9901 MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 9901 9901 MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM7      5 7 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM8      8 7 9 9901 MHS4XNES L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
MM9      9 7 6 9901 MHS4XNES L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
MM10     9902 7 10 9901 MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM11     10 7 9901 9901 MHS4XNES L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM12     2 28 11 9903 MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM13     12 5 3 9903 MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM14     9903 7 5 9903 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
QQ1      9903 11 6 DA0ACBSS
QQ2      11 11 13 DA06CBSS
QQ3      9952 6 9901 DE283ASS
RR22     9902 9952 22.5
QQ4      15 14 16 DE283ASS
XQ5      15 17 14 9901 DB14CASS
MM15     9903 9908 18 9903 MHS4XPES L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM16     9903 18 4 9903 MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM17     18 9908 9901 9901 MHS4XNES L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
MM18     4 18 9901 9901 MHS4XNES L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
XD1      13 9952 9901 DB0308AS
RR7      6 9901 1K
XD2      9902 8 9901 DB0814AS
XD3      16 9902 9901 DB3002AS
RR8      9903 15 15
MM19     9903 4 19 9903 MHS4XPES L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM20     19 28 7 9903 MHS4XPES L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM21     7 4 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM22     7 28 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM23     20 18 21 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM24     21 28 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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MM25     9903 18 20 9903 MHS4XPES L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM26     9903 28 20 9903 MHS4XPES L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM43     9903 4 22 9903 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     22 20 17 9903 MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     17 4 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM46     17 20 9901 9901 MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     9903 4 23 9903 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     23 20 14 9903 MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     14 4 9901 9901 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM58     14 20 9901 9901 MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
RR9      9903 12 10K
QQ6      15 14 16 DE283ASS
XD5      16 9902 9901 DB3002AS
XD6      16 9902 9901 DB3002AS
XD7      16 9902 9901 DB3002AS
XD8      16 9902 9901 DB3002AS
QQ7      9952 6 9901 DE283ASS
QQ8      9952 6 9901 DE283ASS
QQ9      9952 6 9901 DE283ASS
XD9      9901 28 9901 DB3002AS
XD10     9901 28 9901 DB3002AS
XD11     9901 28 9901 DB3002AS
XD12     9901 28 9901 DB3002AS
XD13     9901 28 9901 DB3002AS
MM60     28 9901 9901 9901 MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
XD14     28 9903 9901 DB0814AS
QQ10     24 9901 9901 DE283ASS
QQ11     24 9901 9901 DE283ASS
QQ12     24 9901 9901 DE283ASS
QQ13     24 9901 9901 DE283ASS
RR11     28 24 22.5
QQ14     9908 9901 9901 ESDXXXXS
QQ15     28 9901 9901 ESDXXXXS
QQ16     9902 9901 9901 ESDXXXXS
MM61     9903 9902 25 9903 MHS4XPES L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
MM62     25 9902 9901 9901 MHS4XNES L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
XD15     11 26 9901 DB0814AS
XD16     26 1 9901 DB0814AS
M3M1   9903 9912 27 9903 MHS4XPES L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3M2   27 9912 9901 9901 MHS4XNES L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3M3   28 27 9901 9901 MHS4XNES L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3M4   9903 27 28 9903 MHS4XPES L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.ENDS A162451S
```

A16NOMHS.LIB Subcircuit

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*******************************************************************************
* ABT16 HSPICE SUBCIRCUIT LIBRARY
* A16NOMHS.LIB
* NOMINAL PROCESS CORNER
* STANDARD LOGIC PRODUCT GROUP
* PHILIPS SEMICONDUCTORS
* 3/31/1995
*******************************************************************************
.SUBCKT INV1 D E Q VCC
* USE THIS MODEL FOR ABT16240 (INVERTING PART)
*    IN   OUT   INTVCC   INTGND    (ENABLE)
X1   3     90     99         6          INBUFFN
*    IN   OUT   INTVCC   INTGND    (SIGNAL)
X2   1     91     99         6          MOSINVN
*    D     EN    OUT    INTVCC   INTGND
X3   91    90     2       99         6      OUTBUFFN
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1
*
.SUBCKT INV1_1 D E Q VCC
* USE THIS MODEL FOR ABT16240-1 (INVERTING PART)
*    IN   OUT   INTVCC   INTGND    (ENABLE)
X1   3     90     99         6          INBUFFN
*    IN   OUT   INTVCC   INTGND    (SIGNAL)
X2   1     91     99         6          MOSINVN
*    D     EN    OUT    INTVCC   INTGND
X3   91    90     2       99         6      OUTBUF1N
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1_1
.SUBCKT INV2 D E Q VCC
*
*    IN   OUT   INTVCC   INTGND    (ENABLE)
X1   3     90     99         6          INBUFFN
*    IN   OUT   INTVCC   INTGND    (SIGNAL)
X2   1     91     99         6          MOSINVN
*    D     EN    OUT    INTVCC   INTGND
X3   91    90     2       99         6      OUTBUFFN
*    IN   OUT   INTVCC   INTGND
X4    2    1      99         6          BCKLOADN
```

```
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV2
.SUBCKT NINV D E Q VCC
* USE THIS MODEL FOR ABT16273  -373B  -374B  -541
*  -821  -823  -825  -827  -841  (NON-INVERTING)
*   IN  OUT  INTVCC  INTGND  (ENABLE)
X1  3    90    99       6          INBUFFN
*   IN  OUT  INTVCC  INTGND  (SIGNAL)
X2  1    91    99       6          INBUFFN
*   D    EN   OUT   INTVCC  INTGND
X3  91   90    2      99       6     OUTBUFFN
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINV
*
.SUBCKT NINVB D E Q VCC
* USE THIS MODEL FOR ABT16500  -501  -543  -646  -652  -899
* -952  -1543
*   IN  OUT  INTVCC  INTGND  (ENABLE)
X1  3    90    99       6          INBUFFN
*   IN  OUT  INTVCC  INTGND  (SIGNAL)
X2  1    91    99       6          INBUFFN
*   D    EN   OUT   INTVCC  INTGND
X3  91   90    2      99       6     OUTBUFFN
*   IN  OUT  INTVCC  INTGND
X4   2    1     99       6          BCKLOADN
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINVB
*
```

```
.SUBCKT A16244 D E Q VCC
* USE THIS MODEL FOR ABT16244A
*    D     EN    OUT    INTVCC   INTGND
X3   1      3     2        99       6      A16244N
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16244
*
.SUBCKT A16245 D E Q VCC
* USE THIS MODEL FOR ABT16245B
*    D     EN    OUT    INTVCC   INTGND
X3   1      3     2        99       6      A16245N
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16245
*
.SUBCKT A16244_1 D E Q VCC
* USE THIS MODEL FOR ABT16244-1
*    D     EN    OUT    INTVCC   INTGND
X3   1      3     2        99       6      A162441N
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16244_1
*
```

```
.SUBCKT A16245_1 D E Q VCC
* USE THIS MODEL FOR ABT16245A-1
*    D     EN    OUT    INTVCC   INTGND
X3   1      3     2       99       6      A162451N
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16245_1
*
*
** Philips Semiconductors - MOSINV
.MACRO MOSINVN IN OUT INTVCC INTGND
MM1      INTVCC IN 1 INTVCC MHS4XPEN L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
MM2      1 IN INTGND INTGND MHS4XNEN L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
MM3      OUT 1 INTGND INTGND MHS4XNEN L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
MM4      INTVCC 1 OUT INTVCC MHS4XPEN L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.EOM MOSINVN
* Philips Semiconductors - INBUFF
.MACRO INBUFFN IN OUT INTVCC INTGND
MM1      OUT IN INTGND INTGND MHS4XNEN L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
MM2      INTVCC IN 1 INTVCC MHS4XPEN L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
QQ1      IN INTGND INTGND ESDXXXXN
RR1      1 OUT 100
.EOM INBUFFN
* Philips Semiconductors - OUTBUFF
.MACRO OUTBUFFN   D EN OUT INTVCC INTGND
MM2      2 3 1 INTVCC MHS4XPEN L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
MM3      1 4 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 5 INTGND INTGND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 INTGND INTGND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM13     7 4 2 INTVCC MHS4XPEN L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
QQ1      INTVCC 8 5 DA04CASN
QQ2      1 1 9 DA0ACBSN
QQ3      OUT 6 INTGND DE283ASN
QQ4      11 10 12 DE283ASN
XQ5      11 13 10 INTGND DB14CASN
XD1      9 OUT INTGND DB0814AN
XR7      6 INTGND INTGND DC00400N  RES=1K
```

```
XD3      12 OUT INTGND DB3002AN
XR8      INTVCC 11 INTGND DB01E00N  RES=15
MM43     INTVCC 4 14 INTVCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     14 D 13 INTVCC MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     13 4 INTGND INTGND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM46     13 D INTGND INTGND MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     INTVCC 4 15 INTVCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     15 D 10 INTVCC MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     10 4 INTGND INTGND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM58     10 D INTGND INTGND MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
XR9      INTVCC 7 INTGND DC00400N  RES=10K
QQ6      11 10 12 DE283ASN
XD5      12 OUT INTGND DB3002AN
XD6      12 OUT INTGND DB3002AN
XD7      12 OUT INTGND DB3002AN
XD8      12 OUT INTGND DB3002AN
QQ7      OUT 6 INTGND DE283ASN
QQ8      OUT 6 INTGND DE283ASN
QQ9      OUT 6 INTGND DE283ASN
MM61     INTVCC 17 16 INTVCC MHS4XPEN L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
MM62     16 EN 18 INTGND MHS4XNEN L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
MM63     18 D 6 INTGND MHS4XNEN L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
MM64     17 OUT INTGND INTGND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM65     INTVCC OUT 17 INTVCC MHS4XPEN L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
MM66     OUT EN 19 INTGND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM67     19 D INTGND INTGND MHS4XNEN L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM68     3 D INTGND INTGND MHS4XNEN L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
MM69     INTVCC D 3 INTVCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM70     8 D INTGND INTGND MHS4XNEN L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
MM71     INTVCC D 8 INTVCC MHS4XPEN L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM72     5 D INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM73     INTVCC D 5 INTVCC MHS4XPEN L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
QQ14     INTVCC 1 6 DA0ACBSN
QQ15     OUT INTGND INTGND ESDXXXXN
MM74     4 EN INTGND INTGND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM75     INTVCC EN 4 INTVCC MHS4XPEN L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
.EOM OUTBUFFN
```

```
* Philips Semiconductors - OUTBUF1
.MACRO OUTBUF1N   D EN OUT INTVCC INTGND
MM2     2 3 1 INTVCC MHS4XPEN L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
MM3     1 4 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4     1 5 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5     6 5 INTGND INTGND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6     6 4 INTGND INTGND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM13    7 4 2 INTVCC MHS4XPEN L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
QQ1     INTVCC 8 5 DA04CASN
QQ2     1 1 9 DA0ACBSN
QQ3     OUTA 6 INTGND DE283ASN
RR20    OUT OUTA 22.5
QQ4     11 10 12 DE283ASN
XQ5     11 13 10 INTGND DB14CASN
XD1     9 OUTA INTGND DB0814AN
XR7     6 INTGND INTGND DC00400N  RES=1K
XD3     12 OUT INTGND DB3002AN
XR8     INTVCC 11 INTGND DB01E00N  RES=15
MM43    INTVCC 4 14 INTVCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44    14 D 13 INTVCC MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45    13 4 INTGND INTGND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM46    13 D INTGND INTGND MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55    INTVCC 4 15 INTVCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56    15 D 10 INTVCC MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57    10 4 INTGND INTGND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM58    10 D INTGND INTGND MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
XR9     INTVCC 7 INTGND DC00400N  RES=10K
QQ6     11 10 12 DE283ASN
XD5     12 OUT INTGND DB3002AN
XD6     12 OUT INTGND DB3002AN
XD7     12 OUT INTGND DB3002AN
XD8     12 OUT INTGND DB3002AN
QQ7     OUTA 6 INTGND DE283ASN
QQ8     OUTA 6 INTGND DE283ASN
QQ9     OUTA 6 INTGND DE283ASN
MM61    INTVCC 17 16 INTVCC MHS4XPEN L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
MM62    16 EN 18 INTGND MHS4XNEN L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
MM63    18 D 6 INTGND MHS4XNEN L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
MM64    17 OUT INTGND INTGND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
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```
MM65     INTVCC OUT 17 INTVCC MHS4XPEN L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
MM66     OUT EN 19 INTGND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM67     19 D INTGND INTGND MHS4XNEN L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM68     3 D INTGND INTGND MHS4XNEN L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
MM69     INTVCC D 3 INTVCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM70     8 D INTGND INTGND MHS4XNEN L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
MM71     INTVCC D 8 INTVCC MHS4XPEN L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM72     5 D INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM73     INTVCC D 5 INTVCC MHS4XPEN L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
QQ14     INTVCC 1 6 DA0ACBSN
QQ15     OUT INTGND INTGND ESDXXXXN
MM74     4 EN INTGND INTGND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM75     INTVCC EN 4 INTVCC MHS4XPEN L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
.EOM OUTBUF1N
* Philips Semiconductors - BCKLOAD
.MACRO BCKLOADN IN OUT INTVCC INTGND
XD9      INTGND IN INTGND DB3002AN
XD10     INTGND IN INTGND DB3002AN
XD11     INTGND IN INTGND DB3002AN
XD12     INTGND IN INTGND DB3002AN
XD13     INTGND IN INTGND DB3002AN
MM60     IN INTGND INTGND INTGND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
XD14     IN INTVCC INTGND DB0814AN
QQ10     IN INTGND INTGND DE283ASN
QQ11     IN INTGND INTGND DE283ASN
QQ12     IN INTGND INTGND DE283ASN
QQ13     IN INTGND INTGND DE283ASN
MM61     INTVCC OUT 1 1 MHS4XPEN L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
MM62     1 OUT INTGND INTGND MHS4XNEN L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
.EOM BCKLOADN
* Philips Semiconductors - BUSHLD1
.MACRO BUSHLD1N   BH INTVCC INTGND
XD1      1 2 INTGND DB3002AN
QQ1      3 3 1 DE283ASN
XR1      2 BH INTGND DC00400N  RES=2K
XR2      BH 4 INTGND DC00400N  RES=5K
MM4      4 5 INTGND INTGND MHS4XNEN L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
MM1      5 BH INTGND INTGND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM2      INTVCC BH 5 5 MHS4XPEN L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM3      INTVCC 5 3 3 MHS4XPEN L=1.0U W=8.298U
+ AD=16.596P AS=16.596P PD=20.596U PS=20.596U NRD=0.241 NRS=0.241
.EOM BUSHLD1N
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* Philips Semiconductors - ABT16244
.MACRO A16244N D EN OUT INTVCC INTGND
MM1      1 26 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM2      3 4 2 INTVCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM3      1 4 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 26 INTGND INTGND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 INTGND INTGND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM7      5 7 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM8      9 7 8 INTGND MHS4XNEN L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
MM9      8 7 6 INTGND MHS4XNEN L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
MM10     OUT 7 10 INTGND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM11     10 7 INTGND INTGND MHS4XNEN L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM12     2 26 11 INTVCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM13     12 5 3 INTVCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM14     INTVCC 7 5 INTVCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
QQ1      INTVCC 11 6 DA0ACBSN
QQ2      11 11 13 DA06CBSN
QQ3      OUT 6 INTGND DE283ASN
QQ4      15 14 16 DE283ASN
XQ5      15 17 14 INTGND DB14CASN
MM15     INTVCC OEBAR 18 INTVCC MHS4XPEN L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM16     INTVCC 18 4 INTVCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM17     18 OEBAR INTGND INTGND MHS4XNEN L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
MM18     4 18 INTGND INTGND MHS4XNEN L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
XD1      13 OUT INTGND DB0308AN
XR7      6 INTGND INTGND DC00400N  RES=1K
XD2      OUT 9 INTGND DB0814AN
XD3      16 OUT INTGND DB3002AN
XR8      INTVCC 15 INTGND DB01E00N  RES=15
MM19     INTVCC 4 19 INTVCC MHS4XPEN L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM20     19 26 7 INTVCC MHS4XPEN L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM21     7 4 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM22     7 26 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM23     21 18 20 INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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MM24     20 26 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM25     INTVCC 18 21 INTVCC MHS4XPEN L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM26     INTVCC 26 21 INTVCC MHS4XPEN L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM43     INTVCC 4 22 INTVCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     22 21 17 INTVCC MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     17 4 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM46     17 21 INTGND INTGND MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     INTVCC 4 23 INTVCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     23 21 14 INTVCC MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     14 4 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM58     14 21 INTGND INTGND MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
XR9      INTVCC 12 INTGND DC00400N  RES=10K
QQ6      15 14 16 DE283ASN
XD5      16 OUT INTGND DB3002AN
XD6      16 OUT INTGND DB3002AN
XD7      16 OUT INTGND DB3002AN
XD8      16 OUT INTGND DB3002AN
QQ7      OUT 6 INTGND DE283ASN
QQ8      OUT 6 INTGND DE283ASN
QQ9      OUT 6 INTGND DE283ASN
QQ14     OEBAR INTGND INTGND ESDXXXXN
QQ15     26 INTGND INTGND ESDXXXXN
QQ16     OUT INTGND INTGND ESDXXXXN
M3M1   INTVCC D 25 INTVCC MHS4XPEN L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3M2   25 D INTGND INTGND MHS4XNEN L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3M3   26 25 INTGND INTGND MHS4XNEN L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3M4   INTVCC 25 26 INTVCC MHS4XPEN L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
XD15     24 1 INTGND DB0814AN
XD16     11 24 INTGND DB0814AN
RR13     INTGND D 10MEG
.EOM A16244N
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* Philips Semiconductors - ABT16245
.MACRO A16245N D EN OUT INTVCC INTGND
MM1     1 28 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM2     3 4 2 INTVCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM3     1 4 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4     1 5 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5     6 28 INTGND INTGND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6     6 4 INTGND INTGND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM7     5 7 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM8     8 7 9 INTGND MHS4XNEN L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
MM9     9 7 6 INTGND MHS4XNEN L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
MM10    OUT 7 10 INTGND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM11    10 7 INTGND INTGND MHS4XNEN L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM12    2 28 11 INTVCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM13    12 5 3 INTVCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM14    INTVCC 7 5 INTVCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
QQ1     INTVCC 11 6 DA0ACBSN
QQ2     11 11 13 DA06CBSN
QQ3     OUT 6 INTGND DE283ASN
QQ4     15 14 16 DE283ASN
XQ5     15 17 14 INTGND DB14CASN
MM15    INTVCC OEBAR 18 INTVCC MHS4XPEN L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM16    INTVCC 18 4 INTVCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM17    18 OEBAR INTGND INTGND MHS4XNEN L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
MM18    4 18 INTGND INTGND MHS4XNEN L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
XD1     13 OUT INTGND DB0308AN
XR7     6 INTGND INTGND DC00400N  RES=1K
XD2     OUT 8 INTGND DB0814AN
XD3     16 OUT INTGND DB3002AN
XR8     INTVCC 15 INTGND DB01E00N  RES=15
MM19    INTVCC 4 19 INTVCC MHS4XPEN L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM20    19 28 7 INTVCC MHS4XPEN L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM21    7 4 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM22    7 28 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM23    20 18 21 INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM24    21 28 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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MM25     INTVCC 18 20 INTVCC MHS4XPEN L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM26     INTVCC 28 20 INTVCC MHS4XPEN L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM43     INTVCC 4 22 INTVCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     22 20 17 INTVCC MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     17 4 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM46     17 20 INTGND INTGND MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     INTVCC 4 23 INTVCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     23 20 14 INTVCC MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     14 4 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM58     14 20 INTGND INTGND MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
XR9      INTVCC 12 INTGND DC00400N  RES=10K
QQ6      15 14 16 DE283ASN
XD5      16 OUT INTGND DB3002AN
XD6      16 OUT INTGND DB3002AN
XD7      16 OUT INTGND DB3002AN
XD8      16 OUT INTGND DB3002AN
QQ7      OUT 6 INTGND DE283ASN
QQ8      OUT 6 INTGND DE283ASN
QQ9      OUT 6 INTGND DE283ASN
XD9      INTGND 28 INTGND DB3002AN
XD10     INTGND 28 INTGND DB3002AN
XD11     INTGND 28 INTGND DB3002AN
XD12     INTGND 28 INTGND DB3002AN
XD13     INTGND 28 INTGND DB3002AN
MM60     28 INTGND INTGND INTGND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
XD14     28 INTVCC INTGND DB0814AN
QQ10     24 INTGND INTGND DE283ASN
QQ11     24 INTGND INTGND DE283ASN
QQ12     24 INTGND INTGND DE283ASN
QQ13     24 INTGND INTGND DE283ASN
XR11     28 24 INTGND DB01E00N  RES=22.5
QQ14     OEBAR INTGND INTGND ESDXXXXN
QQ15     28 INTGND INTGND ESDXXXXN
QQ16     OUT INTGND INTGND ESDXXXXN
MM61     INTVCC OUT 25 INTVCC MHS4XPEN L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
MM62     25 OUT INTGND INTGND MHS4XNEN L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
XD15     11 26 INTGND DB0814AN
XD16     26 1 INTGND DB0814AN
M3M1  INTVCC D 27 INTVCC MHS4XPEN L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3M2  27 D INTGND INTGND MHS4XNEN L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3M3  28 27 INTGND INTGND MHS4XNEN L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3M4  INTVCC 27 28 INTVCC MHS4XPEN L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.EOM A16245N
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* Philips Semiconductors - ABT162441
.MACRO A162441N D EN OUT INTVCC INTGND
MM1      1 26 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM2      3 4 2 INTVCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM3      1 4 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 26 INTGND INTGND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 INTGND INTGND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM7      5 7 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM8      9 7 8 INTGND MHS4XNEN L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
MM9      8 7 6 INTGND MHS4XNEN L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
MM10     OUT 7 10 INTGND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM11     10 7 INTGND INTGND MHS4XNEN L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM12     2 26 11 INTVCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM13     12 5 3 INTVCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM14     INTVCC 7 5 INTVCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
QQ1      INTVCC 11 6 DA0ACBSN
QQ2      11 11 13 DA06CBSN
QQ3      OUTA 6 INTGND DE283ASN
RR20     OUT OUTA 22.5
QQ4      15 14 16 DE283ASN
XQ5      15 17 14 INTGND DB14CASN
MM15     INTVCC OEBAR 18 INTVCC MHS4XPEN L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM16     INTVCC 18 4 INTVCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM17     18 OEBAR INTGND INTGND MHS4XNEN L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
MM18     4 18 INTGND INTGND MHS4XNEN L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
XD1      13 OUTA INTGND DB0308AN
XR7      6 INTGND INTGND DC00400N  RES=1K
XD2      OUT 9 INTGND DB0814AN
XD3      16 OUT INTGND DB3002AN
XR8      INTVCC 15 INTGND DB01E00N  RES=15
MM19     INTVCC 4 19 INTVCC MHS4XPEN L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM20     19 26 7 INTVCC MHS4XPEN L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM21     7 4 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM22     7 26 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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MM23     21 18 20 INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM24     20 26 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM25     INTVCC 18 21 INTVCC MHS4XPEN L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM26     INTVCC 26 21 INTVCC MHS4XPEN L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM43     INTVCC 4 22 INTVCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     22 21 17 INTVCC MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     17 4 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM46     17 21 INTGND INTGND MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     INTVCC 4 23 INTVCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     23 21 14 INTVCC MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     14 4 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM58     14 21 INTGND INTGND MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
XR9      INTVCC 12 INTGND DC00400N  RES=10K
QQ6      15 14 16 DE283ASN
XD5      16 OUT INTGND DB3002AN
XD6      16 OUT INTGND DB3002AN
XD7      16 OUT INTGND DB3002AN
XD8      16 OUT INTGND DB3002AN
QQ7      OUTA 6 INTGND DE283ASN
QQ8      OUTA 6 INTGND DE283ASN
QQ9      OUTA 6 INTGND DE283ASN
QQ14     OEBAR INTGND INTGND ESDXXXXN
QQ15     26 INTGND INTGND ESDXXXXN
QQ16     OUT INTGND INTGND ESDXXXXN
M3M1   INTVCC D 25 INTVCC MHS4XPEN L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3M2   25 D INTGND INTGND MHS4XNEN L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3M3   26 25 INTGND INTGND MHS4XNEN L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3M4   INTVCC 25 26 INTVCC MHS4XPEN L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
XD15     24 1 INTGND DB0814AN
XD16     11 24 INTGND DB0814AN
RR13     INTGND D 10MEG
.EOM A162441N
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* Philips Semiconductors - ABT162451
.MACRO A162451N D EN OUT INTVCC INTGND
MM1      1 28 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM2      3 4 2 INTVCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM3      1 4 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 28 INTGND INTGND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 INTGND INTGND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM7      5 7 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM8      8 7 9 INTGND MHS4XNEN L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
MM9      9 7 6 INTGND MHS4XNEN L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
MM10     OUT 7 10 INTGND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM11     10 7 INTGND INTGND MHS4XNEN L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM12     2 28 11 INTVCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM13     12 5 3 INTVCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM14     INTVCC 7 5 INTVCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
QQ1      INTVCC 11 6 DA0ACBSN
QQ2      11 11 13 DA06CBSN
QQ3      OUTA 6 INTGND DE283ASN
RR20     OUT OUTA 22.5
QQ4      15 14 16 DE283ASN
XQ5      15 17 14 INTGND DB14CASN
MM15     INTVCC OEBAR 18 INTVCC MHS4XPEN L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM16     INTVCC 18 4 INTVCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM17     18 OEBAR INTGND INTGND MHS4XNEN L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
MM18     4 18 INTGND INTGND MHS4XNEN L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
XD1      13 OUTA INTGND DB0308AN
XR7      6 INTGND INTGND DC00400N  RES=1K
XD2      OUT 8 INTGND DB0814AN
XD3      16 OUT INTGND DB3002AN
XR8      INTVCC 15 INTGND DB01E00N  RES=15
MM19     INTVCC 4 19 INTVCC MHS4XPEN L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM20     19 28 7 INTVCC MHS4XPEN L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM21     7 4 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM22     7 28 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM23     20 18 21 INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM24     21 28 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
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+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM25     INTVCC 18 20 INTVCC MHS4XPEN L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM26     INTVCC 28 20 INTVCC MHS4XPEN L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM43     INTVCC 4 22 INTVCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     22 20 17 INTVCC MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     17 4 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM46     17 20 INTGND INTGND MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     INTVCC 4 23 INTVCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     23 20 14 INTVCC MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     14 4 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM58     14 20 INTGND INTGND MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
XR9      INTVCC 12 INTGND DC00400N  RES=10K
QQ6      15 14 16 DE283ASN
XD5      16 OUT INTGND DB3002AN
XD6      16 OUT INTGND DB3002AN
XD7      16 OUT INTGND DB3002AN
XD8      16 OUT INTGND DB3002AN
QQ7      OUTA 6 INTGND DE283ASN
QQ8      OUTA 6 INTGND DE283ASN
QQ9      OUTA 6 INTGND DE283ASN
XD9      INTGND 28 INTGND DB3002AN
XD10     INTGND 28 INTGND DB3002AN
XD11     INTGND 28 INTGND DB3002AN
XD12     INTGND 28 INTGND DB3002AN
XD13     INTGND 28 INTGND DB3002AN
MM60     28 INTGND INTGND INTGND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
XD14     28 INTVCC INTGND DB0814AN
QQ10     24 INTGND INTGND DE283ASN
QQ11     24 INTGND INTGND DE283ASN
QQ12     24 INTGND INTGND DE283ASN
QQ13     24 INTGND INTGND DE283ASN
XR11     28 24 INTGND DB01E00N  RES=22.5
QQ14     OEBAR INTGND INTGND ESDXXXXN
QQ15     28 INTGND INTGND ESDXXXXN
QQ16     OUT INTGND INTGND ESDXXXXN
MM61     INTVCC OUT 25 INTVCC MHS4XPEN L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
MM62     25 OUT INTGND INTGND MHS4XNEN L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
XD15     11 26 INTGND DB0814AN
XD16     26 1 INTGND DB0814AN
M3M1   INTVCC D 27 INTVCC MHS4XPEN L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3M2   27 D INTGND INTGND MHS4XNEN L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3M3   28 27 INTGND INTGND MHS4XNEN L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3M4   INTVCC 27 28 INTVCC MHS4XPEN L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.EOM A162451N
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A16FASHS.LIB Subcircuit

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*****************************************************************************
* ABT16 HSPICE SUBCIRCUIT LIBRARY
* A16FASHS.LIB
* FAST PROCESS CORNER
* STANDARD LOGIC PRODUCT GROUP
* PHILIPS SEMICONDUCTORS
* 3/31/1995
*****************************************************************************
.SUBCKT INV1 D E Q VCC
* USE THIS MODEL FOR ABT16240 (INVERTING PART)
*   IN  OUT  INTVCC  INTGND   (ENABLE)
X1  3    90    99       6          INBUFFF
*   IN  OUT  INTVCC  INTGND   (SIGNAL)
X2  1    91    99       6          MOSINVF
*   D    EN   OUT   INTVCC  INTGND
X3  91   90    2      99       6     OUTBUFFF
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1
*
.SUBCKT INV1_1 D E Q VCC
* USE THIS MODEL FOR ABT16240-1 (INVERTING PART)
*   IN  OUT  INTVCC  INTGND   (ENABLE)
X1  3    90    99       6          INBUFFF
*   IN  OUT  INTVCC  INTGND   (SIGNAL)
X2  1    91    99       6          MOSINVF
*   D    EN   OUT   INTVCC  INTGND
X3  91   90    2      99       6     OUTBUF1F
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1_1
.SUBCKT INV2 D E Q VCC
*
*   IN  OUT  INTVCC  INTGND   (ENABLE)
X1  3    90    99       6          INBUFFF
*   IN  OUT  INTVCC  INTGND   (SIGNAL)
X2  1    91    99       6          MOSINVF
*   D    EN   OUT   INTVCC  INTGND
X3  91   90    2      99       6     OUTBUFFF
*   IN  OUT  INTVCC  INTGND
X4   2   1     99       6          BCKLOADF
```

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*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV2
.SUBCKT NINV D E Q VCC
* USE THIS MODEL FOR ABT16273  -373B  -374B  -541
*  -821  -823  -825  -827  -841  (NON-INVERTING)
**    IN  OUT  INTVCC  INTGND  (ENABLE)
X1   3    90    99        6          INBUFFF
*    IN  OUT  INTVCC  INTGND  (SIGNAL)
X2   1    91    99        6          INBUFFF
*    D    EN   OUT   INTVCC  INTGND
X3   91   90    2      99       6     OUTBUFFF
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINV
*
.SUBCKT NINVB D E Q VCC
* USE THIS MODEL FOR ABT16500  -501  -543  -646  -652  -899
* -952  -1543
*    IN  OUT  INTVCC  INTGND  (ENABLE)
X1   3    90    99        6          INBUFFF
*    IN  OUT  INTVCC  INTGND  (SIGNAL)
X2   1    91    99        6          INBUFFF
*    D    EN   OUT   INTVCC  INTGND
X3   91   90    2      99       6     OUTBUFFF
*    IN  OUT  INTVCC  INTGND
X4   2    1     99        6          BCKLOADF
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINVB
*
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.SUBCKT A16244 D E Q VCC
* USE THIS MODEL FOR ABT16244A
*   D     EN    OUT    INTVCC   INTGND
X3  1      3     2        99       6     A16244F
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16244
*
.SUBCKT A16245 D E Q VCC
* USE THIS MODEL FOR ABT16245B
*   D     EN    OUT    INTVCC   INTGND
X3  1      3     2       99        6     A16245F
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16245
*
.SUBCKT A16244_1 D E Q VCC
* USE THIS MODEL FOR ABT16244-1
*   D     EN    OUT    INTVCC   INTGND
X3  1      3     2        99       6     A162441F
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16244_1
*
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```
.SUBCKT A16245_1 D E Q VCC
* USE THIS MODEL FOR ABT16245A-1
*   D    EN   OUT   INTVCC  INTGND
X3  1     3    2      99       6     A162451F
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16245_1
*
* Philips Semiconductors - MOSINV
.MACRO MOSINVF IN OUT INTVCC INTGND
MM1      INTVCC IN 1 INTVCC MHS4XPEF L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
MM2      1 IN INTGND INTGND MHS4XNEF L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
MM3      OUT 1 INTGND INTGND MHS4XNEF L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
MM4      INTVCC 1 OUT INTVCC MHS4XPEF L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.EOM MOSINVF
* Philips Semiconductors - INBUFF
.MACRO INBUFFF IN OUT INTVCC INTGND
MM1      OUT IN INTGND INTGND MHS4XNEF L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
MM2      INTVCC IN 1 INTVCC MHS4XPEF L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
QQ1      IN INTGND INTGND ESDXXXXF
RR1      1 OUT 100
.EOM INBUFFF
* Philips Semiconductors - OUTBUFF
.MACRO OUTBUFFF   D EN OUT INTVCC INTGND
MM2      2 3 1 INTVCC MHS4XPEF L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
MM3      1 4 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 5 INTGND INTGND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 INTGND INTGND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM13     7 4 2 INTVCC MHS4XPEF L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
QQ1      INTVCC 8 5 DA04CASF
QQ2      1 1 9 DA0ACBSF
QQ3      OUT 6 INTGND DE283ASF
QQ4      11 10 12 DE283ASF
XQ5      11 13 10 INTGND DB14CASF
XD1      9 OUT INTGND DB0814AF
XR7      6 INTGND INTGND DC00400F  RES=1K
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XD3      12 OUT INTGND DB3002AF
XR8      INTVCC 11 INTGND DB01E00F  RES=15
MM43     INTVCC 4 14 INTVCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     14 D 13 INTVCC MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     13 4 INTGND INTGND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM46     13 D INTGND INTGND MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     INTVCC 4 15 INTVCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     15 D 10 INTVCC MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     10 4 INTGND INTGND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM58     10 D INTGND INTGND MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
XR9      INTVCC 7 INTGND DC00400F  RES=10K
QQ6      11 10 12 DE283ASF
XD5      12 OUT INTGND DB3002AF
XD6      12 OUT INTGND DB3002AF
XD7      12 OUT INTGND DB3002AF
XD8      12 OUT INTGND DB3002AF
QQ7      OUT 6 INTGND DE283ASF
QQ8      OUT 6 INTGND DE283ASF
QQ9      OUT 6 INTGND DE283ASF
MM61     INTVCC 17 16 INTVCC MHS4XPEF L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
MM62     16 EN 18 INTGND MHS4XNEF L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
MM63     18 D 6 INTGND MHS4XNEF L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
MM64     17 OUT INTGND INTGND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM65     INTVCC OUT 17 INTVCC MHS4XPEF L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
MM66     OUT EN 19 INTGND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM67     19 D INTGND INTGND MHS4XNEF L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM68     3 D INTGND INTGND MHS4XNEF L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
MM69     INTVCC D 3 INTVCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM70     8 D INTGND INTGND MHS4XNEF L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
MM71     INTVCC D 8 INTVCC MHS4XPEF L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM72     5 D INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM73     INTVCC D 5 INTVCC MHS4XPEF L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
QQ14     INTVCC 1 6 DA0ACBSF
QQ15     OUT INTGND INTGND ESDXXXXF
MM74     4 EN INTGND INTGND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM75     INTVCC EN 4 INTVCC MHS4XPEF L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
.EOM OUTBUFFF
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* Philips Semiconductors - OUTBUF1
.MACRO OUTBUF1F   D EN OUT INTVCC INTGND
MM2      2 3 1 INTVCC MHS4XPEF L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
MM3      1 4 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 5 INTGND INTGND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 INTGND INTGND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM13     7 4 2 INTVCC MHS4XPEF L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
QQ1      INTVCC 8 5 DA04CASF
QQ2      1 1 9 DA0ACBSF
QQ3      OUTA 6 INTGND DE283ASF
RR20     OUT OUTA 22.5
QQ4      11 10 12 DE283ASF
XQ5      11 13 10 INTGND DB14CASF
XD1      9 OUTA INTGND DB0814AF
XR7      6 INTGND INTGND DC00400F  RES=1K
XD3      12 OUT INTGND DB3002AF
XR8      INTVCC 11 INTGND DB01E00F  RES=15
MM43     INTVCC 4 14 INTVCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     14 D 13 INTVCC MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     13 4 INTGND INTGND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM46     13 D INTGND INTGND MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     INTVCC 4 15 INTVCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     15 D 10 INTVCC MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     10 4 INTGND INTGND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM58     10 D INTGND INTGND MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
XR9      INTVCC 7 INTGND DC00400F  RES=10K
QQ6      11 10 12 DE283ASF
XD5      12 OUT INTGND DB3002AF
XD6      12 OUT INTGND DB3002AF
XD7      12 OUT INTGND DB3002AF
XD8      12 OUT INTGND DB3002AF
QQ7      OUTA 6 INTGND DE283ASF
QQ8      OUTA 6 INTGND DE283ASF
QQ9      OUTA 6 INTGND DE283ASF
MM61     INTVCC 17 16 INTVCC MHS4XPEF L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
MM62     16 EN 18 INTGND MHS4XNEF L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
MM63     18 D 6 INTGND MHS4XNEF L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
MM64     17 OUT INTGND INTGND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
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MM65     INTVCC OUT 17 INTVCC MHS4XPEF L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
MM66     OUT EN 19 INTGND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM67     19 D INTGND INTGND MHS4XNEF L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM68     3 D INTGND INTGND MHS4XNEF L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
MM69     INTVCC D 3 INTVCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM70     8 D INTGND INTGND MHS4XNEF L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
MM71     INTVCC D 8 INTVCC MHS4XPEF L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM72     5 D INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM73     INTVCC D 5 INTVCC MHS4XPEF L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
QQ14     INTVCC 1 6 DA0ACBSF
QQ15     OUT INTGND INTGND ESDXXXXF
MM74     4 EN INTGND INTGND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM75     INTVCC EN 4 INTVCC MHS4XPEF L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
.EOM OUTBUF1F
* Philips Semiconductors - BCKLOAD
.MACRO BCKLOADF IN OUT INTVCC INTGND
XD9      INTGND IN INTGND DB3002AF
XD10     INTGND IN INTGND DB3002AF
XD11     INTGND IN INTGND DB3002AF
XD12     INTGND IN INTGND DB3002AF
XD13     INTGND IN INTGND DB3002AF
MM60     IN INTGND INTGND INTGND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
XD14     IN INTVCC INTGND DB0814AF
QQ10     IN INTGND INTGND DE283ASF
QQ11     IN INTGND INTGND DE283ASF
QQ12     IN INTGND INTGND DE283ASF
QQ13     IN INTGND INTGND DE283ASF
MM61     INTVCC OUT 1 1 MHS4XPEF L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
MM62     1 OUT INTGND INTGND MHS4XNEF L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
.EOM BCKLOADF
* Philips Semiconductors - BUSHLD1
.MACRO BUSHLD1F   BH INTVCC INTGND
XD1      1 2 INTGND DB3002AF
QQ1      3 3 1 DE283ASF
XR1      2 BH INTGND DC00400F  RES=2K
XR2      BH 4 INTGND DC00400F  RES=5K
MM4      4 5 INTGND INTGND MHS4XNEF L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
MM1      5 BH INTGND INTGND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM2      INTVCC BH 5 5 MHS4XPEF L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM3      INTVCC 5 3 3 MHS4XPEF L=1.0U W=8.298U
+ AD=16.596P AS=16.596P PD=20.596U PS=20.596U NRD=0.241 NRS=0.241
.EOM BUSHLD1F
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* Philips Semiconductors - ABT16244
.MACRO A16244F D EN OUT INTVCC INTGND
MM1      1 26 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM2      3 4 2 INTVCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM3      1 4 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 26 INTGND INTGND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 INTGND INTGND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM7      5 7 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM8      9 7 8 INTGND MHS4XNEF L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
MM9      8 7 6 INTGND MHS4XNEF L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
MM10     OUT 7 10 INTGND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM11     10 7 INTGND INTGND MHS4XNEF L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM12     2 26 11 INTVCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM13     12 5 3 INTVCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM14     INTVCC 7 5 INTVCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
QQ1      INTVCC 11 6 DA0ACBSF
QQ2      11 11 13 DA06CBSF
QQ3      OUT 6 INTGND DE283ASF
QQ4      15 14 16 DE283ASF
XQ5      15 17 14 INTGND DB14CASF
MM15     INTVCC OEBAR 18 INTVCC MHS4XPEF L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM16     INTVCC 18 4 INTVCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM17     18 OEBAR INTGND INTGND MHS4XNEF L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
MM18     4 18 INTGND INTGND MHS4XNEF L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
XD1      13 OUT INTGND DB0308AF
XR7      6 INTGND INTGND DC00400F  RES=1K
XD2      OUT 9 INTGND DB0814AF
XD3      16 OUT INTGND DB3002AF
XR8      INTVCC 15 INTGND DB01E00F  RES=15
MM19     INTVCC 4 19 INTVCC MHS4XPEF L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM20     19 26 7 INTVCC MHS4XPEF L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM21     7 4 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM22     7 26 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM23     21 18 20 INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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MM24     20 26 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM25     INTVCC 18 21 INTVCC MHS4XPEF L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM26     INTVCC 26 21 INTVCC MHS4XPEF L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM43     INTVCC 4 22 INTVCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     22 21 17 INTVCC MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     17 4 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM46     17 21 INTGND INTGND MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     INTVCC 4 23 INTVCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     23 21 14 INTVCC MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     14 4 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM58     14 21 INTGND INTGND MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
XR9      INTVCC 12 INTGND DC00400F  RES=10K
QQ6      15 14 16 DE283ASF
XD5      16 OUT INTGND DB3002AF
XD6      16 OUT INTGND DB3002AF
XD7      16 OUT INTGND DB3002AF
XD8      16 OUT INTGND DB3002AF
QQ7      OUT 6 INTGND DE283ASF
QQ8      OUT 6 INTGND DE283ASF
QQ9      OUT 6 INTGND DE283ASF
QQ14     OEBAR INTGND INTGND ESDXXXXF
QQ15     26 INTGND INTGND ESDXXXXF
QQ16     OUT INTGND INTGND ESDXXXXF
M3M1   INTVCC D 25 INTVCC MHS4XPEF L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3M2   25 D INTGND INTGND MHS4XNEF L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3M3   26 25 INTGND INTGND MHS4XNEF L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3M4   INTVCC 25 26 INTVCC MHS4XPEF L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
XD15     24 1 INTGND DB0814AF
XD16     11 24 INTGND DB0814AF
RR13     INTGND D 10MEG
.EOM A16244F
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* Philips Semiconductors - ABT16245
.MACRO A16245F D EN OUT INTVCC INTGND
MM1      1 28 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM2      3 4 2 INTVCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM3      1 4 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 28 INTGND INTGND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 INTGND INTGND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM7      5 7 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM8      8 7 9 INTGND MHS4XNEF L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
MM9      9 7 6 INTGND MHS4XNEF L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
MM10     OUT 7 10 INTGND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM11     10 7 INTGND INTGND MHS4XNEF L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM12     2 28 11 INTVCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM13     12 5 3 INTVCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM14     INTVCC 7 5 INTVCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
QQ1      INTVCC 11 6 DA0ACBSF
QQ2      11 11 13 DA06CBSF
QQ3      OUT 6 INTGND DE283ASF
QQ4      15 14 16 DE283ASF
XQ5      15 17 14 INTGND DB14CASF
MM15     INTVCC OEBAR 18 INTVCC MHS4XPEF L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM16     INTVCC 18 4 INTVCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM17     18 OEBAR INTGND INTGND MHS4XNEF L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
MM18     4 18 INTGND INTGND MHS4XNEF L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
XD1      13 OUT INTGND DB0308AF
XR7      6 INTGND INTGND DC00400F  RES=1K
XD2      OUT 8 INTGND DB0814AF
XD3      16 OUT INTGND DB3002AF
XR8      INTVCC 15 INTGND DB01E00F  RES=15
MM19     INTVCC 4 19 INTVCC MHS4XPEF L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM20     19 28 7 INTVCC MHS4XPEF L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM21     7 4 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM22     7 28 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM23     20 18 21 INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM24     21 28 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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MM25     INTVCC 18 20 INTVCC MHS4XPEF L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM26     INTVCC 28 20 INTVCC MHS4XPEF L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM43     INTVCC 4 22 INTVCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     22 20 17 INTVCC MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     17 4 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM46     17 20 INTGND INTGND MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     INTVCC 4 23 INTVCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     23 20 14 INTVCC MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     14 4 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM58     14 20 INTGND INTGND MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
XR9      INTVCC 12 INTGND DC00400F  RES=10K
QQ6      15 14 16 DE283ASF
XD5      16 OUT INTGND DB3002AF
XD6      16 OUT INTGND DB3002AF
XD7      16 OUT INTGND DB3002AF
XD8      16 OUT INTGND DB3002AF
QQ7      OUT 6 INTGND DE283ASF
QQ8      OUT 6 INTGND DE283ASF
QQ9      OUT 6 INTGND DE283ASF
XD9      INTGND 28 INTGND DB3002AF
XD10     INTGND 28 INTGND DB3002AF
XD11     INTGND 28 INTGND DB3002AF
XD12     INTGND 28 INTGND DB3002AF
XD13     INTGND 28 INTGND DB3002AF
MM60     28 INTGND INTGND INTGND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
XD14     28 INTVCC INTGND DB0814AF
QQ10     24 INTGND INTGND DE283ASF
QQ11     24 INTGND INTGND DE283ASF
QQ12     24 INTGND INTGND DE283ASF
QQ13     24 INTGND INTGND DE283ASF
XR11     28 24 INTGND DB01E00F  RES=22.5
QQ14     OEBAR INTGND INTGND ESDXXXXF
QQ15     28 INTGND INTGND ESDXXXXF
QQ16     OUT INTGND INTGND ESDXXXXF
MM61     INTVCC OUT 25 INTVCC MHS4XPEF L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
MM62     25 OUT INTGND INTGND MHS4XNEF L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
XD15     11 26 INTGND DB0814AF
XD16     26 1 INTGND DB0814AF
M3M1   INTVCC D 27 INTVCC MHS4XPEF L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3M2   27 D INTGND INTGND MHS4XNEF L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3M3   28 27 INTGND INTGND MHS4XNEF L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3M4   INTVCC 27 28 INTVCC MHS4XPEF L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.EOM A16245F
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* Philips Semiconductors - ABT162441
.MACRO A162441F D EN OUT INTVCC INTGND
MM1      1 26 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM2      3 4 2 INTVCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM3      1 4 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 26 INTGND INTGND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 INTGND INTGND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM7      5 7 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM8      9 7 8 INTGND MHS4XNEF L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
MM9      8 7 6 INTGND MHS4XNEF L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
MM10     OUT 7 10 INTGND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM11     10 7 INTGND INTGND MHS4XNEF L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM12     2 26 11 INTVCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM13     12 5 3 INTVCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM14     INTVCC 7 5 INTVCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
QQ1      INTVCC 11 6 DA0ACBSF
QQ2      11 11 13 DA06CBSF
QQ3      OUTA 6 INTGND DE283ASF
RR20     OUT OUTA 22.5
QQ4      15 14 16 DE283ASF
XQ5      15 17 14 INTGND DB14CASF
MM15     INTVCC OEBAR 18 INTVCC MHS4XPEF L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM16     INTVCC 18 4 INTVCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM17     18 OEBAR INTGND INTGND MHS4XNEF L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
MM18     4 18 INTGND INTGND MHS4XNEF L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
XD1      13 OUTA INTGND DB0308AF
XR7      6 INTGND INTGND DC00400F  RES=1K
XD2      OUT 9 INTGND DB0814AF
XD3      16 OUT INTGND DB3002AF
XR8      INTVCC 15 INTGND DB01E00F  RES=15
MM19     INTVCC 4 19 INTVCC MHS4XPEF L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM20     19 26 7 INTVCC MHS4XPEF L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM21     7 4 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM22     7 26 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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MM23     21 18 20 INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM24     20 26 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM25     INTVCC 18 21 INTVCC MHS4XPEF L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM26     INTVCC 26 21 INTVCC MHS4XPEF L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM43     INTVCC 4 22 INTVCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     22 21 17 INTVCC MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     17 4 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM46     17 21 INTGND INTGND MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     INTVCC 4 23 INTVCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     23 21 14 INTVCC MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     14 4 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM58     14 21 INTGND INTGND MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
XR9      INTVCC 12 INTGND DC00400F  RES=10K
QQ6      15 14 16 DE283ASF
XD5      16 OUT INTGND DB3002AF
XD6      16 OUT INTGND DB3002AF
XD7      16 OUT INTGND DB3002AF
XD8      16 OUT INTGND DB3002AF
QQ7      OUTA 6 INTGND DE283ASF
QQ8      OUTA 6 INTGND DE283ASF
QQ9      OUTA 6 INTGND DE283ASF
QQ14     OEBAR INTGND INTGND ESDXXXXF
QQ15     26 INTGND INTGND ESDXXXXF
QQ16     OUT INTGND INTGND ESDXXXXF
M3M1   INTVCC D 25 INTVCC MHS4XPEF L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3M2   25 D INTGND INTGND MHS4XNEF L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3M3   26 25 INTGND INTGND MHS4XNEF L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3M4   INTVCC 25 26 INTVCC MHS4XPEF L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
XD15     24 1 INTGND DB0814AF
XD16     11 24 INTGND DB0814AF
RR13     INTGND D 10MEG
.EOM A162441F
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* Philips Semiconductors - ABT162451
.MACRO A162451F D EN OUT INTVCC INTGND
MM1      1 28 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM2      3 4 2 INTVCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM3      1 4 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 28 INTGND INTGND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 INTGND INTGND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM7      5 7 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM8      8 7 9 INTGND MHS4XNEF L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
MM9      9 7 6 INTGND MHS4XNEF L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
MM10     OUT 7 10 INTGND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM11     10 7 INTGND INTGND MHS4XNEF L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM12     2 28 11 INTVCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM13     12 5 3 INTVCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM14     INTVCC 7 5 INTVCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
QQ1      INTVCC 11 6 DA0ACBSF
QQ2      11 11 13 DA06CBSF
QQ3      OUTA 6 INTGND DE283ASF
RR20     OUT OUTA 22.5
QQ4      15 14 16 DE283ASF
XQ5      15 17 14 INTGND DB14CASF
MM15     INTVCC OEBAR 18 INTVCC MHS4XPEF L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM16     INTVCC 18 4 INTVCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM17     18 OEBAR INTGND INTGND MHS4XNEF L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
MM18     4 18 INTGND INTGND MHS4XNEF L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
XD1      13 OUTA INTGND DB0308AF
XR7      6 INTGND INTGND DC00400F  RES=1K
XD2      OUT 8 INTGND DB0814AF
XD3      16 OUT INTGND DB3002AF
XR8      INTVCC 15 INTGND DB01E00F  RES=15
MM19     INTVCC 4 19 INTVCC MHS4XPEF L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM20     19 28 7 INTVCC MHS4XPEF L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM21     7 4 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM22     7 28 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM23     20 18 21 INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM24     21 28 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
```

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MM25     INTVCC 18 20 INTVCC MHS4XPEF L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM26     INTVCC 28 20 INTVCC MHS4XPEF L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM43     INTVCC 4 22 INTVCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     22 20 17 INTVCC MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     17 4 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM46     17 20 INTGND INTGND MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     INTVCC 4 23 INTVCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     23 20 14 INTVCC MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     14 4 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM58     14 20 INTGND INTGND MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
XR9      INTVCC 12 INTGND DC00400F  RES=10K
QQ6      15 14 16 DE283ASF
XD5      16 OUT INTGND DB3002AF
XD6      16 OUT INTGND DB3002AF
XD7      16 OUT INTGND DB3002AF
XD8      16 OUT INTGND DB3002AF
QQ7      OUTA 6 INTGND DE283ASF
QQ8      OUTA 6 INTGND DE283ASF
QQ9      OUTA 6 INTGND DE283ASF
XD9      INTGND 28 INTGND DB3002AF
XD10     INTGND 28 INTGND DB3002AF
XD11     INTGND 28 INTGND DB3002AF
XD12     INTGND 28 INTGND DB3002AF
XD13     INTGND 28 INTGND DB3002AF
MM60     28 INTGND INTGND INTGND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
XD14     28 INTVCC INTGND DB0814AF
QQ10     24 INTGND INTGND DE283ASF
QQ11     24 INTGND INTGND DE283ASF
QQ12     24 INTGND INTGND DE283ASF
QQ13     24 INTGND INTGND DE283ASF
XR11     28 24 INTGND DB01E00F  RES=22.5
QQ14     OEBAR INTGND INTGND ESDXXXXF
QQ15     28 INTGND INTGND ESDXXXXF
QQ16     OUT INTGND INTGND ESDXXXXF
MM61     INTVCC OUT 25 INTVCC MHS4XPEF L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
MM62     25 OUT INTGND INTGND MHS4XNEF L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
XD15     11 26 INTGND DB0814AF
XD16     26 1 INTGND DB0814AF
M3M1   INTVCC D 27 INTVCC MHS4XPEF L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3M2   27 D INTGND INTGND MHS4XNEF L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3M3   28 27 INTGND INTGND MHS4XNEF L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3M4   INTVCC 27 28 INTVCC MHS4XPEF L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.EOM A162451F
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A16SLOHS.LIB Subcircuit

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*****************************************************************************
* ABT16 HSPICE SUBCIRCUIT LIBRARY
* A16SLOHS.LIB
* SLOW PROCESS CORNER
* STANDARD LOGIC PRODUCT GROUP
* PHILIPS SEMICONDUCTORS
* 3/31/1995
*****************************************************************************
.SUBCKT INV1 D E Q VCC
* USE THIS MODEL FOR ABT16240 (INVERTING PART)
*    IN   OUT   INTVCC   INTGND    (ENABLE)
X1   3     90     99        6           INBUFFS
*    IN   OUT   INTVCC   INTGND    (SIGNAL)
X2   1     91     99        6           MOSINVS
*    D     EN    OUT    INTVCC   INTGND
X3   91    90     2       99        6      OUTBUFFS
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1
*
.SUBCKT INV1_1 D E Q VCC
* USE THIS MODEL FOR ABT16240-1 (INVERTING PART)
*    IN   OUT   INTVCC   INTGND    (ENABLE)
X1   3     90     99        6           INBUFFS
*    IN   OUT   INTVCC   INTGND    (SIGNAL)
X2   1     91     99        6           MOSINVS
*    D     EN    OUT    INTVCC   INTGND
X3   91    90     2       99        6      OUTBUF1F
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1_1
.SUBCKT INV2 D E Q VCC
*
*    IN   OUT   INTVCC   INTGND    (ENABLE)
X1   3     90     99        6           INBUFFS
*    IN   OUT   INTVCC   INTGND    (SIGNAL)
X2   1     91     99        6           MOSINVS
*    D     EN    OUT    INTVCC   INTGND
X3   91    90     2       99        6      OUTBUFFS
*    IN   OUT   INTVCC   INTGND
X4    2    1      99        6           BCKLOADS
```

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*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV2
.SUBCKT NINV D E Q VCC
* USE THIS MODEL FOR ABT16273  -373B  -374B  -541
*  -821  -823  -825  -827  -841  (NON-INVERTING)
**    IN   OUT   INTVCC   INTGND   (ENABLE)
X1   3     90     99         6          INBUFFS
*    IN   OUT   INTVCC   INTGND    (SIGNAL)
X2   1     91     99         6          INBUFFS
*    D     EN    OUT    INTVCC   INTGND
X3   91    90     2       99        6      OUTBUFFS
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINV
*
.SUBCKT NINVB D E Q VCC
* USE THIS MODEL FOR ABT16500  -501  -543  -646  -652  -899
* -952  -1543
*    IN   OUT   INTVCC   INTGND   (ENABLE)
X1   3     90     99         6          INBUFFS
*    IN   OUT   INTVCC   INTGND   (SIGNAL)
X2   1     91     99         6          INBUFFS
*    D     EN    OUT    INTVCC   INTGND
X3   91    90     2       99        6      OUTBUFFS
*    IN   OUT   INTVCC   INTGND
X4    2    1      99         6             BCKLOADS
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINVB
*
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```
.SUBCKT A16244 D E Q VCC
* USE THIS MODEL FOR ABT16244A
*    D     EN    OUT    INTVCC   INTGND
X3   1      3     2        99       6      A16244S
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16244
*
.SUBCKT A16245 D E Q VCC
* USE THIS MODEL FOR ABT16245B
*    D     EN    OUT    INTVCC   INTGND
X3   1      3     2        99       6      A16245S
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16245
*
.SUBCKT A16244_1 D E Q VCC
* USE THIS MODEL FOR ABT16244-1
*    D     EN    OUT    INTVCC   INTGND
X3   1      3     2        99       6      A162441S
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16244_1
*
```

```
.SUBCKT A16245_1 D E Q VCC
* USE THIS MODEL FOR ABT16245A-1
*   D     EN    OUT    INTVCC  INTGND
X3  1      3     2       99       6     A162451S
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16245_1
*
* Philips Semiconductors - MOSINV
.MACRO MOSINVS IN OUT INTVCC INTGND
MM1      INTVCC IN 1 INTVCC MHS4XPES L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
MM2      1 IN INTGND INTGND MHS4XNES L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
MM3      OUT 1 INTGND INTGND MHS4XNES L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
MM4      INTVCC 1 OUT INTVCC MHS4XPES L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.EOM MOSINVS
* Philips Semiconductors - INBUFF
.MACRO INBUFFS IN OUT INTVCC INTGND
MM1      OUT IN INTGND INTGND MHS4XNES L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
MM2      INTVCC IN 1 INTVCC MHS4XPES L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
QQ1      IN INTGND INTGND ESDXXXXS
RR1      1 OUT 100
.EOM INBUFFS
* Philips Semiconductors - OUTBUFF
.MACRO OUTBUFFS   D EN OUT INTVCC INTGND
MM2      2 3 1 INTVCC MHS4XPES L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
MM3      1 4 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 5 INTGND INTGND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 INTGND INTGND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM13     7 4 2 INTVCC MHS4XPES L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
QQ1      INTVCC 8 5 DA04CASS
QQ2      1 1 9 DA0ACBSS
QQ3      OUT 6 INTGND DE283ASS
QQ4      11 10 12 DE283ASS
XQ5      11 13 10 INTGND DB14CASS
XD1      9 OUT INTGND DB0814AS
XR7      6 INTGND INTGND DC00400S  RES=1K
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XD3      12 OUT INTGND DB3002AS
XR8      INTVCC 11 INTGND DB01E00S  RES=15
MM43     INTVCC 4 14 INTVCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     14 D 13 INTVCC MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     13 4 INTGND INTGND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM46     13 D INTGND INTGND MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     INTVCC 4 15 INTVCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     15 D 10 INTVCC MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     10 4 INTGND INTGND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM58     10 D INTGND INTGND MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
XR9      INTVCC 7 INTGND DC00400S  RES=10K
QQ6      11 10 12 DE283ASS
XD5      12 OUT INTGND DB3002AS
XD6      12 OUT INTGND DB3002AS
XD7      12 OUT INTGND DB3002AS
XD8      12 OUT INTGND DB3002AS
QQ7      OUT 6 INTGND DE283ASS
QQ8      OUT 6 INTGND DE283ASS
QQ9      OUT 6 INTGND DE283ASS
MM61     INTVCC 17 16 INTVCC MHS4XPES L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
MM62     16 EN 18 INTGND MHS4XNES L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
MM63     18 D 6 INTGND MHS4XNES L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
MM64     17 OUT INTGND INTGND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM65     INTVCC OUT 17 INTVCC MHS4XPES L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
MM66     OUT EN 19 INTGND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM67     19 D INTGND INTGND MHS4XNES L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM68     3 D INTGND INTGND MHS4XNES L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
MM69     INTVCC D 3 INTVCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM70     8 D INTGND INTGND MHS4XNES L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
MM71     INTVCC D 8 INTVCC MHS4XPES L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM72     5 D INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM73     INTVCC D 5 INTVCC MHS4XPES L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
QQ14     INTVCC 1 6 DA0ACBSS
QQ15     OUT INTGND INTGND ESDXXXXS
MM74     4 EN INTGND INTGND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM75     INTVCC EN 4 INTVCC MHS4XPES L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
.EOM OUTBUFFS
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* Philips Semiconductors - OUTBUF1
.MACRO OUTBUF1S   D EN OUT INTVCC INTGND
MM2     2 3 1 INTVCC MHS4XPES L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
MM3     1 4 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4     1 5 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5     6 5 INTGND INTGND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6     6 4 INTGND INTGND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM13    7 4 2 INTVCC MHS4XPES L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
QQ1     INTVCC 8 5 DA04CASS
QQ2     1 1 9 DA0ACBSS
QQ3     OUTA 6 INTGND DE283ASS
RR20    OUT OUTA 22.5
QQ4     11 10 12 DE283ASS
XQ5     11 13 10 INTGND DB14CASS
XD1     9 OUTA INTGND DB0814AS
XR7     6 INTGND INTGND DC00400S  RES=1K
XD3     12 OUT INTGND DB3002AS
XR8     INTVCC 11 INTGND DB01E00S  RES=15
MM43    INTVCC 4 14 INTVCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44    14 D 13 INTVCC MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45    13 4 INTGND INTGND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM46    13 D INTGND INTGND MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55    INTVCC 4 15 INTVCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56    15 D 10 INTVCC MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57    10 4 INTGND INTGND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM58    10 D INTGND INTGND MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
XR9     INTVCC 7 INTGND DC00400S  RES=10K
QQ6     11 10 12 DE283ASS
XD5     12 OUT INTGND DB3002AS
XD6     12 OUT INTGND DB3002AS
XD7     12 OUT INTGND DB3002AS
XD8     12 OUT INTGND DB3002AS
QQ7     OUTA 6 INTGND DE283ASS
QQ8     OUTA 6 INTGND DE283ASS
QQ9     OUTA 6 INTGND DE283ASS
MM61    INTVCC 17 16 INTVCC MHS4XPES L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
MM62    16 EN 18 INTGND MHS4XNES L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
MM63    18 D 6 INTGND MHS4XNES L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
MM64    17 OUT INTGND INTGND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM65    INTVCC OUT 17 INTVCC MHS4XPES L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
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MM66     OUT EN 19 INTGND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM67     19 D INTGND INTGND MHS4XNES L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM68     3 D INTGND INTGND MHS4XNES L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
MM69     INTVCC D 3 INTVCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM70     8 D INTGND INTGND MHS4XNES L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
MM71     INTVCC D 8 INTVCC MHS4XPES L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM72     5 D INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM73     INTVCC D 5 INTVCC MHS4XPES L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
QQ14     INTVCC 1 6 DA0ACBSS
QQ15     OUT INTGND INTGND ESDXXXXS
MM74     4 EN INTGND INTGND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM75     INTVCC EN 4 INTVCC MHS4XPES L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
.EOM OUTBUF1S
* Philips Semiconductors - BCKLOAD
.MACRO BCKLOADS IN OUT INTVCC INTGND
XD9      INTGND IN INTGND DB3002AS
XD10     INTGND IN INTGND DB3002AS
XD11     INTGND IN INTGND DB3002AS
XD12     INTGND IN INTGND DB3002AS
XD13     INTGND IN INTGND DB3002AS
MM60     IN INTGND INTGND INTGND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
XD14     IN INTVCC INTGND DB0814AS
QQ10     IN INTGND INTGND DE283ASS
QQ11     IN INTGND INTGND DE283ASS
QQ12     IN INTGND INTGND DE283ASS
QQ13     IN INTGND INTGND DE283ASS
MM61     INTVCC OUT 1 1 MHS4XPES L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
MM62     1 OUT INTGND INTGND MHS4XNES L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
.EOM BCKLOADS
* Philips Semiconductors - BUSHLD1
.MACRO BUSHLD1S   BH INTVCC INTGND
XD1      1 2 INTGND DB3002AS
QQ1      3 3 1 DE283ASS
XR1      2 BH INTGND DC00400S  RES=2K
XR2      BH 4 INTGND DC00400S  RES=5K
MM4      4 5 INTGND INTGND MHS4XNES L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
MM1      5 BH INTGND INTGND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
MM2      INTVCC BH 5 5 MHS4XPES L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM3      INTVCC 5 3 3 MHS4XPES L=1.0U W=8.298U
+ AD=16.596P AS=16.596P PD=20.596U PS=20.596U NRD=0.241 NRS=0.241
.EOM BUSHLD1S
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* Philips Semiconductors - ABT16244
.MACRO A16244S D EN OUT INTVCC INTGND
MM1      1 26 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM2      3 4 2 INTVCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM3      1 4 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 26 INTGND INTGND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 INTGND INTGND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM7      5 7 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM8      9 7 8 INTGND MHS4XNES L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
MM9      8 7 6 INTGND MHS4XNES L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
MM10     OUT 7 10 INTGND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM11     10 7 INTGND INTGND MHS4XNES L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM12     2 26 11 INTVCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM13     12 5 3 INTVCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM14     INTVCC 7 5 INTVCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
QQ1      INTVCC 11 6 DA0ACBSS
QQ2      11 11 13 DA06CBSS
QQ3      OUT 6 INTGND DE283ASS
QQ4      15 14 16 DE283ASS
XQ5      15 17 14 INTGND DB14CASS
MM15     INTVCC OEBAR 18 INTVCC MHS4XPES L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM16     INTVCC 18 4 INTVCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM17     18 OEBAR INTGND INTGND MHS4XNES L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
MM18     4 18 INTGND INTGND MHS4XNES L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
XD1      13 OUT INTGND DB0308AS
XR7      6 INTGND INTGND DC00400S  RES=1K
XD2      OUT 9 INTGND DB0814AS
XD3      16 OUT INTGND DB3002AS
XR8      INTVCC 15 INTGND DB01E00S  RES=15
MM19     INTVCC 4 19 INTVCC MHS4XPES L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM20     19 26 7 INTVCC MHS4XPES L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM21     7 4 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM22     7 26 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM23     21 18 20 INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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MM24     20 26 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM25     INTVCC 18 21 INTVCC MHS4XPES L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM26     INTVCC 26 21 INTVCC MHS4XPES L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM43     INTVCC 4 22 INTVCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     22 21 17 INTVCC MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     17 4 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM46     17 21 INTGND INTGND MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     INTVCC 4 23 INTVCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     23 21 14 INTVCC MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     14 4 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM58     14 21 INTGND INTGND MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
XR9      INTVCC 12 INTGND DC00400S  RES=10K
QQ6      15 14 16 DE283ASS
XD5      16 OUT INTGND DB3002AS
XD6      16 OUT INTGND DB3002AS
XD7      16 OUT INTGND DB3002AS
XD8      16 OUT INTGND DB3002AS
QQ7      OUT 6 INTGND DE283ASS
QQ8      OUT 6 INTGND DE283ASS
QQ9      OUT 6 INTGND DE283ASS
QQ14     OEBAR INTGND INTGND ESDXXXXS
QQ15     26 INTGND INTGND ESDXXXXS
QQ16     OUT INTGND INTGND ESDXXXXS
M3M1   INTVCC D 25 INTVCC MHS4XPES L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3M2   25 D INTGND INTGND MHS4XNES L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3M3   26 25 INTGND INTGND MHS4XNES L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3M4   INTVCC 25 26 INTVCC MHS4XPES L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
XD15     24 1 INTGND DB0814AS
XD16     11 24 INTGND DB0814AS
RR13     INTGND D 10MEG
.EOM A16244S
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* Philips Semiconductors - ABT16245
.MACRO A16245S D EN OUT INTVCC INTGND
MM1     1 28 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM2     3 4 2 INTVCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM3     1 4 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4     1 5 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5     6 28 INTGND INTGND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6     6 4 INTGND INTGND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM7     5 7 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM8     8 7 9 INTGND MHS4XNES L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
MM9     9 7 6 INTGND MHS4XNES L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
MM10    OUT 7 10 INTGND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM11    10 7 INTGND INTGND MHS4XNES L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM12    2 28 11 INTVCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM13    12 5 3 INTVCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM14    INTVCC 7 5 INTVCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
QQ1     INTVCC 11 6 DA0ACBSS
QQ2     11 11 13 DA06CBSS
QQ3     OUT 6 INTGND DE283ASS
QQ4     15 14 16 DE283ASS
XQ5     15 17 14 INTGND DB14CASS
MM15    INTVCC OEBAR 18 INTVCC MHS4XPES L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM16    INTVCC 18 4 INTVCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM17    18 OEBAR INTGND INTGND MHS4XNES L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
MM18    4 18 INTGND INTGND MHS4XNES L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
XD1     13 OUT INTGND DB0308AS
XR7     6 INTGND INTGND DC00400S  RES=1K
XD2     OUT 8 INTGND DB0814AS
XD3     16 OUT INTGND DB3002AS
XR8     INTVCC 15 INTGND DB01E00S  RES=15
MM19    INTVCC 4 19 INTVCC MHS4XPES L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM20    19 28 7 INTVCC MHS4XPES L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM21    7 4 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM22    7 28 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM23    20 18 21 INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM24    21 28 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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MM25     INTVCC 18 20 INTVCC MHS4XPES L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM26     INTVCC 28 20 INTVCC MHS4XPES L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM43     INTVCC 4 22 INTVCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     22 20 17 INTVCC MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     17 4 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM46     17 20 INTGND INTGND MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     INTVCC 4 23 INTVCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     23 20 14 INTVCC MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     14 4 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM58     14 20 INTGND INTGND MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
XR9      INTVCC 12 INTGND DC00400S  RES=10K
QQ6      15 14 16 DE283ASS
XD5      16 OUT INTGND DB3002AS
XD6      16 OUT INTGND DB3002AS
XD7      16 OUT INTGND DB3002AS
XD8      16 OUT INTGND DB3002AS
QQ7      OUT 6 INTGND DE283ASS
QQ8      OUT 6 INTGND DE283ASS
QQ9      OUT 6 INTGND DE283ASS
XD9      INTGND 28 INTGND DB3002AS
XD10     INTGND 28 INTGND DB3002AS
XD11     INTGND 28 INTGND DB3002AS
XD12     INTGND 28 INTGND DB3002AS
XD13     INTGND 28 INTGND DB3002AS
MM60     28 INTGND INTGND INTGND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
XD14     28 INTVCC INTGND DB0814AS
QQ10     24 INTGND INTGND DE283ASS
QQ11     24 INTGND INTGND DE283ASS
QQ12     24 INTGND INTGND DE283ASS
QQ13     24 INTGND INTGND DE283ASS
XR11     28 24 INTGND DB01E00S  RES=22.5
QQ14     OEBAR INTGND INTGND ESDXXXXS
QQ15     28 INTGND INTGND ESDXXXXS
QQ16     OUT INTGND INTGND ESDXXXXS
MM61     INTVCC OUT 25 INTVCC MHS4XPES L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
MM62     25 OUT INTGND INTGND MHS4XNES L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
XD15     11 26 INTGND DB0814AS
XD16     26 1 INTGND DB0814AS
M3M1   INTVCC D 27 INTVCC MHS4XPES L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3M2   27 D INTGND INTGND MHS4XNES L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3M3   28 27 INTGND INTGND MHS4XNES L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3M4   INTVCC 27 28 INTVCC MHS4XPES L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.EOM A16245S
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* Philips Semiconductors - ABT162441
.MACRO A162441S D EN OUT INTVCC INTGND
MM1      1 26 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM2      3 4 2 INTVCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM3      1 4 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 26 INTGND INTGND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 INTGND INTGND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM7      5 7 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM8      9 7 8 INTGND MHS4XNES L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
MM9      8 7 6 INTGND MHS4XNES L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
MM10     OUT 7 10 INTGND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM11     10 7 INTGND INTGND MHS4XNES L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM12     2 26 11 INTVCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM13     12 5 3 INTVCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM14     INTVCC 7 5 INTVCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
QQ1      INTVCC 11 6 DA0ACBSS
QQ2      11 11 13 DA06CBSS
QQ3      OUTA 6 INTGND DE283ASS
RR20     OUT OUTA 22.5
QQ4      15 14 16 DE283ASS
XQ5      15 17 14 INTGND DB14CASS
MM15     INTVCC OEBAR 18 INTVCC MHS4XPES L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM16     INTVCC 18 4 INTVCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM17     18 OEBAR INTGND INTGND MHS4XNES L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
MM18     4 18 INTGND INTGND MHS4XNES L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
XD1      13 OUTA INTGND DB0308AS
XR7      6 INTGND INTGND DC00400S  RES=1K
XD2      OUT 9 INTGND DB0814AS
XD3      16 OUT INTGND DB3002AS
XR8      INTVCC 15 INTGND DB01E00S  RES=15
MM19     INTVCC 4 19 INTVCC MHS4XPES L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM20     19 26 7 INTVCC MHS4XPES L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM21     7 4 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM22     7 26 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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MM23     21 18 20 INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM24     20 26 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM25     INTVCC 18 21 INTVCC MHS4XPES L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM26     INTVCC 26 21 INTVCC MHS4XPES L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM43     INTVCC 4 22 INTVCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     22 21 17 INTVCC MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     17 4 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM46     17 21 INTGND INTGND MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     INTVCC 4 23 INTVCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     23 21 14 INTVCC MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     14 4 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM58     14 21 INTGND INTGND MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
XR9      INTVCC 12 INTGND DC00400S  RES=10K
QQ6      15 14 16 DE283ASS
XD5      16 OUT INTGND DB3002AS
XD6      16 OUT INTGND DB3002AS
XD7      16 OUT INTGND DB3002AS
XD8      16 OUT INTGND DB3002AS
QQ7      OUTA 6 INTGND DE283ASS
QQ8      OUTA 6 INTGND DE283ASS
QQ9      OUTA 6 INTGND DE283ASS
QQ14     OEBAR INTGND INTGND ESDXXXXS
QQ15     26 INTGND INTGND ESDXXXXS
QQ16     OUT INTGND INTGND ESDXXXXS
M3M1   INTVCC D 25 INTVCC MHS4XPES L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3M2   25 D INTGND INTGND MHS4XNES L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3M3   26 25 INTGND INTGND MHS4XNES L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3M4   INTVCC 25 26 INTVCC MHS4XPES L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
XD15     24 1 INTGND DB0814AS
XD16     11 24 INTGND DB0814AS
RR13     INTGND D 10MEG
.EOM A162441S
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* Philips Semiconductors - ABT162451
.MACRO A162451S D EN OUT INTVCC INTGND
MM1      1 28 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM2      3 4 2 INTVCC MHS4XPES L=1.0U W-39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM3      1 4 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM4      1 5 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM5      6 28 INTGND INTGND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM6      6 4 INTGND INTGND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
MM7      5 7 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM8      8 7 9 INTGND MHS4XNES L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
MM9      9 7 6 INTGND MHS4XNES L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
MM10     OUT 7 10 INTGND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
MM11     10 7 INTGND INTGND MHS4XNES L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
MM12     2 28 11 INTVCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM13     12 5 3 INTVCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM14     INTVCC 7 5 INTVCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
QQ1      INTVCC 11 6 DA0ACBSS
QQ2      11 11 13 DA06CBSS
QQ3      OUTA 6 INTGND DE283ASS
RR20     OUT OUTA 22.5
QQ4      15 14 16 DE283ASS
XQ5      15 17 14 INTGND DB14CASS
MM15     INTVCC OEBAR 18 INTVCC MHS4XPES L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
MM16     INTVCC 18 4 INTVCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
MM17     18 OEBAR INTGND INTGND MHS4XNES L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
MM18     4 18 INTGND INTGND MHS4XNES L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
XD1      13 OUTA INTGND DB0308AS
XR7      6 INTGND INTGND DC00400S  RES=1K
XD2      OUT 8 INTGND DB0814AS
XD3      16 OUT INTGND DB3002AS
XR8      INTVCC 15 INTGND DB01E00S  RES=15
MM19     INTVCC 4 19 INTVCC MHS4XPES L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM20     19 28 7 INTVCC MHS4XPES L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
MM21     7 4 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM22     7 28 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM23     20 18 21 INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM24     21 28 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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MM25     INTVCC 18 20 INTVCC MHS4XPES L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM26     INTVCC 28 20 INTVCC MHS4XPES L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
MM43     INTVCC 4 22 INTVCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM44     22 20 17 INTVCC MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM45     17 4 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM46     17 20 INTGND INTGND MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
MM55     INTVCC 4 23 INTVCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
MM56     23 20 14 INTVCC MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
MM57     14 4 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
MM58     14 20 INTGND INTGND MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
XR9      INTVCC 12 INTGND DC00400S  RES=10K
QQ6      15 14 16 DE283ASS
XD5      16 OUT INTGND DB3002AS
XD6      16 OUT INTGND DB3002AS
XD7      16 OUT INTGND DB3002AS
XD8      16 OUT INTGND DB3002AS
QQ7      OUTA 6 INTGND DE283ASS
QQ8      OUTA 6 INTGND DE283ASS
QQ9      OUTA 6 INTGND DE283ASS
XD9      INTGND 28 INTGND DB3002AS
XD10     INTGND 28 INTGND DB3002AS
XD11     INTGND 28 INTGND DB3002AS
XD12     INTGND 28 INTGND DB3002AS
XD13     INTGND 28 INTGND DB3002AS
MM60     28 INTGND INTGND INTGND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
XD14     28 INTVCC INTGND DB0814AS
QQ10     24 INTGND INTGND DE283ASS
QQ11     24 INTGND INTGND DE283ASS
QQ12     24 INTGND INTGND DE283ASS
QQ13     24 INTGND INTGND DE283ASS
XR11     28 24 INTGND DB01E00S  RES=22.5
QQ14     OEBAR INTGND INTGND ESDXXXXS
QQ15     28 INTGND INTGND ESDXXXXS
QQ16     OUT INTGND INTGND ESDXXXXS
MM61     INTVCC OUT 25 INTVCC MHS4XPES L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
MM62     25 OUT INTGND INTGND MHS4XNES L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
XD15     11 26 INTGND DB0814AS
XD16     26 1 INTGND DB0814AS
M3M1   INTVCC D 27 INTVCC MHS4XPES L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3M2   27 D INTGND INTGND MHS4XNES L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3M3   28 27 INTGND INTGND MHS4XNES L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3M4   INTVCC 27 28 INTVCC MHS4XPES L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.EOM A162451S
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A16NOMPS.LIB Subcircuit

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*****************************************************************************
* ABT16 PSPICE SUBCIRCUIT LIBRARY
* A16NOMPS.LIB
* NOMINAL PROCESS CORNER
* STANDARD LOGIC PRODUCT GROUP
* PHILIPS SEMICONDUCTORS
* 3/31/1995
*****************************************************************************
.SUBCKT INV1 D E Q VCC
* USE THIS MODEL FOR ABT16240 (INVERTING PART)
*    IN   OUT   INT_VCC   INT_GND    (ENABLE)
X1   3     90     99         6           INBUFFN
*    IN   OUT   INT_VCC   INT_GND    (SIGNAL)
X2   1     91     99         6           MOSINVN
*    D     EN    OUT    INT_VCC   INT_GND
X3   91    90     2       99         6      OUTBUFFN
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1
*
.SUBCKT INV1_1 D E Q VCC
* USE THIS MODEL FOR ABT16240-1 (INVERTING PART)
*    IN   OUT   INT_VCC   INT_GND    (ENABLE)
X1   3     90     99         6           INBUFFN
*    IN   OUT   INT_VCC   INT_GND    (SIGNAL)
X2   1     91     99         6           MOSINVN
*    D     EN    OUT    INT_VCC   INT_GND
X3   91    90     2       99         6      OUTBUF1N
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1_1
.SUBCKT INV2 D E Q VCC
*
*    IN   OUT   INT_VCC   INT_GND    (ENABLE)
X1   3     90     99         6           INBUFFN
*    IN   OUT   INT_VCC   INT_GND    (SIGNAL)
X2   1     91     99         6           MOSINVN
*    D     EN    OUT    INT_VCC   INT_GND
X3   91    90     2       99         6      OUTBUFFN
*    IN   OUT   INT_VCC   INT_GND
X4    2    1      99         6           BCKLOADN
```

```
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV2
.SUBCKT NINV D E Q VCC
* USE THIS MODEL FOR ABT16273  -373B  -374B  -541
*  -821  -823  -825  -827  -841  (NON-INVERTING)
*   IN  OUT  INT_VCC  INT_GND  (ENABLE)
X1  3    90    99       6         INBUFFN
*   IN  OUT  INT_VCC  INT_GND  (SIGNAL)
X2  1    91    99       6         INBUFFN
*   D    EN   OUT   INT_VCC  INT_GND
X3  91   90    2      99       6     OUTBUFFN
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINV
*
.SUBCKT NINVB D E Q VCC
* USE THIS MODEL FOR ABT16500  -501  -543  -646  -652  -899
* -952  -1543
*   IN  OUT  INT_VCC  INT_GND  (ENABLE)
X1  3    90    99       6         INBUFFN
*   IN  OUT  INT_VCC  INT_GND  (SIGNAL)
X2  1    91    99       6         INBUFFN
*   D    EN   OUT   INT_VCC  INT_GND
X3  91   90    2      99       6     OUTBUFFN
*   IN  OUT  INT_VCC  INT_GND
X4   2   1     99       6         BCKLOADN
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINVB
*
```

```
.SUBCKT A16244 D E Q VCC
* USE THIS MODEL FOR ABT16244S
*   D     EN    OUT    INT_VCC   INT_GND
X3  1      3     2        99       6      A16244N
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16244
*
.SUBCKT A16245 D E Q VCC
* USE THIS MODEL FOR ABT16245B
*   D     EN    OUT    INT_VCC   INT_GND
X3  1      3     2        99       6      A16245N
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16245
*
.SUBCKT A16244_1 D E Q VCC
* USE THIS MODEL FOR ABT16244-1
*   D     EN    OUT    INT_VCC   INT_GND
X3  1      3     2        99       6      A162441N
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16244_1
*
```

```
.SUBCKT A16245_1 D E Q VCC
* USE THIS MODEL FOR ABT16245A-1
*    D     EN    OUT    INT_VCC   INT_GND
X3   1      3     2       99        6      A162451N
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16245_1
*
* Philips Semiconductors - MOSINV
.SUBCKT MOSINVN IN OUT INT_VCC INT_GND
M_M1      INT_VCC IN 01 INT_VCC MHS4XPEN L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M_M2      01 IN INT_GND INT_GND MHS4XNEN L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M_M3      OUT 01 INT_GND INT_GND MHS4XNEN L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M_M4      INT_VCC 01 OUT INT_VCC MHS4XPEN L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.ENDS MOSINVN
* Philips Semiconductors - INBUFF
.SUBCKT INBUFFN    IN OUT INT_VCC INT_GND
M_M1      OUT IN INT_GND INT_GND MHS4XNEN L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M_M2      INT_VCC IN 01 01 MHS4XPEN L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
Q_Q1      IN INT_GND INT_GND ESDXXXXN
R_R1      01 OUT 100
.ENDS INBUFFN
* Philips Semiconductors - OUTBUFF
.SUBCKT OUTBUFFN D EN OUT INT_VCC INT_GND
M_M2      02 03 01 INT_VCC MHS4XPEN L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
M_M3      01 04 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M4      01 05 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M5      06 05 INT_GND INT_GND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M6      06 04 INT_GND INT_GND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M13     07 04 02 INT_VCC MHS4XPEN L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
Q_Q1      INT_VCC 08 05 DA04CASN
Q_Q2      01 01 09 DA0ACBSN
Q_Q3      OUT 06 INT_GND DE283ASN
Q_Q4      11 10 12 DE283ASN
X_Q5      11 13 10 [INT_GND] DB14CASN
X_D1      09 OUT INT_GND DB0814AN
X_R7      06 INT_GND INT_GND DC00400N PARAMS: RES=1K
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X_D3      12 OUT INT_GND DB3002AN
X_R8      INT_VCC 11 INT_GND DB01E00N PARAMS: RES=15
M_M43     INT_VCC 04 14 INT_VCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M44     14 D 13 INT_VCC MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M45     13 04 INT_GND INT_GND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_M46     13 D INT_GND INT_GND MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
M_M55     INT_VCC 04 15 INT_VCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M56     15 D 10 INT_VCC MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M57     10 04 INT_GND INT_GND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_M58     10 D INT_GND INT_GND MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
X_R9      INT_VCC 07 INT_GND DC00400N PARAMS: RES=10K
Q_Q6      11 10 12 DE283ASN
X_D5      12 OUT INT_GND DB3002AN
X_D6      12 OUT INT_GND DB3002AN
X_D7      12 OUT INT_GND DB3002AN
X_D8      12 OUT INT_GND DB3002AN
Q_Q7      OUT 06 INT_GND DE283ASN
Q_Q8      OUT 06 INT_GND DE283ASN
Q_Q9      OUT 06 INT_GND DE283ASN
M_M61     INT_VCC 17 16 INT_VCC MHS4XPEN L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
M_M62     16 EN 18 INT_GND MHS4XNEN L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
M_M63     18 D 06 INT_GND MHS4XNEN L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
M_M64     17 OUT INT_GND INT_GND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_M65     INT_VCC OUT 17 INT_VCC MHS4XPEN L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M_M66     OUT EN 19 INT_GND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_M67     19 D INT_GND INT_GND MHS4XNEN L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
M_M68     03 D INT_GND INT_GND MHS4XNEN L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
M_M69     INT_VCC D 03 INT_VCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M70     08 D INT_GND INT_GND MHS4XNEN L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M_M71     INT_VCC D 08 INT_VCC MHS4XPEN L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
M_M72     05 D INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M73     INT_VCC D 05 INT_VCC MHS4XPEN L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
Q_Q14     INT_VCC 01 06 DA0ACBSN
Q_Q15     OUT INT_GND INT_GND ESDXXXXN
M_M74     04 EN INT_GND INT_GND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M75     INT_VCC EN 04 INT_VCC MHS4XPEN L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
.ENDS OUTBUFFN
```

```
* Philips Semiconductors - OUTBUFF1N
.SUBCKT OUTBUF1N D EN OUT INT_VCC INT_GND
M_M2      02 03 01 INT_VCC MHS4XPEN L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
M_M3      01 04 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M4      01 05 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M5      06 05 INT_GND INT_GND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M6      06 04 INT_GND INT_GND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M13     07 04 02 INT_VCC MHS4XPEN L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
Q_Q1      INT_VCC 08 05 DA04CASN
Q_Q2      01 01 09 DA0ACBSN
Q_Q3      OUTA 06 INT_GND DE283ASN
RR20      OUT OUTA 22.5
Q_Q4      11 10 12 DE283ASN
X_Q5      11 13 10 [INT_GND] DB14CASN
X_D1      09 OUTA INT_GND DB0814AN
X_R7      06 INT_GND INT_GND DC00400N PARAMS: RES=1K
X_D3      12 OUT INT_GND DB3002AN
X_R8      INT_VCC 11 INT_GND DB01E00N PARAMS: RES=15
M_M43     INT_VCC 04 14 INT_VCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M44     14 D 13 INT_VCC MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M45     13 04 INT_GND INT_GND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_M46     13 D INT_GND INT_GND MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
M_M55     INT_VCC 04 15 INT_VCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M56     15 D 10 INT_VCC MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M57     10 04 INT_GND INT_GND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_M58     10 D INT_GND INT_GND MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
X_R9      INT_VCC 07 INT_GND DC00400N PARAMS: RES=10K
Q_Q6      11 10 12 DE283ASN
X_D5      12 OUT INT_GND DB3002AN
X_D6      12 OUT INT_GND DB3002AN
X_D7      12 OUT INT_GND DB3002AN
X_D8      12 OUT INT_GND DB3002AN
Q_Q7      OUTA 06 INT_GND DE283ASN
Q_Q8      OUTA 06 INT_GND DE283ASN
Q_Q9      OUTA 06 INT_GND DE283ASN
M_M61     INT_VCC 17 16 INT_VCC MHS4XPEN L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
M_M62     16 EN 18 INT_GND MHS4XNEN L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
M_M63     18 D 06 INT_GND MHS4XNEN L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
M_M64     17 OUT INT_GND INT_GND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_M65     INT_VCC OUT 17 INT_VCC MHS4XPEN L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
```

```
M_M66     OUT EN 19 INT_GND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_M67     19 D INT_GND INT_GND MHS4XNEN L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
M_M68     03 D INT_GND INT_GND MHS4XNEN L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
M_M69     INT_VCC D 03 INT_VCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M70     08 D INT_GND INT_GND MHS4XNEN L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M_M71     INT_VCC D 08 INT_VCC MHS4XPEN L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
M_M72     05 D INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M73     INT_VCC D 05 INT_VCC MHS4XPEN L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
Q_Q14     INT_VCC 01 06 DA0ACBSN
Q_Q15     OUT INT_GND INT_GND ESDXXXXN
M_M74     04 EN INT_GND INT_GND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M75     INT_VCC EN 04 INT_VCC MHS4XPEN L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
.ENDS OUTBUF1N
* Philips Semiconductors - BCKLOAD
.SUBCKT BCKLOADN IN OUT INT_VCC INT_GND
X_D9      INT_GND IN INT_GND DB3002AN
X_D10     INT_GND IN INT_GND DB3002AN
X_D11     INT_GND IN INT_GND DB3002AN
X_D12     INT_GND IN INT_GND DB3002AN
X_D13     INT_GND IN INT_GND DB3002AN
M_M60     IN INT_GND INT_GND INT_GND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
X_D14     IN INT_VCC INT_GND DB0814AN
Q_Q10     IN INT_GND INT_GND DE283ASN
Q_Q11     IN INT_GND INT_GND DE283ASN
Q_Q12     IN INT_GND INT_GND DE283ASN
Q_Q13     IN INT_GND INT_GND DE283ASN
M_M61     INT_VCC OUT 01 01 MHS4XPEN L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M_M62     01 OUT INT_GND INT_GND MHS4XNEN L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
.ENDS BCKLOADN
* Philips Semiconductors - BUSHOLD1
.SUBCKT BUSHLD1N BH INT_GND INT_VCC
X_D1      01 02 INT_GND DB3002AN
Q_Q1      03 03 01 DE283ASN
X_R1      02 BH INT_GND DC00400N PARAMS: RES=2K
X_R2      BH 04 INT_GND DC00400N PARAMS: RES=5K
M_M4      04 05 INT_GND INT_GND MHS4XNEN L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
M_M1      05 BH INT_GND INT_GND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_M2      INT_VCC BH 05 05 MHS4XPEN L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
M_M3      INT_VCC 05 03 03 MHS4XPEN L=1.0U W=8.298U
+ AD=16.596P AS=16.596P PD=20.596U PS=20.596U NRD=0.241 NRS=0.241
.ENDS BUSHLD1N
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* Philips Semiconductors - ABT16244
.SUBCKT A16244N D EN OUT INT_VCC INT_GND
M_M1      01 26 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M2      03 04 02 INT_VCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M3      01 04 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M4      01 05 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M5      06 26 INT_GND INT_GND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M6      06 04 INT_GND INT_GND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M7      05 07 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M8      09 07 08 INT_GND MHS4XNEN L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
M_M9      08 07 06 INT_GND MHS4XNEN L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
M_M10     OUT 07 10 INT_GND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_M11     10 07 INT_GND INT_GND MHS4XNEN L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
M_M12     02 26 11 INT_VCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M13     12 05 03 INT_VCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M14     INT_VCC 07 05 INT_VCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
Q_Q1      INT_VCC 11 06 DA0ACBSN
Q_Q2      11 11 13 DA06CBSN
Q_Q3      OUT 06 INT_GND DE283ASN
Q_Q4      15 14 16 DE283ASN
X_Q5      15 17 14 INT_GND DB14CASN
M_M15     INT_VCC OEBAR 18 INT_VCC MHS4XPEN L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
M_M16     INT_VCC 18 04 INT_VCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M17     18 OEBAR INT_GND INT_GND MHS4XNEN L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
M_M18     04 18 INT_GND INT_GND MHS4XNEN L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
X_D1      13 OUT INT_GND DB0308AN
X_R7      06 INT_GND INT_GND DC00400N PARAMS: RES=1K
X_D2      OUT 09 INT_GND DB0814AN
X_D3      16 OUT INT_GND DB3002AN
X_R8      INT_VCC 15 INT_GND DB01E00N PARAMS: RES=15
M_M19     INT_VCC 04 19 INT_VCC MHS4XPEN L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
M_M20     19 26 07 INT_VCC MHS4XPEN L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
M_M21     07 04 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M22     07 26 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M23     21 18 20 INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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M_M24     20 26 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M25     INT_VCC 18 21 INT_VCC MHS4XPEN L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
M_M26     INT_VCC 26 21 INT_VCC MHS4XPEN L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
M_M43     INT_VCC 04 22 INT_VCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M44     22 21 17 INT_VCC MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M45     17 04 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M46     17 21 INT_GND INT_GND MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
M_M55     INT_VCC 04 23 INT_VCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M56     23 21 14 INT_VCC MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M57     14 04 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M58     14 21 INT_GND INT_GND MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
X_R9      INT_VCC 12 INT_GND DC00400N PARAMS: RES=10K
Q_Q6      15 14 16 DE283ASN
X_D5      16 OUT INT_GND DB3002AN
X_D6      16 OUT INT_GND DB3002AN
X_D7      16 OUT INT_GND DB3002AN
X_D8      16 OUT INT_GND DB3002AN
Q_Q7      OUT 06 INT_GND DE283ASN
Q_Q8      OUT 06 INT_GND DE283ASN
Q_Q9      OUT 06 INT_GND DE283ASN
Q_Q14     OEBAR INT_GND INT_GND ESDXXXXN
Q_Q15     26 INT_GND INT_GND ESDXXXXN
Q_Q16     OUT INT_GND INT_GND ESDXXXXN
M3_M1   INT_VCC D 25 INT_VCC MHS4XPEN L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3_M2   25 D INT_GND INT_GND MHS4XNEN L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3_M3   26 25 INT_GND INT_GND MHS4XNEN L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3_M4   INT_VCC 25 26 INT_VCC MHS4XPEN L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
X_D15     24 01 INT_GND DB0814AN
X_D16     11 24 INT_GND DB0814AN
R_R13     INT_GND D 10MEG
.ENDS A16244N
* Philips Semiconductors - ABT16245
.SUBCKT A16245N D EN OUT INT_VCC INT_GND
M_M1      01 28 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M2      03 04 02 INT_VCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M3      01 04 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M4      01 05 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M5      06 28 INT_GND INT_GND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
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M_M6      06 04 INT_GND INT_GND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M7      05 07 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M8      08 07 09 INT_GND MHS4XNEN L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
M_M9      09 07 06 INT_GND MHS4XNEN L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
M_M10     OUT 07 10 INT_GND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_M11     10 07 INT_GND INT_GND MHS4XNEN L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
M_M12     02 28 11 INT_VCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M13     12 05 03 INT_VCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M14     INT_VCC 07 05 INT_VCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
Q_Q1      INT_VCC 11 06 DA0ACBSN
Q_Q2      11 11 13 DA06CBSN
Q_Q3      OUT 06 INT_GND DE283ASN
Q_Q4      15 14 16 DE283ASN
X_Q5      15 17 14 [INT_GND] DB14CASN
M_M15     INT_VCC OEBAR 18 INT_VCC MHS4XPEN L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
M_M16     INT_VCC 18 04 INT_VCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M17     18 OEBAR INT_GND INT_GND MHS4XNEN L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
M_M18     04 18 INT_GND INT_GND MHS4XNEN L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
X_D1      13 OUT INT_GND DB0308AN
X_R7      06 INT_GND INT_GND DC00400N PARAMS: RES=1K
X_D2      OUT 08 INT_GND DB0814AN
X_D3      16 OUT INT_GND DB3002AN
X_R8      INT_VCC 15 INT_GND DB01E00N PARAMS: RES=15
M_M19     INT_VCC 04 19 INT_VCC MHS4XPEN L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
M_M20     19 28 07 INT_VCC MHS4XPEN L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
M_M21     07 04 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M22     07 28 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M23     20 18 21 INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M24     21 28 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M25     INT_VCC 18 20 INT_VCC MHS4XPEN L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
M_M26     INT_VCC 28 20 INT_VCC MHS4XPEN L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
M_M43     INT_VCC 04 22 INT_VCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M44     22 20 17 INT_VCC MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M45     17 04 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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M_M46     17 20 INT_GND INT_GND MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
M_M55     INT_VCC 04 23 INT_VCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M56     23 20 14 INT_VCC MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M57     14 04 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M58     14 20 INT_GND INT_GND MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
X_R9      INT_VCC 12 INT_GND DC00400N PARAMS: RES=10K
Q_Q6      15 14 16 DE283ASN
X_D5      16 OUT INT_GND DB3002AN
X_D6      16 OUT INT_GND DB3002AN
X_D7      16 OUT INT_GND DB3002AN
X_D8      16 OUT INT_GND DB3002AN
Q_Q7      OUT 06 INT_GND DE283ASN
Q_Q8      OUT 06 INT_GND DE283ASN
Q_Q9      OUT 06 INT_GND DE283ASN
X_D9      INT_GND 28 INT_GND DB3002AN
X_D10     INT_GND 28 INT_GND DB3002AN
X_D11     INT_GND 28 INT_GND DB3002AN
X_D12     INT_GND 28 INT_GND DB3002AN
X_D13     INT_GND 28 INT_GND DB3002AN
M_M60     28 INT_GND INT_GND INT_GND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
X_D14     28 INT_VCC INT_GND DB0814AN
Q_Q10     24 INT_GND INT_GND DE283ASN
Q_Q11     24 INT_GND INT_GND DE283ASN
Q_Q12     24 INT_GND INT_GND DE283ASN
Q_Q13     24 INT_GND INT_GND DE283ASN
X_R11     28 24 INT_GND DB01E00N PARAMS: RES=22.5
Q_Q14     OEBAR INT_GND INT_GND ESDXXXXN
Q_Q15     28 INT_GND INT_GND ESDXXXXN
Q_Q16     OUT INT_GND INT_GND ESDXXXXN
M_M61     INT_VCC OUT 25 INT_VCC MHS4XPEN L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
M_M62     25 OUT INT_GND INT_GND MHS4XNEN L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
X_D15     11 26 INT_GND DB0814AN
X_D16     26 01 INT_GND DB0814AN
M_U3_M1   INT_VCC D 27 INT_VCC MHS4XPEN L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M_U3_M2   27 D INT_GND INT_GND MHS4XNEN L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M_U3_M3   28 27 INT_GND INT_GND MHS4XNEN L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M_U3_M4   INT_VCC 27 28 INT_VCC MHS4XPEN L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.ENDS A16245N
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* Philips Semiconductors - ABT162441N
.SUBCKT A162441N D EN OUT INT_VCC INT_GND
M_M1      01 26 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M2      03 04 02 INT_VCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M3      01 04 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M4      01 05 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M5      06 26 INT_GND INT_GND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M6      06 04 INT_GND INT_GND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M7      05 07 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M8      09 07 08 INT_GND MHS4XNEN L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
M_M9      08 07 06 INT_GND MHS4XNEN L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
M_M10     OUT 07 10 INT_GND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_M11     10 07 INT_GND INT_GND MHS4XNEN L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
M_M12     02 26 11 INT_VCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M13     12 05 03 INT_VCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M14     INT_VCC 07 05 INT_VCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
Q_Q1      INT_VCC 11 06 DA0ACBSN
Q_Q2      11 11 13 DA06CBSN
Q_Q3      OUTA 06 INT_GND DE283ASN
RR20      OUT OUTA 22.5
Q_Q4      15 14 16 DE283ASN
X_Q5      15 17 14 INT_GND DB14CASN
M_M15     INT_VCC OEBAR 18 INT_VCC MHS4XPEN L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
M_M16     INT_VCC 18 04 INT_VCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M17     18 OEBAR INT_GND INT_GND MHS4XNEN L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
M_M18     04 18 INT_GND INT_GND MHS4XNEN L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
X_D1      13 OUTA INT_GND DB0308AN
X_R7      06 INT_GND INT_GND DC00400N PARAMS: RES=1K
X_D2      OUT 09 INT_GND DB0814AN
X_D3      16 OUT INT_GND DB3002AN
X_R8      INT_VCC 15 INT_GND DB01E00N PARAMS: RES=15
M_M19     INT_VCC 04 19 INT_VCC MHS4XPEN L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
M_M20     19 26 07 INT_VCC MHS4XPEN L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
M_M21     07 04 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M22     07 26 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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M_M23     21 18 20 INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M24     20 26 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M M25     INT_VCC 18 21 INT_VCC MHS4XPEN L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
M_M26     INT_VCC 26 21 INT_VCC MHS4XPEN L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
M_M43     INT_VCC 04 22 INT_VCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M44     22 21 17 INT_VCC MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M45     17 04 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M46     17 21 INT_GND INT_GND MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
M_M55     INT_VCC 04 23 INT_VCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M56     23 21 14 INT_VCC MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M57     14 04 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M58     14 21 INT_GND INT_GND MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
X_R9      INT_VCC 12 INT_GND DC00400N PARAMS: RES=10K
Q_Q6      15 14 16 DE283ASN
X_D5      16 OUT INT_GND DB3002AN
X_D6      16 OUT INT_GND DB3002AN
X_D7      16 OUT INT_GND DB3002AN
X_D8      16 OUT INT_GND DB3002AN
Q_Q7      OUTA 06 INT_GND DE283ASN
Q_Q8      OUTA 06 INT_GND DE283ASN
Q_Q9      OUTA 06 INT_GND DE283ASN
Q_Q14     OEBAR INT_GND INT_GND ESDXXXXN
Q_Q15     26 INT_GND INT_GND ESDXXXXN
Q_Q16     OUT INT_GND INT_GND ESDXXXXN
M3_M1   INT_VCC D 25 INT_VCC MHS4XPEN L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3_M2   25 D INT_GND INT_GND MHS4XNEN L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3_M3   26 25 INT_GND INT_GND MHS4XNEN L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3_M4   INT_VCC 25 26 INT_VCC MHS4XPEN L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
X_D15     24 01 INT_GND DB0814AN
X_D16     11 24 INT_GND DB0814AN
R_R13     INT_GND D 10MEG
.ENDS A162441N
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* Philips Semiconductors - ABT162451
.SUBCKT A162451N D EN OUT INT_VCC INT_GND
M_M1      01 28 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M2      03 04 02 INT_VCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M3      01 04 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M4      01 05 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M5      06 28 INT_GND INT_GND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M6      06 04 INT_GND INT_GND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M7      05 07 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M8      08 07 09 INT_GND MHS4XNEN L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
M_M9      09 07 06 INT_GND MHS4XNEN L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
M_M10     OUT 07 10 INT_GND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_M11     10 07 INT_GND INT_GND MHS4XNEN L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
M_M12     02 28 11 INT_VCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M13     12 05 03 INT_VCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M14     INT_VCC 07 05 INT_VCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
Q_Q1      INT_VCC 11 06 DA0ACBSN
Q_Q2      11 11 13 DA06CBSN
Q_Q3      OUTA 06 INT_GND DE283ASN
RR20      OUT OUTA 22.5
Q_Q4      15 14 16 DE283ASN
X_Q5      15 17 14 [INT_GND] DB14CASN
M_M15     INT_VCC OEBAR 18 INT_VCC MHS4XPEN L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
M_M16     INT_VCC 18 04 INT_VCC MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M17     18 OEBAR INT_GND INT_GND MHS4XNEN L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
M_M18     04 18 INT_GND INT_GND MHS4XNEN L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
X_D1      13 OUTA INT GND DB0308AN
X_R7      06 INT_GND INT_GND DC00400N PARAMS: RES=1K
X_D2      OUT 08 INT_GND DB0814AN
X_D3      16 OUT INT_GND DB3002AN
X_R8      INT_VCC 15 INT_GND DB01E00N PARAMS: RES=15
M_M19     INT_VCC 04 19 INT_VCC MHS4XPEN L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
M_M20     19 28 07 INT_VCC MHS4XPEN L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
M_M21     07 04 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M22     07 28 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M23     20 18 21 INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M24     21 28 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
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+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M25     INT_VCC 18 20 INT_VCC MHS4XPEN L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
M_M26     INT_VCC 28 20 INT_VCC MHS4XPEN L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
M_M43     INT_VCC 04 22 INT_VCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M44     22 20 17 INT_VCC MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M45     17 04 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M46     17 20 INT_GND INT_GND MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
M_M55     INT_VCC 04 23 INT_VCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M56     23 20 14 INT_VCC MHS4XPEN L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M57     14 04 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M58     14 20 INT_GND INT_GND MHS4XNEN L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
X_R9      INT_VCC 12 INT_GND DC00400N PARAMS: RES=10K
Q_Q6      15 14 16 DE283ASN
X_D5      16 OUT INT_GND DB3002AN
X_D6      16 OUT INT_GND DB3002AN
X_D7      16 OUT INT_GND DB3002AN
X_D8      16 OUT INT_GND DB3002AN
Q_Q7      OUTA 06 INT_GND DE283ASN
Q_Q8      OUTA 06 INT_GND DE283ASN
Q_Q9      OUTA 06 INT_GND DE283ASN
X_D9      INT_GND 28 INT_GND DB3002AN
X_D10     INT_GND 28 INT_GND DB3002AN
X_D11     INT_GND 28 INT_GND DB3002AN
X_D12     INT_GND 28 INT_GND DB3002AN
X_D13     INT_GND 28 INT_GND DB3002AN
M_M60     28 INT_GND INT_GND INT_GND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
X_D14     28 INT_VCC INT_GND DB0814AN
Q_Q10     24 INT_GND INT_GND DE283ASN
Q_Q11     24 INT_GND INT_GND DE283ASN
Q_Q12     24 INT_GND INT_GND DE283ASN
Q_Q13     24 INT_GND INT_GND DE283ASN
X_R11     28 24 INT_GND DB01E00N PARAMS: RES=22.5
Q_Q14     OEBAR INT_GND INT_GND ESDXXXXN
Q_Q15     28 INT_GND INT_GND ESDXXXXN
Q_Q16     OUT INT_GND INT_GND ESDXXXXN
M_M61     INT_VCC OUT 25 INT_VCC MHS4XPEN L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
M_M62     25 OUT INT_GND INT_GND MHS4XNEN L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
X_D15     11 26 INT_GND DB0814AN
X_D16     26 01 INT_GND DB0814AN
M_U3_M1   INT_VCC D 27 INT_VCC MHS4XPEN L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M_U3_M2   27 D INT_GND INT_GND MHS4XNEN L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M_U3_M3   28 27 INT_GND INT_GND MHS4XNEN L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M_U3_M4   INT_VCC 27 28 INT_VCC MHS4XPEN L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.ENDS A162451N
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A16FASPS.LIB Subcircuit

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*****************************************************************************
* ABT16 PSPICE SUBCIRCUIT LIBRARY
* A16FASPS.LIB
* FAST PROCESS CORNER
* STANDARD LOGIC PRODUCT GROUP
* PHILIPS SEMICONDUCTORS
* 3/31/1995
*****************************************************************************
.SUBCKT INV1 D E Q VCC
* USE THIS MODEL FOR ABT16240 (INVERTING PART)
*    IN   OUT   INT_VCC   INT_GND    (ENABLE)
X1   3     90     99        6           INBUFFF
*    IN   OUT   INT_VCC   INT_GND    (SIGNAL)
X2   1     91     99        6           MOSINVF
*    D     EN    OUT    INT_VCC   INT_GND
X3   91    90     2       99        6      OUTBUFFF
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1
*
.SUBCKT INV1_1 D E Q VCC
* USE THIS MODEL FOR ABT16240-1 (INVERTING PART)
*    IN   OUT   INT_VCC   INT_GND    (ENABLE)
X1   3     90     99        6           INBUFFF
*    IN   OUT   INT_VCC   INT_GND    (SIGNAL)
X2   1     91     99        6           MOSINVF
*    D     EN    OUT    INT_VCC   INT_GND
X3   91    90     2       99        6      OUTBUF1F
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1_1
.SUBCKT INV2 D E Q VCC
*
*    IN   OUT   INT_VCC   INT_GND    (ENABLE)
X1   3     90     99        6           INBUFFF
*    IN   OUT   INT_VCC   INT_GND    (SIGNAL)
X2   1     91     99        6           MOSINVF
*    D     EN    OUT    INT_VCC   INT_GND
X3   91    90     2       99        6      OUTBUFFF
*    IN   OUT   INT_VCC   INT_GND
X4    2    1      99        6           BCKLOADN
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*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV2
.SUBCKT NINV D E Q VCC
* USE THIS MODEL FOR ABT16273  -373B  -374B  -541
*  -821  -823  -825  -827  -841  (NON-INVERTING)
*   IN  OUT  INT_VCC  INT_GND  (ENABLE)
X1  3    90    99       6         INBUFFF
*   IN  OUT  INT_VCC  INT_GND  (SIGNAL)
X2  1    91    99       6         INBUFFF
*   D    EN   OUT   INT_VCC  INT_GND
X3  91   90    2      99       6     OUTBUFFF
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINV
*
.SUBCKT NINVB D E Q VCC
* USE THIS MODEL FOR ABT16500  -501  -543  -646  -652  -899
* -952  -1543
*   IN  OUT  INT_VCC  INT_GND  (ENABLE)
X1  3    90    99       6         INBUFFF
*   IN  OUT  INT_VCC  INT_GND  (SIGNAL)
X2  1    91    99       6         INBUFFF
*   D    EN   OUT   INT_VCC  INT_GND
X3  91   90    2      99       6     OUTBUFFF
*   IN  OUT  INT_VCC  INT_GND
X4   2   1     99       6          BCKLOADF
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINVB
*
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.SUBCKT A16244 D E Q VCC
* USE THIS MODEL FOR ABT16244A
*    D     EN    OUT    INT_VCC   INT_GND
X3   1      3     2        99       6      A16244F
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16244
*
.SUBCKT A16245 D E Q VCC
* USE THIS MODEL FOR ABT16245B
*    D     EN    OUT    INT_VCC   INT_GND
X3   1      3     2        99       6      A16245F
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16245
.SUBCKT A16244_1 D E Q VCC
* USE THIS MODEL FOR ABT16244-1
*    D     EN    OUT    INT_VCC   INT_GND
X3   1      3     2        99       6      A162441F
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16244_1
*
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.SUBCKT A16245_1 D E Q VCC
* USE THIS MODEL FOR ABT16245A-1
*   D    EN   OUT   INT_VCC  INT_GND
X3  1     3    2      99       6     A162451F
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16245_1
*
* Philips Semiconductors - MOSINV
.SUBCKT MOSINVF IN OUT INT_VCC INT_GND
M_M1     INT_VCC IN 01 INT_VCC MHS4XPEF L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M_M2     01 IN INT_GND INT_GND MHS4XNEF L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M_M3     OUT 01 INT_GND INT_GND MHS4XNEF L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M_M4     INT_VCC 01 OUT INT_VCC MHS4XPEF L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.ENDS MOSINVF
* Philips Semiconductors - INBUFF
.SUBCKT INBUFFF   IN OUT INT_VCC INT_GND
M_M1     OUT IN INT_GND INT_GND MHS4XNEF L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M_M2     INT_VCC IN 01 01 MHS4XPEF L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
Q_Q1     IN INT_GND INT_GND ESDXXXXF
R_R1     01 OUT 100
.ENDS INBUFFF
* Philips Semiconductors - OUTBUFF
.SUBCKT OUTBUFFF D EN OUT INT_VCC INT_GND
M_M2     02 03 01 INT_VCC MHS4XPEF L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
M_M3     01 04 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M4     01 05 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M5     06 05 INT_GND INT_GND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M6     06 04 INT_GND INT_GND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M13    07 04 02 INT_VCC MHS4XPEF L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
Q_Q1     INT_VCC 08 05 DA04CASF
Q_Q2     01 01 09 DA0ACBSF
Q_Q3     OUT 06 INT_GND DE283ASF
Q_Q4     11 10 12 DE283ASF
X_Q5     11 13 10 [INT_GND] DB14CASF
X_D1     09 OUT INT_GND DB0814AF
X_R7     06 INT_GND INT_GND DC00400F PARAMS: RES=1K
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X_D3      12 OUT INT_GND DB3002AF
X_R8      INT_VCC 11 INT_GND DB01E00F PARAMS: RES=15
M_M43     INT_VCC 04 14 INT_VCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M44     14 D 13 INT_VCC MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M45     13 04 INT_GND INT_GND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_M46     13 D INT_GND INT_GND MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
M_M55     INT_VCC 04 15 INT_VCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M56     15 D 10 INT_VCC MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M57     10 04 INT_GND INT_GND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_M58     10 D INT_GND INT_GND MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
X_R9      INT_VCC 07 INT_GND DC00400F PARAMS: RES=10K
Q_Q6      11 10 12 DE283ASF
X_D5      12 OUT INT_GND DB3002AF
X_D6      12 OUT INT_GND DB3002AF
X_D7      12 OUT INT_GND DB3002AF
X_D8      12 OUT INT_GND DB3002AF
Q_Q7      OUT 06 INT_GND DE283ASF
Q_Q8      OUT 06 INT_GND DE283ASF
Q_Q9      OUT 06 INT_GND DE283ASF
M_M61     INT_VCC 17 16 INT_VCC MHS4XPEF L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
M_M62     16 EN 18 INT_GND MHS4XNEF L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
M_M63     18 D 06 INT_GND MHS4XNEF L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
M_M64     17 OUT INT_GND INT_GND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_M65     INT_VCC OUT 17 INT_VCC MHS4XPEF L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M_M66     OUT EN 19 INT_GND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_M67     19 D INT_GND INT_GND MHS4XNEF L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
M_M68     03 D INT_GND INT_GND MHS4XNEF L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
M_M69     INT_VCC D 03 INT_VCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M70     08 D INT_GND INT_GND MHS4XNEF L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M_M71     INT_VCC D 08 INT_VCC MHS4XPEF L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
M_M72     05 D INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M73     INT_VCC D 05 INT_VCC MHS4XPEF L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
Q_Q14     INT_VCC 01 06 DA0ACBSF
Q_Q15     OUT INT_GND INT_GND ESDXXXXF
M_M74     04 EN INT_GND INT_GND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M75     INT_VCC EN 04 INT_VCC MHS4XPEF L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
.ENDS OUTBUFFF
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* Philips Semiconductors - OUTBUFF1
.SUBCKT OUTBUF1F D EN OUT INT_VCC INT_GND
M_M2      02 03 01 INT_VCC MHS4XPEF L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
M_M3      01 04 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M4      01 05 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M5      06 05 INT_GND INT_GND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M6      06 04 INT_GND INT_GND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M13     07 04 02 INT_VCC MHS4XPEF L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
Q_Q1      INT_VCC 08 05 DA04CASF
Q_Q2      01 01 09 DA0ACBSF
Q_Q3      OUTA 06 INT_GND DE283ASF
RR20      OUT OUTA 22.5
Q_Q4      11 10 12 DE283ASF
X_Q5      11 13 10 [INT_GND] DB14CASF
X_D1      09 OUTA INT_GND DB0814AF
X_R7      06 INT_GND INT_GND DC00400F PARAMS: RES=1K
X_D3      12 OUT INT_GND DB3002AF
X_R8      INT_VCC 11 INT_GND DB01E00F PARAMS: RES=15
M_M43     INT_VCC 04 14 INT_VCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M44     14 D 13 INT_VCC MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M45     13 04 INT_GND INT_GND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_M46     13 D INT_GND INT_GND MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
M_M55     INT_VCC 04 15 INT_VCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M56     15 D 10 INT_VCC MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M57     10 04 INT_GND INT_GND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_M58     10 D INT_GND INT_GND MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
X_R9      INT_VCC 07 INT_GND DC00400F PARAMS: RES=10K
Q_Q6      11 10 12 DE283ASF
X_D5      12 OUT INT_GND DB3002AF
X_D6      12 OUT INT_GND DB3002AF
X_D7      12 OUT INT_GND DB3002AF
X_D8      12 OUT INT_GND DB3002AF
Q_Q7      OUTA 06 INT_GND DE283ASF
Q_Q8      OUTA 06 INT_GND DE283ASF
Q_Q9      OUTA 06 INT_GND DE283ASF
M_M61     INT_VCC 17 16 INT_VCC MHS4XPEF L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
M_M62     16 EN 18 INT_GND MHS4XNEF L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
M_M63     18 D 06 INT_GND MHS4XNEF L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
M_M64     17 OUT INT_GND INT_GND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
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M_M65     INT_VCC OUT 17 INT_VCC MHS4XPEF L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M_M66     OUT EN 19 INT_GND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_M67     19 D INT_GND INT_GND MHS4XNEF L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
M_M68     03 D INT_GND INT_GND MHS4XNEF L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
M_M69     INT_VCC D 03 INT_VCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M70     08 D INT_GND INT_GND MHS4XNEF L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M_M71     INT_VCC D 08 INT_VCC MHS4XPEF L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
M_M72     05 D INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M73     INT_VCC D 05 INT_VCC MHS4XPEF L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
Q_Q14     INT_VCC 01 06 DA0ACBSF
Q_Q15     OUT INT_GND INT_GND ESDXXXXF
M_M74     04 EN INT_GND INT_GND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M75     INT_VCC EN 04 INT_VCC MHS4XPEF L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
.ENDS OUTBUF1F
* Philips Semiconductors - BCKLOAD
.SUBCKT BCKLOADF IN OUT INT_VCC INT_GND
X_D9      INT_GND IN INT_GND DB3002AF
X_D10     INT_GND IN INT_GND DB3002AF
X_D11     INT_GND IN INT_GND DB3002AF
X_D12     INT_GND IN INT_GND DB3002AF
X_D13     INT_GND IN INT_GND DB3002AF
M_M60     IN INT_GND INT_GND INT_GND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
X_D14     IN INT_VCC INT_GND DB0814AF
Q_Q10     IN INT_GND INT_GND DE283ASF
Q_Q11     IN INT_GND INT_GND DE283ASF
Q_Q12     IN INT_GND INT_GND DE283ASF
Q_Q13     IN INT_GND INT_GND DE283ASF
M_M61     INT_VCC OUT 01 01 MHS4XPEF L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M_M62     01 OUT INT_GND INT_GND MHS4XNEF L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
.ENDS BCKLOADF
* Philips Semiconductors - BUSHOLD1
.SUBCKT BUSHLD1F BH INT_GND INT_VCC
X_D1      01 02 INT_GND DB3002AF
Q_Q1      03 03 01 DE283ASF
X_R1      02 BH INT_GND DC00400F PARAMS: RES=2K
X_R2      BH 04 INT_GND DC00400F PARAMS: RES=5K
M_M4      04 05 INT_GND INT_GND MHS4XNEF L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
M_M1      05 BH INT_GND INT_GND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_M2      INT_VCC BH 05 05 MHS4XPEF L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
M_M3      INT_VCC 05 03 03 MHS4XPEF L=1.0U W=8.298U
+ AD=16.596P AS=16.596P PD=20.596U PS=20.596U NRD=0.241 NRS=0.241
.ENDS BUSHLD1F
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* Philips Semiconductors - ABT16244
.SUBCKT A16244F D EN OUT INT_VCC INT_GND
M_M1      01 26 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M2      03 04 02 INT_VCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M3      01 04 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M4      01 05 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M5      06 26 INT_GND INT_GND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M6      06 04 INT_GND INT_GND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M7      05 07 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M8      09 07 08 INT_GND MHS4XNEF L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
M_M9      08 07 06 INT_GND MHS4XNEF L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
M_M10     OUT 07 10 INT_GND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_M11     10 07 INT_GND INT_GND MHS4XNEF L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
M_M12     02 26 11 INT_VCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M13     12 05 03 INT_VCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M14     INT_VCC 07 05 INT_VCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
Q_Q1      INT_VCC 11 06 DA0ACBSF
Q_Q2      11 11 13 DA06CBSF
Q_Q3      OUT 06 INT_GND DE283ASF
Q_Q4      15 14 16 DE283ASF
X_Q5      15 17 14 INT_GND DB14CASF
M_M15     INT_VCC OEBAR 18 INT_VCC MHS4XPEF L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
M_M16     INT_VCC 18 04 INT_VCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M17     18 OEBAR INT_GND INT_GND MHS4XNEF L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
M_M18     04 18 INT_GND INT_GND MHS4XNEF L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
X_D1      13 OUT INT_GND DB0308AF
X_R7      06 INT_GND INT_GND DC00400F PARAMS: RES=1K
X_D2      OUT 09 INT_GND DB0814AF
X_D3      16 OUT INT_GND DB3002AF
X_R8      INT_VCC 15 INT_GND DB01E00F PARAMS: RES=15
M_M19     INT_VCC 04 19 INT_VCC MHS4XPEF L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
M_M20     19 26 07 INT_VCC MHS4XPEF L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
M_M21     07 04 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M22     07 26 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M23     21 18 20 INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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M_M24     20 26 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M25     INT_VCC 18 21 INT_VCC MHS4XPEF L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
M_M26     INT_VCC 26 21 INT_VCC MHS4XPEF L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
M_M43     INT_VCC 04 22 INT_VCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M44     22 21 17 INT_VCC MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M45     17 04 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M46     17 21 INT_GND INT_GND MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
M_M55     INT_VCC 04 23 INT_VCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M56     23 21 14 INT_VCC MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M57     14 04 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M58     14 21 INT_GND INT_GND MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
X_R9      INT_VCC 12 INT_GND DC00400F PARAMS: RES=10K
Q_Q6      15 14 16 DE283ASF
X_D5      16 OUT INT_GND DB3002AF
X_D6      16 OUT INT_GND DB3002AF
X_D7      16 OUT INT_GND DB3002AF
X_D8      16 OUT INT_GND DB3002AF
Q_Q7      OUT 06 INT_GND DE283ASF
Q_Q8      OUT 06 INT_GND DE283ASF
Q_Q9      OUT 06 INT_GND DE283ASF
Q_Q14     OEBAR INT_GND INT_GND ESDXXXXF
Q_Q15     26 INT_GND INT_GND ESDXXXXF
Q_Q16     OUT INT_GND INT_GND ESDXXXXF
M3_M1   INT_VCC D 25 INT_VCC MHS4XPEF L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3_M2   25 D INT_GND INT_GND MHS4XNEF L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3_M3   26 25 INT_GND INT_GND MHS4XNEF L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3_M4   INT_VCC 25 26 INT_VCC MHS4XPEF L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
X_D15     24 01 INT_GND DB0814AF
X_D16     11 24 INT_GND DB0814AF
R_R13     INT_GND D 10MEG
.ENDS A16244F
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* Philips Semiconductors - ABT16245
.SUBCKT A16245F D EN OUT INT_VCC INT_GND
M_M1      01 28 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M2      03 04 02 INT_VCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M3      01 04 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M4      01 05 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M5      06 28 INT_GND INT_GND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M6      06 04 INT_GND INT_GND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M7      05 07 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M8      08 07 09 INT_GND MHS4XNEF L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
M_M9      09 07 06 INT_GND MHS4XNEF L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
M_M10     OUT 07 10 INT_GND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_M11     10 07 INT_GND INT_GND MHS4XNEF L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
M_M12     02 28 11 INT_VCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M13     12 05 03 INT_VCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M14     INT_VCC 07 05 INT_VCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
Q_Q1      INT_VCC 11 06 DA0ACBSF
Q_Q2      11 11 13 DA06CBSF
Q_Q3      OUT 06 INT_GND DE283ASF
Q_Q4      15 14 16 DE283ASF
X_Q5      15 17 14 [INT_GND] DB14CASF
M_M15     INT_VCC OEBAR 18 INT_VCC MHS4XPEF L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
M_M16     INT_VCC 18 04 INT_VCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M17     18 OEBAR INT_GND INT_GND MHS4XNEF L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
M_M18     04 18 INT_GND INT_GND MHS4XNEF L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
X_D1      13 OUT INT_GND DB0308AF
X_R7      06 INT_GND INT_GND DC00400F PARAMS: RES=1K
X_D2      OUT 08 INT_GND DB0814AF
X_D3      16 OUT INT_GND DB3002AF
X_R8      INT_VCC 15 INT_GND DB01E00F PARAMS: RES=15
M_M19     INT_VCC 04 19 INT_VCC MHS4XPEF L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
M_M20     19 28 07 INT_VCC MHS4XPEF L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
M_M21     07 04 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M22     07 28 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M23     20 18 21 INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M24     21 28 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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M_M25     INT_VCC 18 20 INT_VCC MHS4XPEF L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
M_M26     INT_VCC 28 20 INT_VCC MHS4XPEF L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
M_M43     INT_VCC 04 22 INT_VCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M44     22 20 17 INT_VCC MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M45     17 04 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M46     17 20 INT_GND INT_GND MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
M_M55     INT_VCC 04 23 INT_VCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M56     23 20 14 INT_VCC MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M57     14 04 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M58     14 20 INT_GND INT_GND MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
X_R9      INT_VCC 12 INT_GND DC00400F PARAMS: RES=10K
Q_Q6      15 14 16 DE283ASF
X_D5      16 OUT INT_GND DB3002AF
X_D6      16 OUT INT_GND DB3002AF
X_D7      16 OUT INT_GND DB3002AF
X_D8      16 OUT INT_GND DB3002AF
Q_Q7      OUT 06 INT_GND DE283ASF
Q_Q8      OUT 06 INT_GND DE283ASF
Q_Q9      OUT 06 INT_GND DE283ASF
X_D9      INT_GND 28 INT_GND DB3002AF
X_D10     INT_GND 28 INT_GND DB3002AF
X_D11     INT_GND 28 INT_GND DB3002AF
X_D12     INT_GND 28 INT_GND DB3002AF
X_D13     INT_GND 28 INT_GND DB3002AF
M_M60     28 INT_GND INT_GND INT_GND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
X_D14     28 INT_VCC INT_GND DB0814AF
Q_Q10     24 INT_GND INT_GND DE283ASF
Q_Q11     24 INT_GND INT_GND DE283ASF
Q_Q12     24 INT_GND INT_GND DE283ASF
Q_Q13     24 INT_GND INT_GND DE283ASF
X_R11     28 24 INT_GND DB01E00F PARAMS: RES=22.5
Q_Q14     OEBAR INT_GND INT_GND ESDXXXXF
Q_Q15     28 INT_GND INT_GND ESDXXXXF
Q_Q16     OUT INT_GND INT_GND ESDXXXXF
M_M61     INT_VCC OUT 25 INT_VCC MHS4XPEF L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
M_M62     25 OUT INT_GND INT_GND MHS4XNEF L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
X_D15     11 26 INT_GND DB0814AF
X_D16     26 01 INT_GND DB0814AF
M_U3_M1   INT_VCC D 27 INT_VCC MHS4XPEF L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M_U3_M2   27 D INT_GND INT_GND MHS4XNEF L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M_U3_M3   28 27 INT_GND INT_GND MHS4XNEF L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M_U3_M4   INT_VCC 27 28 INT_VCC MHS4XPEF L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.ENDS A16245F
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* Philips Semiconductors - ABT162441F
.SUBCKT A162441F D EN OUT INT_VCC INT_GND
M_M1      01 26 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M2      03 04 02 INT_VCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M3      01 04 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M4      01 05 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M5      06 26 INT_GND INT_GND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M6      06 04 INT_GND INT_GND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M7      05 07 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M8      09 07 08 INT_GND MHS4XNEF L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
M_M9      08 07 06 INT_GND MHS4XNEF L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
M_M10     OUT 07 10 INT_GND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_M11     10 07 INT_GND INT_GND MHS4XNEF L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
M_M12     02 26 11 INT_VCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M13     12 05 03 INT_VCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M14     INT_VCC 07 05 INT_VCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
Q_Q1      INT_VCC 11 06 DA0ACBSF
Q_Q2      11 11 13 DA06CBSF
Q_Q3      OUTA 06 INT_GND DE283ASF
RR20      OUT OUTA 22.5
Q_Q4      15 14 16 DE283ASF
X_Q5      15 17 14 INT_GND DB14CASF
M_M15     INT_VCC OEBAR 18 INT_VCC MHS4XPEF L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
M_M16     INT_VCC 18 04 INT_VCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M17     18 OEBAR INT_GND INT_GND MHS4XNEF L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
M_M18     04 18 INT_GND INT_GND MHS4XNEF L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
X_D1      13 OUTA INT_GND DB0308AF
X_R7      06 INT_GND INT_GND DC00400F PARAMS: RES=1K
X_D2      OUT 09 INT_GND DB0814AF
X_D3      16 OUT INT_GND DB3002AF
X_R8      INT_VCC 15 INT_GND DB01E00F PARAMS: RES=15
M_M19     INT_VCC 04 19 INT_VCC MHS4XPEF L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
M_M20     19 26 07 INT_VCC MHS4XPEF L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
M_M21     07 04 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M22     07 26 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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M_M23     21 18 20 INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M24     20 26 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M25     INT_VCC 18 21 INT_VCC MHS4XPEF L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
M_M26     INT_VCC 26 21 INT_VCC MHS4XPEF L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
M_M43     INT_VCC 04 22 INT_VCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M44     22 21 17 INT_VCC MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M45     17 04 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M46     17 21 INT_GND INT_GND MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
M_M55     INT_VCC 04 23 INT_VCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M56     23 21 14 INT_VCC MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M57     14 04 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M58     14 21 INT_GND INT_GND MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
X_R9      INT_VCC 12 INT_GND DC00400F PARAMS: RES=10K
Q_Q6      15 14 16 DE283ASF
X_D5      16 OUT INT_GND DB3002AF
X_D6      16 OUT INT_GND DB3002AF
X_D7      16 OUT INT_GND DB3002AF
X_D8      16 OUT INT_GND DB3002AF
Q_Q7      OUTA 06 INT_GND DE283ASF
Q_Q8      OUTA 06 INT_GND DE283ASF
Q_Q9      OUTA 06 INT_GND DE283ASF
Q_Q14     OEBAR INT_GND INT_GND ESDXXXXF
Q_Q15     26 INT_GND INT_GND ESDXXXXF
Q_Q16     OUT INT_GND INT_GND ESDXXXXF
M3_M1   INT_VCC D 25 INT_VCC MHS4XPEF L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3_M2   25 D INT_GND INT_GND MHS4XNEF L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3_M3   26 25 INT_GND INT_GND MHS4XNEF L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3_M4   INT_VCC 25 26 INT_VCC MHS4XPEF L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
X_D15     24 01 INT_GND DB0814AF
X_D16     11 24 INT_GND DB0814AF
R_R13     INT_GND D 10MEG
.ENDS A162441F
```

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* Philips Semiconductors - ABT162451F
.SUBCKT A162451F D EN OUT INT_VCC INT_GND
M_M1      01 28 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M2      03 04 02 INT_VCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M3      01 04 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M4      01 05 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M5      06 28 INT_GND INT_GND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M6      06 04 INT_GND INT_GND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M7      05 07 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M8      08 07 09 INT_GND MHS4XNEF L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
M_M9      09 07 06 INT_GND MHS4XNEF L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
M_M10     OUT 07 10 INT_GND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_M11     10 07 INT_GND INT_GND MHS4XNEF L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
M_M12     02 28 11 INT_VCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M13     12 05 03 INT_VCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M14     INT_VCC 07 05 INT_VCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
Q_Q1      INT_VCC 11 06 DA0ACBSF
Q_Q2      11 11 13 DA06CBSF
Q_Q3      OUTA 06 INT_GND DE283ASF
RR20      OUT OUTA 22.5
Q_Q4      15 14 16 DE283ASF
X_Q5      15 17 14 [INT_GND] DB14CASF
M_M15     INT_VCC OEBAR 18 INT_VCC MHS4XPEF L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
M_M16     INT_VCC 18 04 INT_VCC MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M17     18 OEBAR INT_GND INT_GND MHS4XNEF L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
M_M18     04 18 INT_GND INT_GND MHS4XNEF L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
X_D1      13 OUTA INT_GND DB0308AF
X_R7      06 INT_GND INT_GND DC00400F PARAMS: RES=1K
X_D2      OUT 08 INT_GND DB0814AF
X_D3      16 OUT INT_GND DB3002AF
X_R8      INT_VCC 15 INT_GND DB01E00F PARAMS: RES=15
M_M19     INT_VCC 04 19 INT_VCC MHS4XPEF L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
M_M20     19 28 07 INT_VCC MHS4XPEF L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
M_M21     07 04 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M22     07 28 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M23     20 18 21 INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M24     21 28 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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M_M25     INT_VCC 18 20 INT_VCC MHS4XPEF L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
M_M26     INT_VCC 28 20 INT_VCC MHS4XPEF L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
M_M43     INT_VCC 04 22 INT_VCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M44     22 20 17 INT_VCC MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M45     17 04 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M46     17 20 INT_GND INT_GND MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
M_M55     INT_VCC 04 23 INT_VCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M56     23 20 14 INT_VCC MHS4XPEF L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M57     14 04 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M58     14 20 INT_GND INT_GND MHS4XNEF L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
X_R9      INT_VCC 12 INT_GND DC00400F PARAMS: RES=10K
Q_Q6      15 14 16 DE283ASF
X_D5      16 OUT INT_GND DB3002AF
X_D6      16 OUT INT_GND DB3002AF
X_D7      16 OUT INT_GND DB3002AF
X_D8      16 OUT INT_GND DB3002AF
Q_Q7      OUTA 06 INT_GND DE283ASF
Q_Q8      OUTA 06 INT_GND DE283ASF
Q_Q9      OUTA 06 INT_GND DE283ASF
X_D9      INT_GND 28 INT_GND DB3002AF
X_D10     INT_GND 28 INT_GND DB3002AF
X_D11     INT_GND 28 INT_GND DB3002AF
X_D12     INT_GND 28 INT_GND DB3002AF
X_D13     INT_GND 28 INT_GND DB3002AF
M_M60     28 INT_GND INT_GND INT_GND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
X_D14     28 INT_VCC INT_GND DB0814AF
Q_Q10     24 INT_GND INT_GND DE283ASF
Q_Q11     24 INT_GND INT_GND DE283ASF
Q_Q12     24 INT_GND INT_GND DE283ASF
Q_Q13     24 INT_GND INT_GND DE283ASF
X_R11     28 24 INT_GND DB01E00F PARAMS: RES=22.5
Q_Q14     OEBAR INT_GND INT_GND ESDXXXXF
Q_Q15     28 INT_GND INT_GND ESDXXXXF
Q_Q16     OUT INT_GND INT_GND ESDXXXXF
M_M61     INT_VCC OUT 25 INT_VCC MHS4XPEF L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
M_M62     25 OUT INT_GND INT_GND MHS4XNEF L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
X_D15     11 26 INT_GND DB0814AF
X_D16     26 01 INT_GND DB0814AF
M_U3_M1   INT_VCC D 27 INT_VCC MHS4XPEF L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M_U3_M2   27 D INT_GND INT_GND MHS4XNEF L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M_U3_M3   28 27 INT_GND INT_GND MHS4XNEF L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M_U3_M4   INT_VCC 27 28 INT_VCC MHS4XPEF L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.ENDS A162451F
```

A16SLOPS.LIB Subcircuit

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*****************************************************************************
* ABT16 PSPICE SUBCIRCUIT LIBRARY
* A16SLOPS.LIB
* SLOW PROCESS CORNER
* STANDARD LOGIC PRODUCT GROUP
* PHILIPS SEMICONDUCTORS
* 3/31/1995
*****************************************************************************
.SUBCKT INV1 D E Q VCC
* USE THIS MODEL FOR ABT16240 (INVERTING PART)
*    IN   OUT   INT_VCC   INT_GND    (ENABLE)
X1   3     90     99        6           INBUFFS
*    IN   OUT   INT_VCC   INT_GND    (SIGNAL)
X2   1     91     99        6           MOSINVS
*    D     EN    OUT    INT_VCC   INT_GND
X3   91    90     2       99        6      OUTBUFFS
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1
*
.SUBCKT INV1_1 D E Q VCC
* USE THIS MODEL FOR ABT16240-1 (INVERTING PART)
*    IN   OUT   INT_VCC   INT_GND    (ENABLE)
X1   3     90     99        6           INBUFFS
*    IN   OUT   INT_VCC   INT_GND    (SIGNAL)
X2   1     91     99        6           MOSINVS
*    D     EN    OUT    INT_VCC   INT_GND
X3   91    90     2       99        6      OUTBUF1F
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1_1
.SUBCKT INV2 D E Q VCC
*
*    IN   OUT   INT_VCC   INT_GND    (ENABLE)
X1   3     90     99        6           INBUFFS
*    IN   OUT   INT_VCC   INT_GND    (SIGNAL)
X2   1     91     99        6           MOSINVS
*    D     EN    OUT    INT_VCC   INT_GND
X3   91    90     2       99        6      OUTBUFFS
*    IN   OUT   INT_VCC   INT_GND
X4    2    1      99        6           BCKLOADS
```

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*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV2
.SUBCKT NINV D E Q VCC
* USE THIS MODEL FOR ABT16273  -373B  -374B  -541
*  -821  -823  -825  -827  -841  (NON-INVERTING)
*   IN  OUT  INT_VCC  INT_GND  (ENABLE)
X1  3    90    99       6         INBUFFS
*   IN  OUT  INT_VCC  INT_GND  (SIGNAL)
X2  1    91    99       6         INBUFFS
*   D    EN   OUT   INT_VCC  INT_GND
X3  91   90    2      99       6     OUTBUFFS
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINV
*
.SUBCKT NINVB D E Q VCC
* USE THIS MODEL FOR ABT16500  -501  -543  -646  -652  -899
* -952  -1543
*   IN  OUT  INT_VCC  INT_GND  (ENABLE)
X1  3    90    99       6         INBUFFS
*   IN  OUT  INT_VCC  INT_GND  (SIGNAL)
X2  1    91    99       6         INBUFFS
*   D    EN   OUT   INT_VCC  INT_GND
X3  91   90    2      99       6     OUTBUFFS
*   IN  OUT  INT_VCC  INT_GND
X4   2    1     99       6         BCKLOADS
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINVB
*
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```
.SUBCKT A16244 D E Q VCC
* USE THIS MODEL FOR ABT16244A
*    D     EN    OUT    INT_VCC   INT_GND
X3   1      3     2        99       6      A16244S
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16244
*
.SUBCKT A16245 D E Q VCC
* USE THIS MODEL FOR ABT16245B
*    D     EN    OUT    INT_VCC   INT_GND
X3   1      3     2        99       6      A16245S
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16245
.SUBCKT A16244_1 D E Q VCC
* USE THIS MODEL FOR ABT16244-1
*    D     EN    OUT    INT_VCC   INT_GND
X3   1      3     2        99       6      A162441S
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16244_1
*
```

```
.SUBCKT A16245_1 D E Q VCC
* USE THIS MODEL FOR ABT16245A-1
*   D     EN    OUT    INT_VCC   INT_GND
X3  1      3     2       99        6      A162451S
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A16245_1
*
* Philips Semiconductors - MOSINV
.SUBCKT MOSINVS IN OUT INT_VCC INT_GND
M_M1      INT_VCC IN 01 INT_VCC MHS4XPES L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M_M2      01 IN INT_GND INT_GND MHS4XNES L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M_M3      OUT 01 INT_GND INT_GND MHS4XNES L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M_M4      INT_VCC 01 OUT INT_VCC MHS4XPES L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.ENDS MOSINVS
* Philips Semiconductors - INBUFF
.SUBCKT INBUFFS   IN OUT INT_VCC INT_GND
M_M1      OUT IN INT_GND INT_GND MHS4XNES L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M_M2      INT_VCC IN 01 01 MHS4XPES L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
Q_Q1      IN INT_GND INT_GND ESDXXXXS
R_R1      01 OUT 100
.ENDS INBUFFS
* Philips Semiconductors - OUTBUFF
.SUBCKT OUTBUFFS D EN OUT INT_VCC INT_GND
M_M2      02 03 01 INT_VCC MHS4XPES L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
M_M3      01 04 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M4      01 05 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M5      06 05 INT_GND INT_GND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M6      06 04 INT_GND INT_GND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M13     07 04 02 INT_VCC MHS4XPES L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
Q_Q1      INT_VCC 08 05 DA04CASS
Q_Q2      01 01 09 DA0ACBSS
Q_Q3      OUT 06 INT_GND DE283ASS
Q_Q4      11 10 12 DE283ASS
X_Q5      11 13 10 [INT_GND] DB14CASS
X_D1      09 OUT INT_GND DB0814AS
X_R7      06 INT_GND INT_GND DC00400S PARAMS: RES=1K
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X_D3      12 OUT INT_GND DB3002AS
X_R8      INT_VCC 11 INT_GND DB01E00S PARAMS: RES=15
M_M43     INT_VCC 04 14 INT_VCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M44     14 D 13 INT_VCC MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M45     13 04 INT_GND INT_GND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_M46     13 D INT_GND INT_GND MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
M_M55     INT_VCC 04 15 INT_VCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M56     15 D 10 INT_VCC MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M57     10 04 INT_GND INT_GND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_M58     10 D INT_GND INT_GND MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
X_R9      INT_VCC 07 INT_GND DC00400S PARAMS: RES=10K
Q_Q6      11 10 12 DE283ASS
X_D5      12 OUT INT_GND DB3002AS
X_D6      12 OUT INT_GND DB3002AS
X_D7      12 OUT INT_GND DB3002AS
X_D8      12 OUT INT_GND DB3002AS
Q_Q7      OUT 06 INT_GND DE283ASS
Q_Q8      OUT 06 INT_GND DE283ASS
Q_Q9      OUT 06 INT_GND DE283ASS
M_M61     INT_VCC 17 16 INT_VCC MHS4XPES L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
M_M62     16 EN 18 INT_GND MHS4XNES L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
M_M63     18 D 06 INT_GND MHS4XNES L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
M_M64     17 OUT INT_GND INT_GND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_M65     INT_VCC OUT 17 INT_VCC MHS4XPES L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M_M66     OUT EN 19 INT_GND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_M67     19 D INT_GND INT_GND MHS4XNES L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
M_M68     03 D INT_GND INT_GND MHS4XNES L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
M_M69     INT_VCC D 03 INT_VCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M70     08 D INT_GND INT_GND MHS4XNES L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M_M71     INT_VCC D 08 INT_VCC MHS4XPES L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
M_M72     05 D INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M73     INT_VCC D 05 INT_VCC MHS4XPES L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
Q_Q14     INT_VCC 01 06 DA0ACBSS
Q_Q15     OUT INT_GND INT_GND ESDXXXXS
M_M74     04 EN INT_GND INT_GND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M75     INT_VCC EN 04 INT_VCC MHS4XPES L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
.ENDS OUTBUFFS
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* Philips Semiconductors - OUTBUF1S
.SUBCKT OUTBUF1S D EN OUT INT_VCC INT_GND
M_M2      02 03 01 INT_VCC MHS4XPES L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
M_M3      01 04 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M4      01 05 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M5      06 05 INT_GND INT_GND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M6      06 04 INT_GND INT_GND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M13     07 04 02 INT_VCC MHS4XPES L=1.0U W=34.298U
+ AD=68.596P AS=68.596P PD=72.596U PS=72.596U NRD=0.058 NRS=0.058
Q_Q1      INT_VCC 08 05 DA04CASS
Q_Q2      01 01 09 DA0ACBSS
Q_Q3      OUTA 06 INT_GND DE283ASS
RR20      OUT OUTA 22.5
Q_Q4      11 10 12 DE283ASS
X_Q5      11 13 10 [INT_GND] DB14CASS
X_D1      09 OUTA INT_GND DB0814AS
X_R7      06 INT_GND INT_GND DC00400S PARAMS: RES=1K
X_D3      12 OUT INT_GND DB3002AS
X_R8      INT_VCC 11 INT_GND DB01E00S PARAMS: RES=15
M_M43     INT_VCC 04 14 INT_VCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M44     14 D 13 INT_VCC MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M45     13 04 INT_GND INT_GND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_M46     13 D INT_GND INT_GND MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
M_M55     INT_VCC 04 15 INT_VCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M56     15 D 10 INT_VCC MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M57     10 04 INT_GND INT_GND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_M58     10 D INT_GND INT_GND MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
X_R9      INT_VCC 07 INT_GND DC00400S PARAMS: RES=10K
Q_Q6      11 10 12 DE283ASS
X_D5      12 OUT INT_GND DB3002AS
X_D6      12 OUT INT_GND DB3002AS
X_D7      12 OUT INT_GND DB3002AS
X_D8      12 OUT INT_GND DB3002AS
Q_Q7      OUTA 06 INT_GND DE283ASS
Q_Q8      OUTA 06 INT_GND DE283ASS
Q_Q9      OUTA 06 INT_GND DE283ASS
M_M61     INT_VCC 17 16 INT_VCC MHS4XPES L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
M_M62     16 EN 18 INT_GND MHS4XNES L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
M_M63     18 D 06 INT_GND MHS4XNES L=1.0U W=99.926U
+ AD=199.852P AS=199.852P PD=203.852U PS=203.852U NRD=0.020 NRS=0.020
M_M64     17 OUT INT_GND INT_GND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_M65     INT_VCC OUT 17 INT_VCC MHS4XPES L=1.0U W=29.298U
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+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M_M66     OUT EN 19 INT_GND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_M67     19 D INT_GND INT_GND MHS4XNES L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
M_M68     03 D INT_GND INT_GND MHS4XNES L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
M_M69     INT_VCC D 03 INT_VCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M70     08 D INT_GND INT_GND MHS4XNES L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M_M71     INT_VCC D 08 INT_VCC MHS4XPES L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
M_M72     05 D INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M73     INT_VCC D 05 INT_VCC MHS4XPES L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
Q_Q14     INT_VCC 01 06 DA0ACBSS
Q_Q15     OUT INT_GND INT_GND ESDXXXXS
M_M74     04 EN INT_GND INT_GND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M75     INT_VCC EN 04 INT_VCC MHS4XPES L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
.ENDS OUTBUF1S
* Philips Semiconductors - BCKLOAD
.SUBCKT BCKLOADS IN OUT INT_VCC INT_GND
X_D9      INT_GND IN INT_GND DB3002AS
X_D10     INT_GND IN INT_GND DB3002AS
X_D11     INT_GND IN INT_GND DB3002AS
X_D12     INT_GND IN INT_GND DB3002AS
X_D13     INT_GND IN INT_GND DB3002AS
M_M60     IN INT_GND INT_GND INT_GND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
X_D14     IN INT_VCC INT_GND DB0814AS
Q_Q10     IN INT_GND INT_GND DE283ASS
Q_Q11     IN INT_GND INT_GND DE283ASS
Q_Q12     IN INT_GND INT_GND DE283ASS
Q_Q13     IN INT_GND INT_GND DE283ASS
M_M61     INT_VCC OUT 01 01 MHS4XPES L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M_M62     01 OUT INT_GND INT_GND MHS4XNES L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
.ENDS BCKLOADS
* Philips Semiconductors - BUSHOLD1
.SUBCKT BUSHLD1S BH INT_GND INT_VCC
X_D1      01 02 INT_GND DB3002AS
Q_Q1      03 03 01 DE283ASS
X_R1      02 BH INT_GND DC00400S PARAMS: RES=2K
X_R2      BH 04 INT_GND DC00400S PARAMS: RES=5K
M_M4      04 05 INT_GND INT_GND MHS4XNES L=1.0U W=2.926U
+ AD=5.852P AS=5.852P PD=9.852U PS=9.852U NRD=0.684 NRS=0.684
M_M1      05 BH INT_GND INT_GND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_M2      INT_VCC BH 05 05 MHS4XPES L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
M_M3      INT_VCC 05 03 03 MHS4XPES L=1.0U W=8.298U
+ AD=16.596P AS=16.596P PD=20.596U PS=20.596U NRD=0.241 NRS=0.241
.ENDS BUSHLD1S
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* Philips Semiconductors - ABT16244
.SUBCKT A16244S D EN OUT INT_VCC INT_GND
M_M1      01 26 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M2      03 04 02 INT_VCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M3      01 04 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M4      01 05 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M5      06 26 INT_GND INT_GND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M6      06 04 INT_GND INT_GND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M7      05 07 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M8      09 07 08 INT_GND MHS4XNES L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
M_M9      08 07 06 INT_GND MHS4XNES L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
M_M10     OUT 07 10 INT_GND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_M11     10 07 INT_GND INT_GND MHS4XNES L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
M_M12     02 26 11 INT_VCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M13     12 05 03 INT_VCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M14     INT_VCC 07 05 INT_VCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
Q_Q1      INT_VCC 11 06 DA0ACBSS
Q_Q2      11 11 13 DA06CBSS
Q_Q3      OUT 06 INT_GND DE283ASS
Q_Q4      15 14 16 DE283ASS
X_Q5      15 17 14 INT_GND DB14CASS
M_M15     INT_VCC OEBAR 18 INT_VCC MHS4XPES L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
M_M16     INT_VCC 18 04 INT_VCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M17     18 OEBAR INT_GND INT_GND MHS4XNES L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
M_M18     04 18 INT_GND INT_GND MHS4XNES L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
X_D1      13 OUT INT_GND DB0308AS
X_R7      06 INT_GND INT_GND DC00400S PARAMS: RES=1K
X_D2      OUT 09 INT_GND DB0814AS
X_D3      16 OUT INT_GND DB3002AS
X_R8      INT_VCC 15 INT_GND DB01E00S PARAMS: RES=15
M_M19     INT_VCC 04 19 INT_VCC MHS4XPES L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
M_M20     19 26 07 INT_VCC MHS4XPES L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
M_M21     07 04 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M22     07 26 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M23     21 18 20 INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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M_M24     20 26 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M25     INT_VCC 18 21 INT_VCC MHS4XPES L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
M_M26     INT_VCC 26 21 INT_VCC MHS4XPES L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
M_M43     INT_VCC 04 22 INT_VCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M44     22 21 17 INT_VCC MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M45     17 04 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M46     17 21 INT_GND INT_GND MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
M_M55     INT_VCC 04 23 INT_VCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M56     23 21 14 INT_VCC MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M57     14 04 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M58     14 21 INT_GND INT_GND MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
X_R9      INT_VCC 12 INT_GND DC00400S PARAMS: RES=10K
Q_Q6      15 14 16 DE283ASS
X_D5      16 OUT INT_GND DB3002AS
X_D6      16 OUT INT_GND DB3002AS
X_D7      16 OUT INT_GND DB3002AS
X_D8      16 OUT INT_GND DB3002AS
Q_Q7      OUT 06 INT_GND DE283ASS
Q_Q8      OUT 06 INT_GND DE283ASS
Q_Q9      OUT 06 INT_GND DE283ASS
Q_Q14     OEBAR INT_GND INT_GND ESDXXXXS
Q_Q15     26 INT_GND INT_GND ESDXXXXS
Q_Q16     OUT INT_GND INT_GND ESDXXXXS
M3_M1   INT_VCC D 25 INT_VCC MHS4XPES L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3_M2   25 D INT_GND INT_GND MHS4XNES L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3_M3   26 25 INT_GND INT_GND MHS4XNES L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3_M4   INT_VCC 25 26 INT_VCC MHS4XPES L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
X_D15     24 01 INT_GND DB0814AS
X_D16     11 24 INT_GND DB0814AS
R_R13     INT_GND D 10MEG
.ENDS A16244S
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* Philips Semiconductors - ABT16245
.SUBCKT A16245S D EN OUT INT_VCC INT_GND
M_M1      01 28 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M2      03 04 02 INT_VCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M3      01 04 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M4      01 05 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M5      06 28 INT_GND INT_GND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M6      06 04 INT_GND INT_GND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M7      05 07 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M8      08 07 09 INT_GND MHS4XNES L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
M_M9      09 07 06 INT_GND MHS4XNES L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
M_M10     OUT 07 10 INT_GND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_M11     10 07 INT_GND INT_GND MHS4XNES L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
M_M12     02 28 11 INT_VCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M13     12 05 03 INT_VCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M14     INT_VCC 07 05 INT_VCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
Q_Q1      INT_VCC 11 06 DA0ACBSS
Q_Q2      11 11 13 DA06CBSS
Q_Q3      OUT 06 INT_GND DE283ASS
Q_Q4      15 14 16 DE283ASS
X_Q5      15 17 14 [INT_GND] DB14CASS
M_M15     INT_VCC OEBAR 18 INT_VCC MHS4XPES L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
M_M16     INT_VCC 18 04 INT_VCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M17     18 OEBAR INT_GND INT_GND MHS4XNES L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
M_M18     04 18 INT_GND INT_GND MHS4XNES L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
X_D1      13 OUT INT GND DB0308AS
X_R7      06 INT_GND INT_GND DC00400S PARAMS: RES=1K
X_D2      OUT 08 INT_GND DB0814AS
X_D3      16 OUT INT_GND DB3002AS
X_R8      INT_VCC 15 INT_GND DB01E00S PARAMS: RES=15
M_M19     INT_VCC 04 19 INT_VCC MHS4XPES L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
M_M20     19 28 07 INT_VCC MHS4XPES L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
M_M21     07 04 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M22     07 28 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M23     20 18 21 INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M24     21 28 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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M_M25     INT_VCC 18 20 INT_VCC MHS4XPES L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
M_M26     INT_VCC 28 20 INT_VCC MHS4XPES L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
M_M43     INT_VCC 04 22 INT_VCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M44     22 20 17 INT_VCC MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M45     17 04 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M46     17 20 INT_GND INT_GND MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
M_M55     INT_VCC 04 23 INT_VCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M56     23 20 14 INT_VCC MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M57     14 04 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M58     14 20 INT_GND INT_GND MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
X_R9      INT_VCC 12 INT_GND DC00400S PARAMS: RES=10K
Q_Q6      15 14 16 DE283ASS
X_D5      16 OUT INT_GND DB3002AS
X_D6      16 OUT INT_GND DB3002AS
X_D7      16 OUT INT_GND DB3002AS
X_D8      16 OUT INT_GND DB3002AS
Q_Q7      OUT 06 INT_GND DE283ASS
Q_Q8      OUT 06 INT_GND DE283ASS
Q_Q9      OUT 06 INT_GND DE283ASS
X_D9      INT_GND 28 INT_GND DB3002AS
X_D10     INT_GND 28 INT_GND DB3002AS
X_D11     INT_GND 28 INT_GND DB3002AS
X_D12     INT_GND 28 INT_GND DB3002AS
X_D13     INT_GND 28 INT_GND DB3002AS
M_M60     28 INT_GND INT_GND INT_GND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
X_D14     28 INT_VCC INT_GND DB0814AS
Q_Q10     24 INT_GND INT_GND DE283ASS
Q_Q11     24 INT_GND INT_GND DE283ASS
Q_Q12     24 INT_GND INT_GND DE283ASS
Q_Q13     24 INT_GND INT_GND DE283ASS
X_R11     28 24 INT_GND DB01E00S PARAMS: RES=22.5
Q_Q14     OEBAR INT_GND INT_GND ESDXXXXS
Q_Q15     28 INT_GND INT_GND ESDXXXXS
Q_Q16     OUT INT_GND INT_GND ESDXXXXS
M_M61     INT_VCC OUT 25 INT_VCC MHS4XPES L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
M_M62     25 OUT INT_GND INT_GND MHS4XNES L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
X_D15     11 26 INT_GND DB0814AS
X_D16     26 01 INT_GND DB0814AS
M_U3_M1   INT_VCC D 27 INT_VCC MHS4XPES L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M_U3_M2   27 D INT_GND INT_GND MHS4XNES L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M_U3_M3   28 27 INT_GND INT_GND MHS4XNES L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M_U3_M4   INT_VCC 27 28 INT_VCC MHS4XPES L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.ENDS A16245S
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* Philips Semiconductors - ABT162441S
.SUBCKT A162441S D EN OUT INT_VCC INT_GND
M_M1      01 26 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M2      03 04 02 INT_VCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M3      01 04 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M4      01 05 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M5      06 26 INT_GND INT_GND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M6      06 04 INT_GND INT_GND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M7      05 07 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M8      09 07 08 INT_GND MHS4XNES L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
M_M9      08 07 06 INT_GND MHS4XNES L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
M_M10     OUT 07 10 INT_GND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_M11     10 07 INT_GND INT_GND MHS4XNES L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
M_M12     02 26 11 INT_VCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M13     12 05 03 INT_VCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M14     INT_VCC 07 05 INT_VCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
Q_Q1      INT_VCC 11 06 DA0ACBSS
Q_Q2      11 11 13 DA06CBSS
Q_Q3      OUTA 06 INT_GND DE283ASS
RR20      OUT OUTA 22.5
Q_Q4      15 14 16 DE283ASS
X_Q5      15 17 14 INT_GND DB14CASS
M_M15     INT_VCC OEBAR 18 INT_VCC MHS4XPES L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
M_M16     INT_VCC 18 04 INT_VCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M17     18 OEBAR INT_GND INT_GND MHS4XNES L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
M M18     04 18 INT GND INT_GND MHS4XNES L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
X_D1      13 OUTA INT_GND DB0308AS
X_R7      06 INT_GND INT_GND DC00400S PARAMS: RES=1K
X_D2      OUT 09 INT_GND DB0814AS
X_D3      16 OUT INT_GND DB3002AS
X_R8      INT_VCC 15 INT_GND DB01E00S PARAMS: RES=15
M_M19     INT_VCC 04 19 INT_VCC MHS4XPES L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
M_M20     19 26 07 INT_VCC MHS4XPES L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
M_M21     07 04 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M22     07 26 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
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M_M23     21 18 20 INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M24     20 26 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M25     INT_VCC 18 21 INT_VCC MHS4XPES L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
M_M26     INT_VCC 26 21 INT_VCC MHS4XPES L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
M_M43     INT_VCC 04 22 INT_VCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M44     22 21 17 INT_VCC MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M45     17 04 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M46     17 21 INT_GND INT_GND MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
M_M55     INT_VCC 04 23 INT_VCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M56     23 21 14 INT_VCC MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M57     14 04 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M58     14 21 INT_GND INT_GND MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
X_R9      INT_VCC 12 INT_GND DC00400S PARAMS: RES=10K
Q_Q6      15 14 16 DE283ASS
X_D5      16 OUT INT_GND DB3002AS
X_D6      16 OUT INT_GND DB3002AS
X_D7      16 OUT INT_GND DB3002AS
X_D8      16 OUT INT_GND DB3002AS
Q_Q7      OUTA 06 INT_GND DE283ASS
Q_Q8      OUTA 06 INT_GND DE283ASS
Q_Q9      OUTA 06 INT_GND DE283ASS
Q_Q14     OEBAR INT_GND INT_GND ESDXXXXS
Q_Q15     26 INT_GND INT_GND ESDXXXXS
Q_Q16     OUT INT_GND INT_GND ESDXXXXS
M3_M1   INT_VCC D 25 INT_VCC MHS4XPES L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M3_M2   25 D INT_GND INT_GND MHS4XNES L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M3_M3   26 25 INT_GND INT_GND MHS4XNES L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M3_M4   INT_VCC 25 26 INT_VCC MHS4XPES L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
X_D15     24 01 INT_GND DB0814AS
X_D16     11 24 INT_GND DB0814AS
R_R13     INT_GND D 10MEG
.ENDS A162441S
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* Philips Semiconductors - ABT162451S
.SUBCKT A162451S D EN OUT INT_VCC INT_GND
M_M1      01 28 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M2      03 04 02 INT_VCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M3      01 04 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M4      01 05 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M5      06 28 INT_GND INT_GND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M6      06 04 INT_GND INT_GND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_M7      05 07 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M8      08 07 09 INT_GND MHS4XNES L=1.0U W=110.926U
+ AD=221.852P AS=221.852P PD=225.852U PS=225.852U NRD=0.018 NRS=0.018
M_M9      09 07 06 INT_GND MHS4XNES L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
M_M10     OUT 07 10 INT_GND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_M11     10 07 INT_GND INT_GND MHS4XNES L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
M_M12     02 28 11 INT_VCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M13     12 05 03 INT_VCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M14     INT_VCC 07 05 INT_VCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
Q_Q1      INT_VCC 11 06 DA0ACBSS
Q_Q2      11 11 13 DA06CBSS
Q_Q3      OUTA 06 INT_GND DE283ASS
RR20      OUT OUTA 22.5
Q_Q4      15 14 16 DE283ASS
X_Q5      15 17 14 [INT_GND] DB14CASS
M_M15     INT_VCC OEBAR 18 INT_VCC MHS4XPES L=1.0U W=14.298U
+ AD=28.596P AS=28.596P PD=32.596U PS=32.596U NRD=0.140 NRS=0.140
M_M16     INT_VCC 18 04 INT_VCC MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_M17     18 OEBAR INT_GND INT_GND MHS4XNES L=1.0U W=77.926U
+ AD=155.852P AS=155.852P PD=159.852U PS=159.852U NRD=0.026 NRS=0.026
M_M18     04 18 INT_GND INT_GND MHS4XNES L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
X_D1      13 OUTA INT_GND DB0308AS
X_R7      06 INT_GND INT_GND DC00400S PARAMS: RES=1K
X_D2      OUT 08 INT_GND DB0814AS
X_D3      16 OUT INT_GND DB3002AS
X_R8      INT_VCC 15 INT_GND DB01E00S PARAMS: RES=15
M_M19     INT_VCC 04 19 INT_VCC MHS4XPES L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
M_M20     19 28 07 INT_VCC MHS4XPES L=1.0U W=12.298U
+ AD=24.596P AS=24.596P PD=28.596U PS=28.596U NRD=0.163 NRS=0.163
M_M21     07 04 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M22     07 28 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M23     20 18 21 INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M24     21 28 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
```

```
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M25     INT_VCC 18 20 INT_VCC MHS4XPES L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
M_M26     INT_VCC 28 20 INT_VCC MHS4XPES L=1.0U W=6.298U
+ AD=12.596P AS=12.596P PD=16.596U PS=16.596U NRD=0.318 NRS=0.318
M_M43     INT_VCC 04 22 INT_VCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M44     22 20 17 INT_VCC MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M45     17 04 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M46     17 20 INT_GND INT_GND MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
M_M55     INT_VCC 04 23 INT_VCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_M56     23 20 14 INT_VCC MHS4XPES L=1.0U W=9.298U
+ AD=18.596P AS=18.596P PD=22.596U PS=22.596U NRD=0.215 NRS=0.215
M_M57     14 04 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
M_M58     14 20 INT_GND INT_GND MHS4XNES L=1.0U W=14.926U
+ AD=29.852P AS=29.852P PD=33.852U PS=33.852U NRD=0.134 NRS=0.134
X_R9      INT_VCC 12 INT_GND DC00400S PARAMS: RES=10K
Q_Q6      15 14 16 DE283ASS
X_D5      16 OUT INT_GND DB3002AS
X_D6      16 OUT INT_GND DB3002AS
X_D7      16 OUT INT_GND DB3002AS
X_D8      16 OUT INT_GND DB3002AS
Q_Q7      OUTA 06 INT_GND DE283ASS
Q_Q8      OUTA 06 INT_GND DE283ASS
Q_Q9      OUTA 06 INT_GND DE283ASS
X_D9      INT_GND 28 INT_GND DB3002AS
X_D10     INT_GND 28 INT_GND DB3002AS
X_D11     INT_GND 28 INT_GND DB3002AS
X_D12     INT_GND 28 INT_GND DB3002AS
X_D13     INT_GND 28 INT_GND DB3002AS
M_M60     28 INT_GND INT_GND INT_GND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
X_D14     28 INT_VCC INT_GND DB0814AS
Q_Q10     24 INT_GND INT_GND DE283ASS
Q_Q11     24 INT_GND INT_GND DE283ASS
Q_Q12     24 INT_GND INT_GND DE283ASS
Q_Q13     24 INT_GND INT_GND DE283ASS
X_R11     28 24 INT_GND DB01E00S PARAMS: RES=22.5
Q_Q14     OEBAR INT_GND INT_GND ESDXXXXS
Q_Q15     28 INT_GND INT_GND ESDXXXXS
Q_Q16     OUT INT_GND INT_GND ESDXXXXS
M_M61     INT_VCC OUT 25 INT_VCC MHS4XPES L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
M_M62     25 OUT INT_GND INT_GND MHS4XNES L=1.0U W=89.926U
+ AD=179.852P AS=179.852P PD=183.852U PS=183.852U NRD=0.022 NRS=0.022
X_D15     11 26 INT_GND DB0814AS
X_D16     26 01 INT_GND DB0814AS
M_U3_M1   INT_VCC D 27 INT_VCC MHS4XPES L=1.0U W=299.298U
+ AD=598.596P AS=598.596P PD=602.596U PS=602.596U NRD=0.007 NRS=0.007
M_U3_M2   27 D INT_GND INT_GND MHS4XNES L=1.0U W=199.926U
+ AD=399.852P AS=399.852P PD=403.852U PS=403.852U NRD=0.010 NRS=0.010
M_U3_M3   28 27 INT_GND INT_GND MHS4XNES L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M_U3_M4   INT_VCC 27 28 INT_VCC MHS4XPES L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
.ENDS A162451S
```

Section 4
LVT

SPICE

CONTENTS

Each LVT device requires some combination of an input stage, an output stage, one or two inverting stages, and some package parasitics. Table 3-1 shows LVT model combinations that correlate input, inverting, and output structures for each part type.

Table 4-1. LVT Model Combinations

LVT	Input Circuit	Inverter Circuit	Output Circuit	Inverting Output	Subcircuit Name
125	IN_D	INVB	OUTCKT	No	INV1
240	IN_D	INVB/INVB	OUTCKT	Yes	NINV
244A	IN_D	INVB	OUTCKT	No	INV1
245	IN_D	INVD	OUTCKT	No	A2BINV1
273	IN_D	INVA	OUTCKT	No	INV2
543	IN_D	INVC	OUTCKT	No	A2BINV2
573	IN_D	INVA	OUTCKT	No	INV2
574	IN_D	INVA	OUTCKT	No	INV2
646	IN_D	INVD	OUTCKT	No	A2BINV1
652	IN_D	INVD	OUTCKT	No	A2BINV3
2952	IN_D	INVD	OUTCKT	No	A2BINV3

The data sheet section provides information on each LVT part type. Each data sheet contains a part description, part features, quick reference data, ordering information, pin configuration, logic symbol or diagram, and function table.

To do simulations on a particular part type, refer to the LVT Netlists section of the book. That section contains files called "LVTXX.CIR" AND "LVTXXX.CIR" that are simulation test circuits for individual device types. The files are also in the LVT directory in the attached diskette. The "XX" in LVTXX.CIR refers to HS, or PS for the HSPICE and PSPICE protocols. Berkeley SPICE programs are called "LVTBSH.CIR" and "LVTBSP.CIR" and can be run using HSPICE and PSPICE simulators. See the BSPICE, HSPICE, or PSPICE subdirectories for the appropriate program you need. Transient analysis statements are included that can be changed to suit the application. Figure 3-1 shows how the test circuits are assembled.

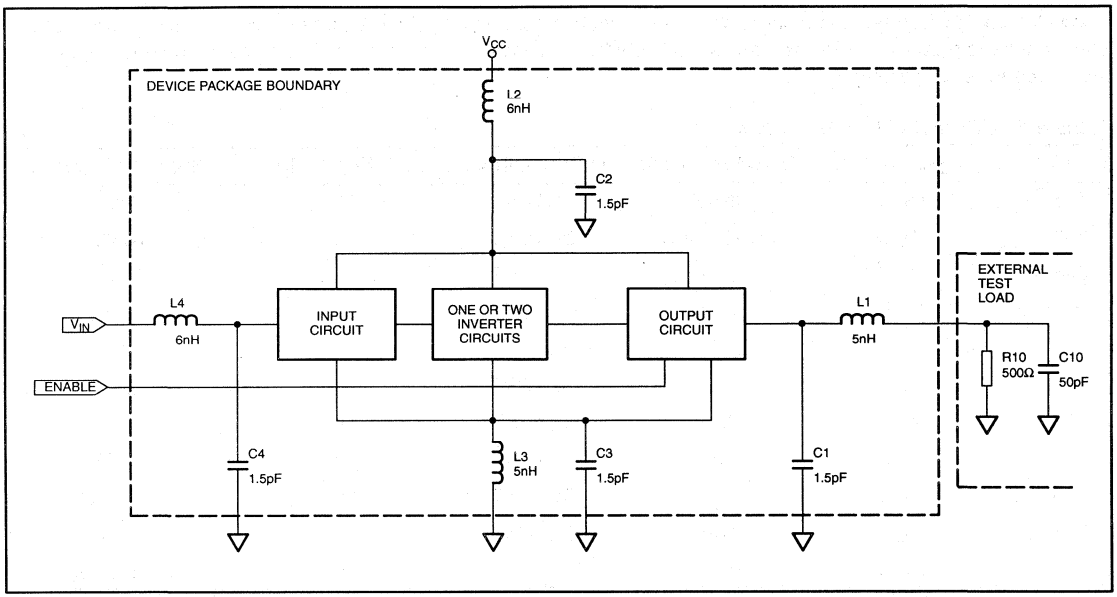


Figure 4-1. Examples of LVT Test Circuits

Also in the Netlists section of the book are files called LVTXXXYY.LIB. The "XXX" refers to NOM, SLO, or FAS for nominal, slow, or fast process corners. The "YY" refers to BS, HS or PS for the Berkeley SPICE, HSPICE, and PSPICE protocols. These files contain subcircuits for each part type, input, output, and inverter blocks, and nominal value package parasitics to simulate a die in a package. The values may be changed for a particular package, and these values are listed in the Packaging section of the book. LVTXXXYY.LIB is located in the BSPICE, HSPICE, and PSPICE subdirectories of the LVT directory on the attached diskette.

Libraries for primitive elements, such as resistors, diodes and transistors, etc., are also included for reference and are located in the BSPICE, HSPICE, and PSPICE subdirectories of the LVT directory on the attached diskette. The file names are called "LVTMDLXX.LIB". "XX" refers to BS, HS, or PS for the Berkeley SPICE, HSPICE, and PSPICE protocols.

For clarification, the following illustration shows how the three programs interact with each other:

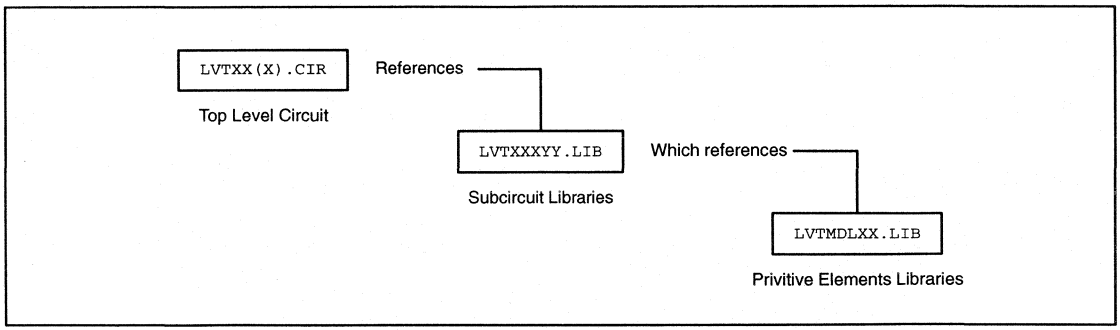


Figure 4-2. LVT SPICE Program Hierarchy

Note that in the top level program, LVTXX.CIR, the ".INC" and ".LIB" commands that specify the path to reference the other two programs should be modified to reflect your disk directory structure. Also, the top level program contains values for V_{CC} and input voltages. The input signal is a 3.3V pulse with a 2ns delay, 2.5ns rise and fall times, 10ns pulse width, and a 25ns period. V_{CC} is 3.3V, and the output enable voltage is 3.3V. A 500Ω, 50 pF load is connected. These conditions may be modified to suit the application.

LVT Short-form Datasheets

3.3V ABT Quad buffer (3-State) 74LVT125

FEATURES

- Quad bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up 3-State
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT125 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device combines low static and dynamic power dissipation with high speed and high output drive.

The 74LVT125 device is a quad buffer that is ideal for driving bus lines. The device features four Output Enables ($\overline{OE}0$, $\overline{OE}1$, $\overline{OE}2$, $\overline{OE}3$), each controlling one of the 3-State outputs.

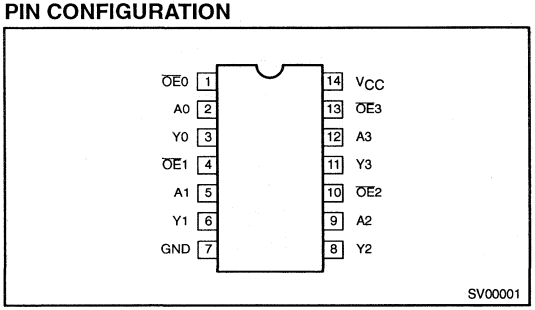
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 3.3V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

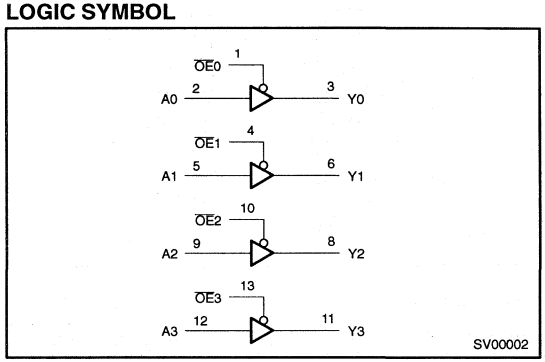
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
14-Pin Plastic Small Outline Package (SO)	–40°C to +85°C	74LVT125D	SOT108-1

PIN CONFIGURATION



LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 5, 9, 12	A0 – A3	Data inputs
3, 6, 8, 11	Y0 – Y3	Data outputs
1, 4, 10, 13	$\overline{OE}0$ – $\overline{OE}3$	Output enables
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

FUNCTION TABLE (EACH BUFFER)

INPUTS		OUTPUTS
$\overline{OE}n$	An	Yn
L	L	L
L	H	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "Off" state

3.3V ABT Octal inverting buffer (3-State) 74LVT240

FEATURES

- Octal bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Power-up 3-State
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model.

DESCRIPTION

The LVT240 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an octal inverting buffer that is ideal for driving bus lines. The device features two Output Enables ($1\overline{OE}$, $2\overline{OE}$), each controlling four of the 3-State outputs.

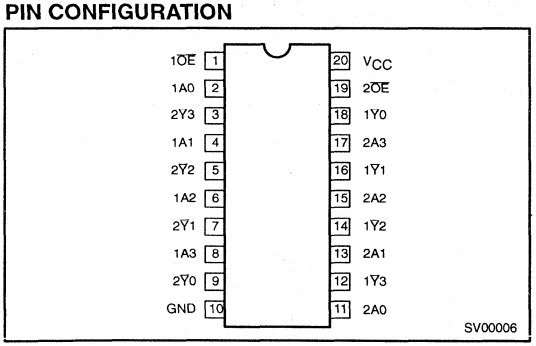
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	C_L = 50pF; V_{CC} = 3.3V	2.5	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.12	mA

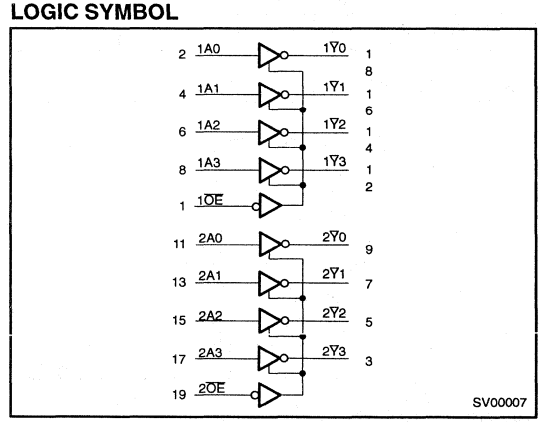
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-Pin Plastic Small Outline Large (300mil) (SOL)	–40°C to +85°C	74LVT240D	SOT163-1
20-Pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVT240DB	SOT399-1
20-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVT240PW	SOT360-1

PIN CONFIGURATION



LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
11, 13, 15, 17	2A0 – 2A3	Data inputs
18, 16, 14, 12	1$\overline{Y}$0 – 1$\overline{Y}$3	Data outputs
9, 7, 5, 3	2$\overline{Y}$0 – 2$\overline{Y}$3	Data outputs
1, 19	1$\overline{OE}$, 2$\overline{OE}$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUTS
n$\overline{OE}$	nAx	n$\overline{Y}$x
L	L	H
L	H	L
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "Off" state

3.3V ABT Octal buffer/line driver (3-State) 74LVT244A

FEATURES

- Octal bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Power-up 3-State
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT244A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an octal buffer that is ideal for driving bus lines. The device features two Output Enables ($\overline{OE}1$, $\overline{OE}2$), each controlling four of the 3-State outputs.

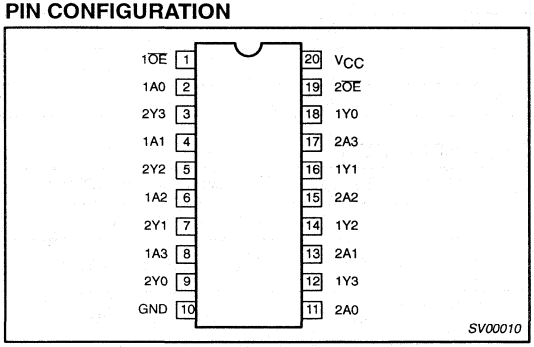
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 3.3V	2.5	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

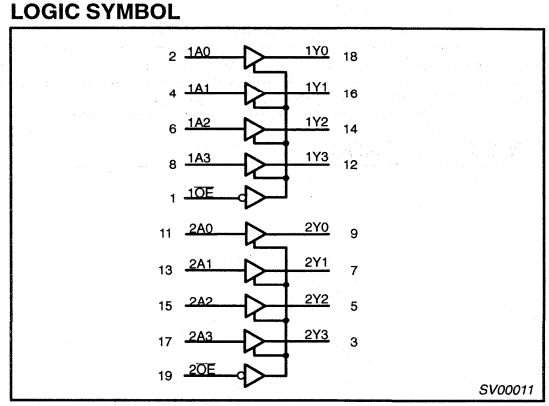
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-Pin Plastic Small Outline Large (300mil) (SOL)	–40°C to +85°C	74LVT244AD	SOT163-1
20-Pin Plastic Shrink Small Outline SSOP Type II	–40°C to +85°C	74LVT244ADB	SOT399-1
20-Pin Plastic Thin Shrink Small Outline TSSOP Type I	–40°C to +85°C	74LVT244APW	SOT360-1

PIN CONFIGURATION



LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
11. 13, 15, 17	2A0 – 2A3	Data inputs
18, 16, 14, 12	1Y0 – 1Y3	Data outputs
9, 7, 5, 3	2Y0 – 2Y3	Data outputs
1, 19	1$\overline{OE}$, 2$\overline{OE}$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{n}OE1$	nAx	nYx
L	L	L
L	H	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

3.3V ABT Octal transceiver with direction pin (3-State)

74LVT245

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT245 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

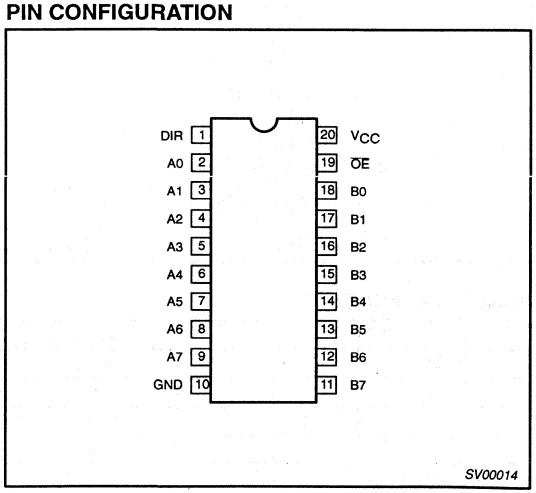
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 3.3V	2.4	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin Plastic Small Outline Large (300mil) (SOL)	–40°C to +85°C	74LVT245D	SOT163-1
20-pin Plastic Shrink Small Outline SSOP Type II	–40°C to +85°C	74LVT245DB	SOT339-1
20-pin Plastic Thin Shrink Small Outline TSSOP Type I	–40°C to +85°C	74LVT245PW	SOT360-1

PIN CONFIGURATION



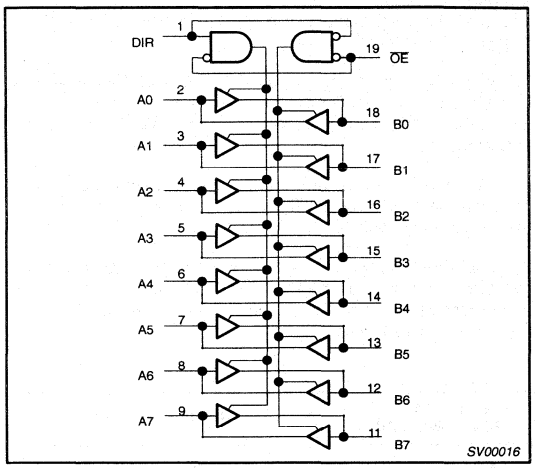
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	DIR	Direction control input
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs/outputs (A side)
18, 17, 16, 15, 14, 13, 12, 11	$\overline{B0}$ – $\overline{B7}$	Data inputs/outputs ($\overline{B}$ side)
19	$\overline{OE}$	Output enable input (active–Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

3.3V ABT Octal transceiver with direction pin (3-State)

74LVT245

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$n	**DIR**	**An**	**Bn**
L	L	An= Bn	Inputs
L	H	Inputs	Bn =An
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "Off" state

3.3V ABT Octal D flip-flop | 74LVT273

FEATURES

- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Buffered asynchronous Master Reset
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Power-up reset
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus

DESCRIPTION

The LVT273 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced Low independent of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the CP and $\overline{MR}$ are common elements.

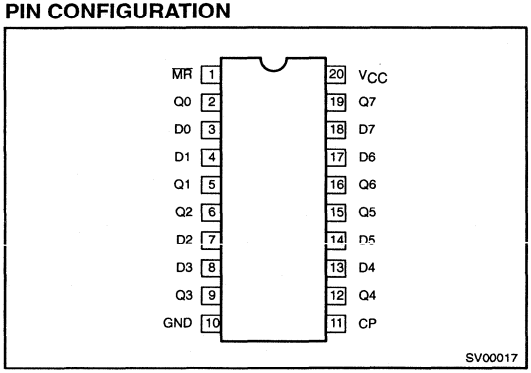
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 3.3V	3.5	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin Plastic Small Outline Large (300mil)(SOL)	–40°C to +85°C	74LVT273D	SOT163-1
20-pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVT273DB	SOT399-1
20-pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVT273PW	SOT360-1

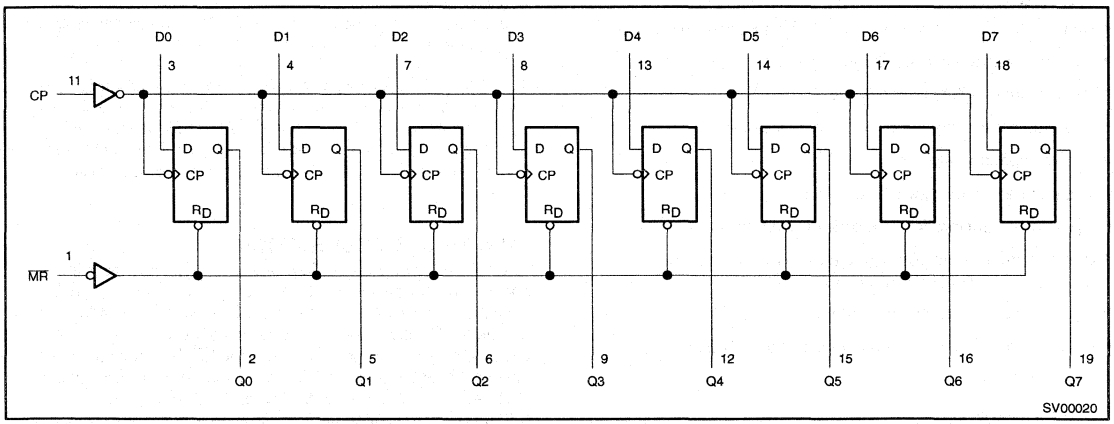
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
11	CP	Clock pulse input (active rising edge)
3, 4, 7, 8, 13, 14, 17, 18	D0 – D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	Q0 – Q7	Data outputs
1	$\overline{MR}$	Master Reset input (active-Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING
$\overline{MR}$	CP	D_n	Q0 – Q7	MODE
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"
H	L	X	Q_0	Retain state

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
Q_0 = Output as it was

3.3V ABT Octal latched transceiver with dual enable (3-State)

74LVT543

FEATURES

- Combines 74LVT245 and 74LVT373 type functions in one device
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Output capability: +64mA/–32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT543 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of data transfer in either direction. The outputs are guaranteed to sink 64mA.

FUNCTIONAL DESCRIPTION

The 'LVT543 contains two sets of eight D–type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable ($\overline{EAB}$) input and the A-to-B Latch Enable ($\overline{LEAB}$) input are Low the A-to-B path is transparent. A subsequent Low-to-High transition of the $\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

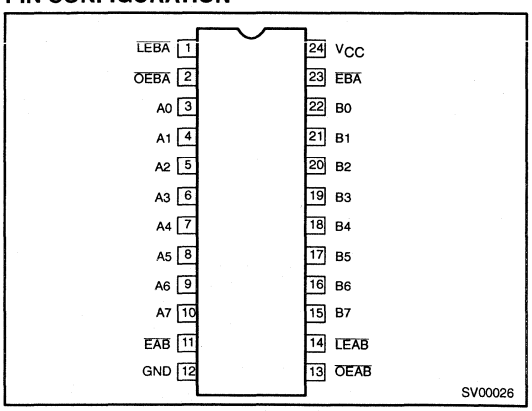
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 3.3V	3.3	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4.5	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	11	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	.13	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-pin Plastic Small Outline Large (300mil) (SOL)	–40°C to +85°C	74LVT543D	SOT137-1
24-pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVT543DB	SOT340-1
24-pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVT543PW	SOT355-1

PIN CONFIGURATION



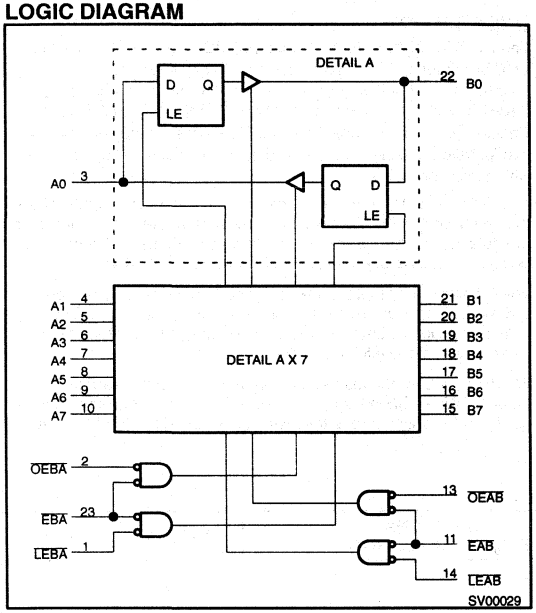
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
14, 1	$\overline{LEAB}$ / $\overline{LEBA}$	A to B / B to A Latch Enable input (active-Low)
11, 23	$\overline{EAB}$ / $\overline{EBA}$	A to B / B to A Enable input (active-Low)
13, 2	$\overline{OEAB}$ / $\overline{OEBA}$	A to B / B to A Output Enable input (active-Low)
3, 4, 5, 6, 7, 8, 9, 10	A0 – A7	Port A, 3-State outputs
22, 21, 20, 19, 18, 17, 16, 15	B0 – B7	Port B, 3-State outputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

3.3V ABT Octal latched transceiver with dual enable (3-State)

74LVT543

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OEXX}$	$\overline{EXX}$	$\overline{LEXX}$	An or Bn	Bn or An	
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	H L	Latch + Display
L L	L L	L L	H L	H L	Transparent
L	L	H	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX = AB or BA)
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX = AB or BA)
X = Don't care
↑ = Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX = AB or BA)
NC= No change
Z = High impedance or "off" state

3.3V ABT Octal D-type transparent latch (3-State) 74LVT573

FEATURES

- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- 3-State output buffers
- Common output enable
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- Power-up 3-State
- Power-up reset
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT573 is a high-performance BiCMOS product designed for VCC operation at 3.3V. This device is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates. The 74LVT573 has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

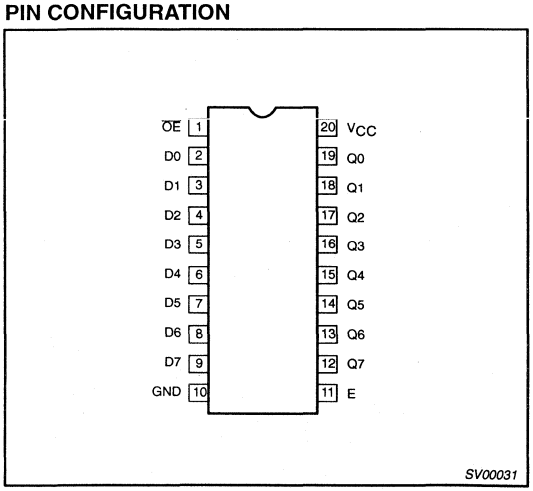
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	C_L = 50pF; V_{CC} = 3.3V	2.7	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	.13	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin Plastic Small Outline Large (300mil) (SOL)	–40°C to +85°C	74LVT573D	SOT163-1
20-pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVT573DB	SOT399-1
20-pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVT573PW	SOT360-1

PIN CONFIGURATION

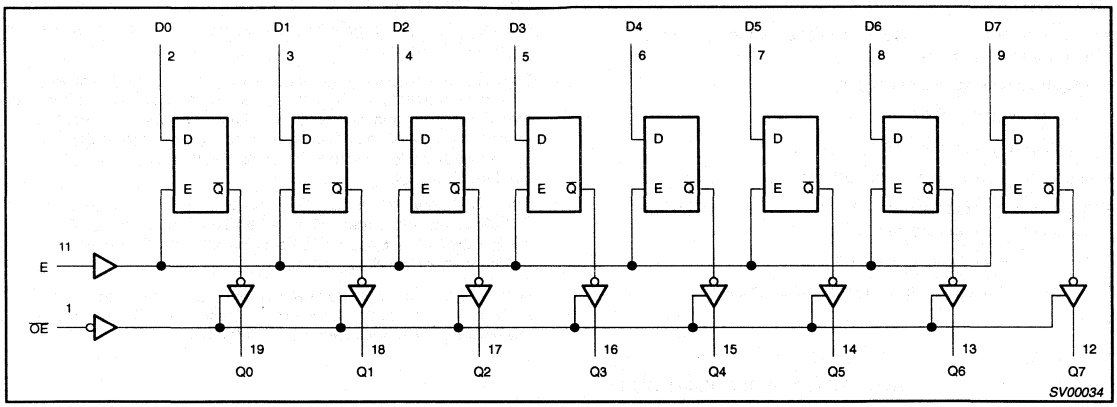


PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9	D0-D7	Data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0-Q7	Data outputs
11	E	Enable input (active-High)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

3.3V ABT Octal D-type transparent latch (3-State) 74LVT573

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING
$\overline{OE}$	E	Dn	REGISTER	Q0 – Q7	MODE
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	l h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

3.3V ABT Octal D-type flip-flop (3-State) 74LVT574

FEATURES

- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- 3-State outputs for bus interfacing
- Common output enable
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT574 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates. The state of each D input (one set-up time before the Low-to-High clock transition) is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the clock operation.

When $\overline{OE}$ is Low, the stored data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "off" state, which means they will neither drive nor load the bus.

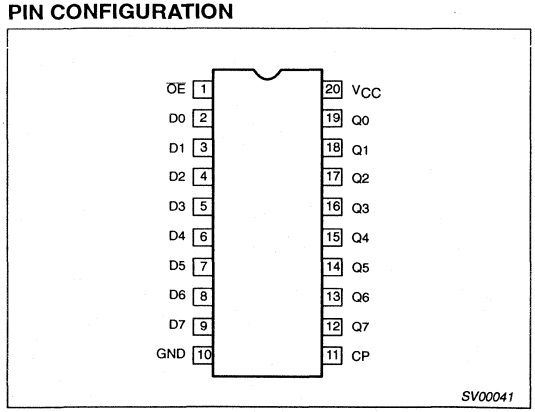
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 3.3V	3.6 4.3	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	.13	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-Pin Plastic Small Outline Large (300mil) (SOL)	–40°C to +85°C	74LVT574D	SOT163-1
20-Pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVT574DB	SOT399-1
20-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVT574PW	SOT360-1

PIN CONFIGURATION

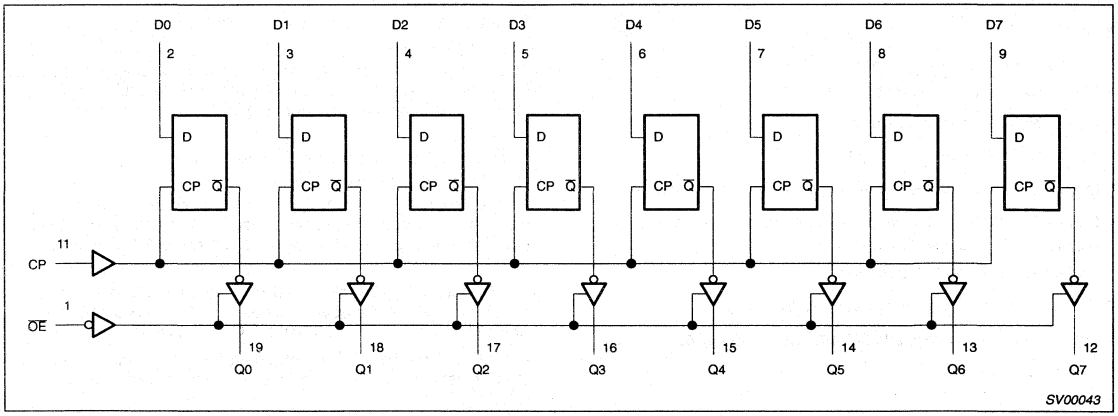


PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-low)
2, 3, 4, 5, 6, 7, 8, 9	D0-D7	Data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0-Q7	Data outputs
11	CP	Clock pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

3.3V ABT Octal D-type flip-flop (3-State) 74LVT574

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING
$\overline{OE}$	CP	Dn	REGISTER	Q0 – Q7	MODE
L	L	X	Q0	Q0	Retain output
L L	↑ ↑	l h	L H	L H	Load and read register
L	L	X	NC	NC	Hold
H	X	X	NC	Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
Q0 = output as it was

3.3V ABT Octal bus transceiver/register (3-State) 74LVT646

FEATURES

- Combines 74LVT245 and 74LVT574 type functions in one device
- Independent registers for A and B buses
- Multiplexed real–time and stored data
- Output capability: +64mA/–32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- Power-up 3-State
- Power-up reset
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT646 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device consists of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers.

Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High.

Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The Select (SAB, SBA) pins determine whether data is stored or transferred through the device in real–time. The DIR determines which bus will receive data when the $\overline{OE}$ is active (Low).

In the isolation mode ($\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time. The examples on the next page demonstrate the four fundamental bus management functions that can be performed with the 74LVT646.

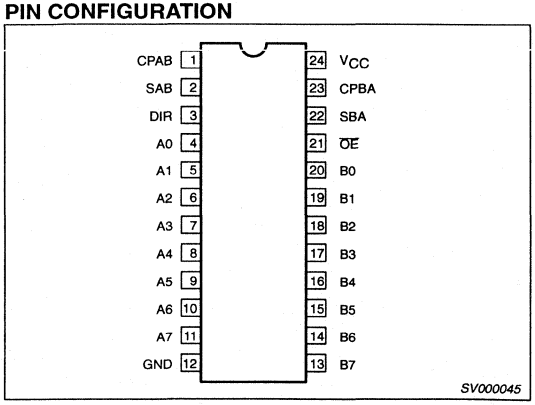
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 3.3V	2.8	ns
C_{IN}	Input capacitance CP, S, $\overline{OE}$, DIR	$V_{I/O}$ = 0V or 3.0V	4.5	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	11	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-Pin plastic Small Outline Large (300mil) (SOL)	–40°C to +85°C	74LVT646D	SOT137-1
24-Pin Plastic Shrink Small Outline SSOP Type II	–40°C to +85°C	74LVT646DB	SOT340-1
24-Pin Plastic Thin Shrink Small Outline TSSOP Type I	–40°C to +85°C	74LVT646PW	SOT355-1

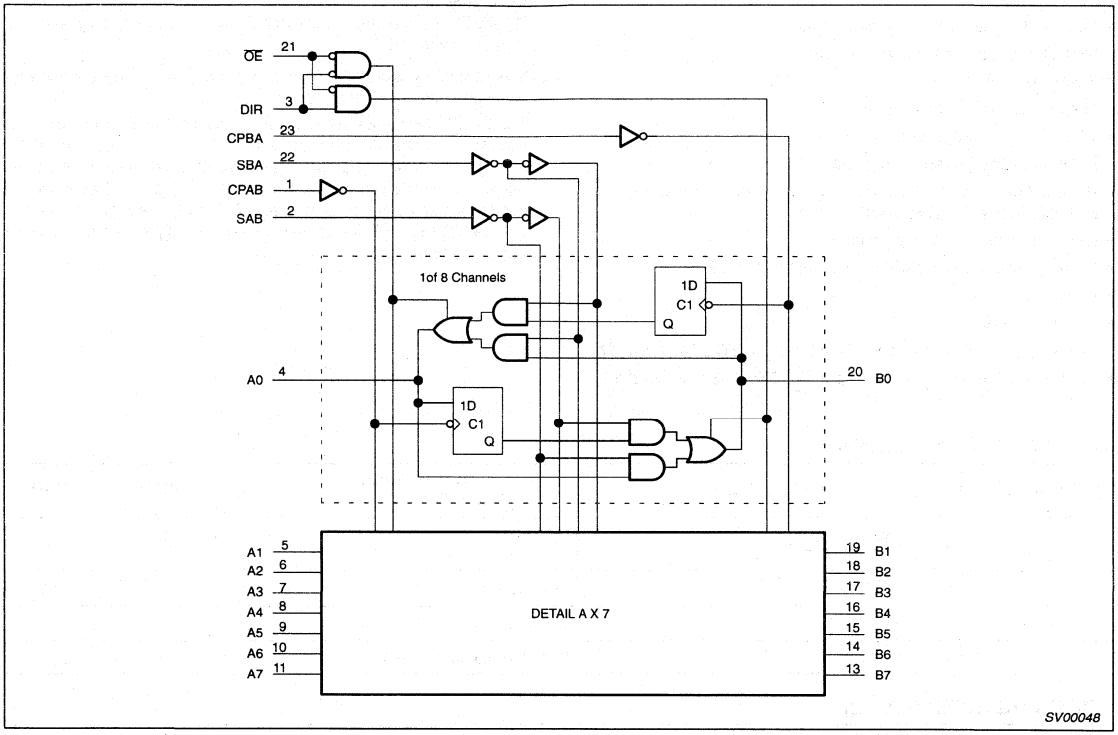
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 23	CPAB / CPBA	A to B clock input / B to A clock input
2, 22	SAB / SBA	A to B select input / B to A select input
3	DIR	Direction control input
4, 5, 6, 7, 8, 9, 10, 11	A0 – A7	Data inputs/outputs (A side)
20, 19, 18, 17, 16, 15, 14, 13	B0 – B7	Data inputs/outputs (B side)
21	$\overline{OE}$	Output enable input (active-low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	An	Bn	
X	X	↑	X	X	X	Input	Unspecified output*	Store A, B unspecified
X	X	X	↑	X	X	Unspecified output*	Input	Store B, A unspecified
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Stored A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the $\overline{OE}$ input. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

3.3V ABT Octal Transceiver/register, non-inverting (3-State)

74LVT652

FEATURES

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- 3-State outputs
- Output capability: +64mA/–32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up 3-State
- Power-up reset
- Latch–up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT652 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device combines low static and dynamic power dissipation with high speed and high output drive.

The 74LVT652 transceiver/register consists of bus transceiver circuits with 3-State outputs, D–type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{OEBA}$) and Select (SAB, SBA) pins are provided for bus management.

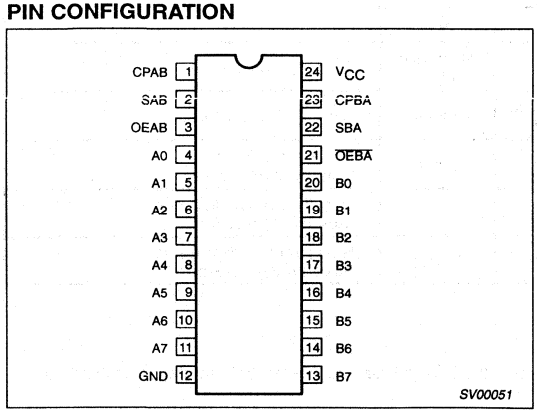
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 3.3V	2.8	ns
C_{IN}	Input capacitance	V_I = 0V or 3V	4.5	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3V	11	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	.13	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-Pin Plastic Small Outline Large (300mil) (SOL)	–40°C to +85°C	74LVT652D	SOT137-1
24-Pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVT652DB	SOT340-1
24-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVT652PW	SOT355-1

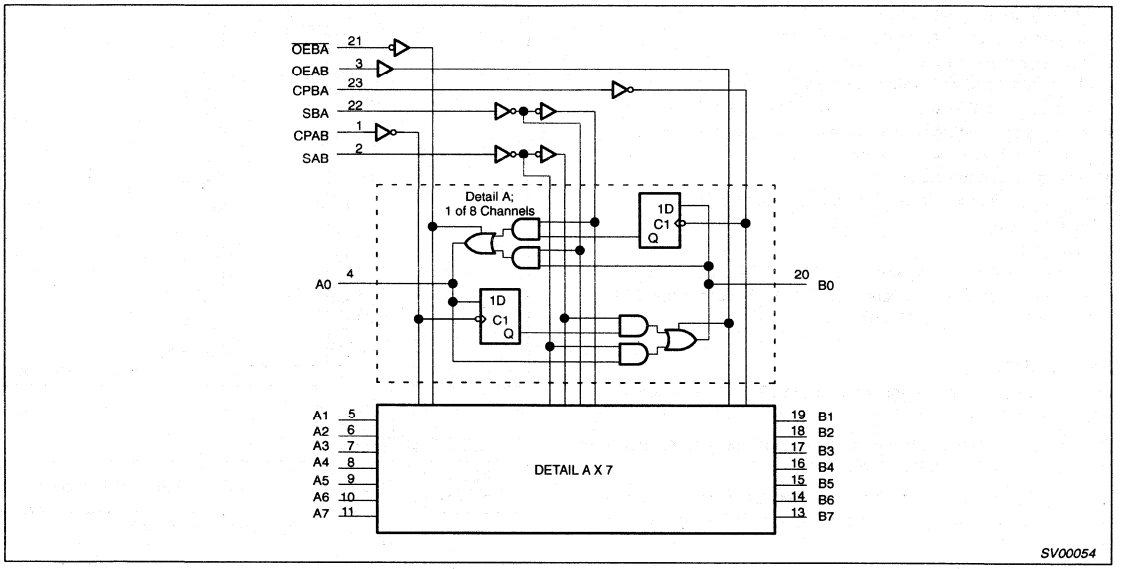
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 23	CPAB / CPBA	A to B clock input / B to A clock input
2, 22	SAB / SBA	A to B select input / B to A select input
3, 21	OEAB / $\overline{OEBA}$	A to B Output Enable input (active-High) / B to A Output Enable input (active-Low)
4, 5, 6, 7, 8, 9, 10, 11	A0 – A7	Data inputs/outputs (A side)
20, 19, 18, 17, 16, 15, 14, 13	B0 – B7	Data inputs/outputs (B side)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	An	Bn	
L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B data
X H	H H	↑ ↑	H or L ↑	X **	X X	Input	Unspecified** Output*	Store A, Hold B Store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X **	Unspecified** Output*	Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Store A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus Stored B data to A bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the $\overline{OEBA}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
** If both Select controls (SAB and SBA) are Low, then clocks can occur simultaneously. If either Select control is High, the clocks must be staggered in order to load both registers.

3.3V LVT Octal registered transceiver (3-State) 74LVT2952

FEATURES

- 8-bit registered transceiver
- Independent registers for A and B buses
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up reset
- Power-up 3-State
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

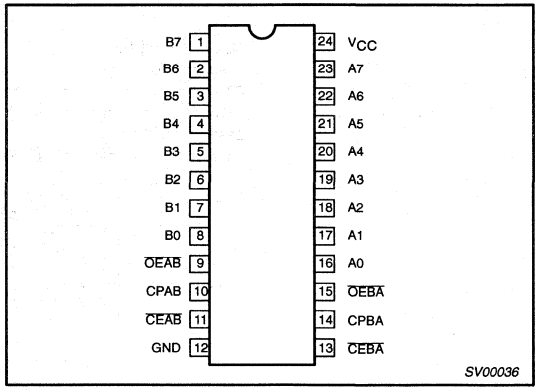
The LVT2952 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device combines low static and dynamic power dissipation with high speed and high output drive.

The 74LVT2952 device is an 8-bit registered transceiver. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses.

Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{CEXX}$) is Low. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable ($\overline{OEXX}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
10, 14	CPAB / CPBA	Clock input A to B / Clock input B to A
11, 13	$\overline{CEAB}$ / $\overline{CEBA}$	Clock enable input A to B / Clock enable input B to A
16, 17, 18, 19, 20, 21, 22, 23	A0 – A7	Data inputs/outputs (A side)
8, 7, 6, 5, 4, 3, 2, 1	B0 – B7	Data outputs/outputs (B side)
9, 15	$\overline{OEAB}$ / $\overline{OEBA}$	Output enable inputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

QUICK REFERENCE DATA

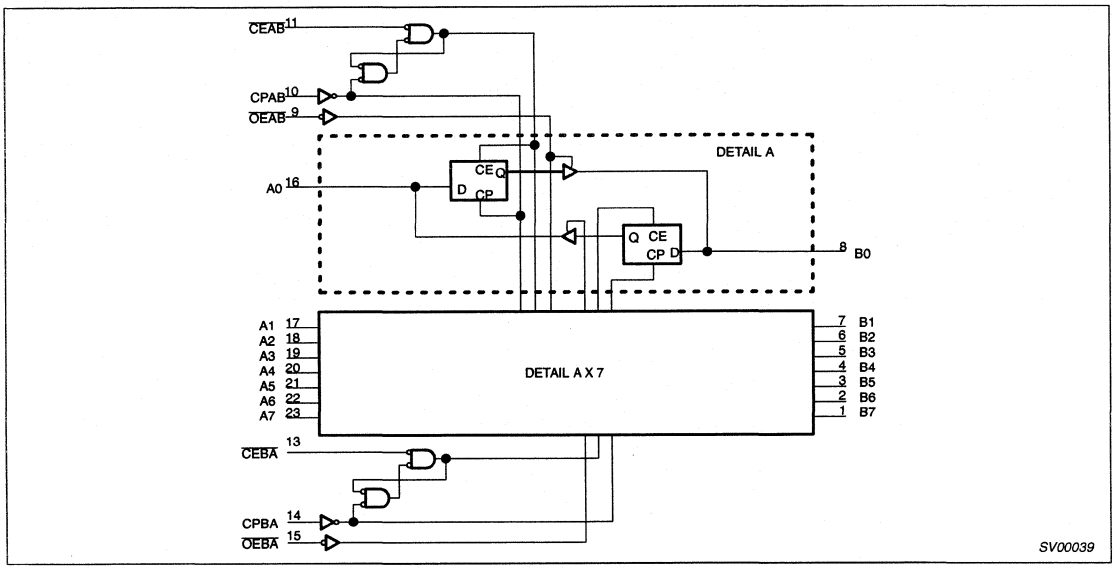
SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPBA to An or CPAB to Bn	C_L = 50pF; V_{CC} = 3.3V	3.1 3.8	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-Pin Plastic Small Outline Large (300mil) (SOL)	–40°C to +85°C	74LVT2952D	SOT137-1
24-Pin Plastic Shrink Small Outline SSOP Type II	–40°C to +85°C	74LVT2952DB	SOT340-1
24-Pin Plastic Thin Small Shrink Outline TSSOP Type I	–40°C to +85°C	74LVT2952PW	SOT355-1

3.3V LVT Octal registered transceiver (3-State) 74LVT2952

LOGIC DIAGRAM



FUNCTION TABLE for Register An or Bn

INPUTS			INTERNAL Q	OPERATING MODE
An or Bn	CPXX	$\overline{CEXX}$		
X	X	H	NC	Hold data
L H	↑ ↑	L L	L H	Load data

H = HIgh voltage level
L = Low voltage level
↑ = Low-to-High transition
X = Don't care
XX = AB or BA
NC = No change

FUNCTION TABLE for Output Enable

INPUTS	INTERNAL Q	An or Bn OUTPUTS	OPERATING MODE
$\overline{OEXX}$			
H	X	Z	Disable outputs
L L	L H	L H	Enable outputs

H = High voltage level
L = Low voltage level
X = Don't care
XX = AB or BA
Z = High impedance "off" state

LVT Netlists

LVT BERKELEY SPICE MODELS (for HSPICE Simulation)

```
*****************************************************************************
* LVTBSH.CIR
* Low Voltage BiCMOS Logic
* Standard Logic Product Group
* Philips Semiconductors
* 4/5/95
*****************************************************************************
* To simulate a particular device, locate the device in the section
* of this file titled "LVT Circuit Models.  Delete the comment mark, "*",
* in the leading column for that device only.  Make sure that the
* comment "*" is present for all other devices on the list.
* To simulate with nominal, slow, or fast process parameters, go
* to the section of the file with the particular process corner you want
* and remove the "*".  Insure that the other parameters in the set are
* remarked out with the "*" added.  You may also wish to adjust the
* values of the load and parasitic inductors and capacitors as found in
* the LVTXXXBS.LIB files according to the package chosen.  The basic
* files use nominal values.
*****************************************************************************
*
*
* Common Models for Nominal, Slow and Fast
* (Do not comment out this .INCLUDE line)
.INCLUDE "C:\SPICE\LVT\BSPICE\LVTMDLBS.LIB"

* Nominal Parameters
.INCLUDE "C:\SPICE\LVT\BSPICE\LVTNOMBS.LIB"

* Slow Parameters
* .INCLUDE "C:\SPICE\LVT\BSPICE\LVTSLOBS.LIB"

* Fast Parameters
* .INCLUDE "C:\SPICE\LVT\BSPICE\LVTFASBS.LIB"

*** LVT Circuit Models

* Part Type    In   En   Out  Vcc
* XL125        5    7    4    100    INV1

* XL240        5    7    4    100    NINV

* XL244        5    7    4    100    INV1

* XL245        5    7    4    100    A2BINV1

* XL273        5    7    4    100    INV2

* XL543        5    7    4    100    A2BINV2

XL573         5    7    4    100    INV2

* XL574        5    7    4    100    INV2

* XL646        5    7    4    100    A2BINV1

* XL652        5    7    4    100    A2BINV3

* XL2952       5    7    4    100    A2BINV3

* EXTERNAL LOAD
```

```
R10 4 0 500
C10 4 0 50PF

* POWER
VCC 100 0 3.3

* DRIVE (Note: VOE is active hi not like real ckt.)
VIN 5 0 PULSE 0.0 3.3 2N 2.5N 2.5N 10N 25N
VOE 7 0 3.3

.TRAN   1.000000E-11  2.500000E-08
.TEMP  .2500E+02
.OPTION  ACCT NODE OPTS LIST LIMTIM=50
+         GMIN=1.00E-12 RELTOL=1.00E-03 ABSTOL=1.00E-12
+         VNTOL=1.00E-06 TRTOL=7.00E+00
+         ITL1=1.00E+02 ITL2=1.00E+02 ITL3=4.00E+00 ITL4=2.50E+01
+         ITL5=1.00E+06 LVLTIM=2.00E+00 TNOM=+2.50E+01 LIMPTS=99999
+         CHGTOL=1.00E-14
+         MAXORD= .20E+01
+         METHOD=TRAP
+         DELMAX= 6.00E-10
+         POST
.END
```

LVT BERKELEY SPICE MODELS (for PSPICE Simulation)

```
**********************************************************************
* LVTBSP.CIR
* Low Voltage BiCMOS Logic
* Standard Logic Product Group
* Philips Semiconductors
* 4/5/95
**********************************************************************
* To simulate a particular device, locate the device in the section
* of this file titled "LVT Circuit Models.  Delete the comment mark, "*",
* in the leading column for that device only.  Make sure that the
* comment "*" is present for all other devices on the list.
* To simulate with nominal, slow, or fast process parameters, go
* to the section of the file with the particular process corner you want
* and remove the "*".  Insure that the other parameters in the set are
* remarked out with the "*" added.  You may also wish to adjust the
* values of the load and parasitic inductors and capacitors as found in
* the LVTXXXBS.LIB files according to the package chosen.  The basic
* files use nominal values.
**********************************************************************
*
*
* Common Models for Nominal, Slow and Fast
* (Do not comment out this .LIB line)
.LIB "C:\SPICE\LVT\BSPICE\LVTMDLBS.LIB"

* Nominal Parameters
.LIB "C:\SPICE\LVT\BSPICE\LVTNOMBS.LIB"

* Slow Parameters
* .LIB "C:\SPICE\LVT\BSPICE\LVTSLOBS.LIB"

* Fast Parameters
* .LIB "C:\SPICE\LVT\BSPICE\LVTFASBS.LIB"

*** LVT Circuit Models

* Part Type    In  En  Out  Vcc
* XL125        5   7   4    100   INV1

* XL240        5   7   4    100   NINV

* XL244        5   7   4    100   INV1

* XL245        5   7   4    100   A2BINV1

XL273          5   7   4    100   INV2

* XL543        5   7   4    100   A2BINV2

* XL573        5   7   4    100   INV2

* XL574        5   7   4    100   INV2

* XL646        5   7   4    100   A2BINV1

* XL652        5   7   4    100   A2BINV3

* XL2952       5   7   4    100   A2BINV3

* EXTERNAL LOAD
```

```
R10 4 0 500
C10 4 0 50PF

* POWER
VCC 100 0 3.3

* DRIVE (Note: VOE is active hi not like real ckt.)
VIN 5 0 PULSE 0.0 3.3 2N 2.5N 2.5N 10N 25N
VOE 7 0 3.3

.TRAN   1N  25N  ; 0 1P
.OPTIONS ITL4=50
.TEMP  25
.PROBE
.END
```

LVT HSPICE MODELS

```
*****************************************************************************
* LVTHS.CIR
* Low Voltage BiCMOS Logic
* Standard Logic Product Group
* Philips Semiconductors
* 4/5/95
*****************************************************************************
* To simulate a particular device, locate the device in the section
* of this file titled "LVT Circuit Models.  Delete the comment mark, "*",
* in the leading column for that device only.  Make sure that the
* comment "*" is present for all other devices on the list.
* To simulate with nominal, slow, or fast process parameters, go
* to the section of the file with the particular process corner you want
* and remove the "*".  Insure that the other parameters in the set are
* remarked out with the "*" added.  You may also wish to adjust the
* values of the load and parasitic inductors and capacitors as found in
* the LVTXXXHS.LIB files according to the package chosen.  The basic
* files use nominal values.
*****************************************************************************
*
*
* Common Models for Nominal, Slow and Fast
* (Do not comment out this INCLUDE line)
.INCLUDE "C:\SPICE\LVT\HSPICE\LVTMDLHS.LIB"

* Nominal Parameters
.INCLUDE "C:\SPICE\LVT\HSPICE\LVTNOMHS.LIB"

* Slow Parameters
* .INCLUDE "C:\SPICE\LVT\HSPICE\LVTSLOHS.LIB"

* Fast Parameters
* .INCLUDE "C:\SPICE\LVT\HSPICE\LVTFASHS.LIB"

*** LVT Circuit Models

* Part Type    In   En   Out    Vcc

* XL125         5    7    4     100    INV1

XL240          5    7    4     100    NINV

* XL244         5    7    4     100    INV1

* XL245         5    7    4     100    A2BINV1

* XL273         5    7    4     100    INV2

* XL543         5    7    4     100    A2BINV2

* XL573         5    7    4     100    INV2

* XL574         5    7    4     100    INV2

* XL646         5    7    4     100    A2BINV1

* XL652         5    7    4     100    A2BINV3

* XL2952        5    7    4     100    A2BINV3
```

```
* EXTERNAL LOAD
R10 4 0 500
C10 4 0 50PF

* POWER
VCC 100 0 3.3

* DRIVE (Note: VOE is active hi not like real ckt.)
VIN 5 0 PULSE 0.0 3.3 2N 2.5N 2.5N 10N 25N
VOE 7 0 3.3

.TRAN   1.000000E-11  2.500000E-08
.TEMP  .2500E+02
.OPTION  ACCT NODE OPTS LIST LIMTIM=50
+         GMIN=1.00E-12 RELTOL=1.00E-03 ABSTOL=1.00E-12
+         VNTOL=1.00E-06 TRTOL=7.00E+00
+         ITL1=1.00E+02 ITL2=1.00E+02 ITL3=4.00E+00 ITL4=2.50E+01
+         ITL5=1.00E+06 LVLTIM=2.00E+00 TNOM=+2.50E+01 LIMPTS=99999
+         CHGTOL=1.00E-14
+         MAXORD= .20E+01
+         METHOD=TRAP
+         DELMAX= 6.00E-10
+         POST
.END
```

LVT PSPICE MODELS

```
*****************************************************************************
* LVTPS.CIR
* Low Voltage BiCMOS Logic
* Standard Logic Product Group
* Philips Semiconductors
* 4/5/95
*****************************************************************************
* To simulate a particular device, locate the device in the section
* of this file titled "LVT Circuit Models.  Delete the comment mark, "*",
* in the leading column for that device only.  Make sure that the
* comment "*" is present for all other devices on the list.
* To simulate with nominal, slow, or fast process parameters, go to
* the section of the file with the particular process corner you want
* and remove the "*".  Insure that the other parameters in the set are
* remarked out with the "*" added.  You may also wish to adjust the
* values of the load and parasitic inductors and capacitors as found in
* the LVTXXXPS.LIB files according to the package chosen.  The basic
* files use nominal values.
*****************************************************************************
*
*
* Common Models for Nominal, Slow and Fast
* (Do not comment out this .LIB line)
.LIB "C:\SPICE\LVT\PSPICE\LVTMDLPS.LIB"

* Nominal Parameters
.LIB "C:\SPICE\LVT\PSPICE\LVTNOMPS.LIB"

* Slow Parameters
* .LIB "C:\SPICE\LVT\PSPICE\LVTSLOPS.LIB"

* Fast Parameters
* .LIB "C:\SPICE\LVT\PSPICE\LVTFASPS.LIB"

*** LVT Circuit Models

* Part Type    In  En  Out  Vcc  Subckt.
* XL125        5   7   4    100   INV1

* XL240        5   7   4    100   NINV

* XL244        5   7   4    100   INV1

* XL245        5   7   4    100   A2BINV1

* XL273        5   7   4    100   INV2

XL543          5   7   4    100   A2BINV2

* XL573        5   7   4    100   INV2

* XL574        5   7   4    100   INV2

* XL646        5   7   4    100   A2BINV1

* XL652        5   7   4    100   A2BINV3

* XL2952       5   7   4    100   A2BINV3

* EXTERNAL LOAD
```

```
R10 4 0 500
C10 4 0 50PF

* POWER
VCC 100 0 3.3

* DRIVE (Note: VOE is active hi not like real ckt.)
VIN 5 0 PULSE 0.0 3.0 2N 2.5N 2.5N 10N 25N
VOE 7 0 3.0

.TRAN   1N  25N  ; 0 1P
.OPTIONS ITL4=50
.TEMP  25
.PROBE
.END
```

LVTNOMBS.LIB Subcircuit

```
*****************************************************************************
* LVT BERKELEY SPICE SUBCIRCUIT LIBRARY
* LVTNOMBS.LIB
* NOMINAL PROCESS CORNER
* STANDARD LOGIC PRODUCT GROUP
* PHILIPS SEMICONDUCTORS
* 4/5/95
*****************************************************************************
.SUBCKT INV1 D E Q VCC
* USE THIS MODEL FOR 74LVT125 - 244
*    D   INTVCC   INTGND
X1   1     99        6                    IN_DN
*    D    INT   INTVCC   INTGND
X2   1     90     99        6           INVBN
*   INT    E    Q    INTVCC   INTGND   INTOGND
X4   90    3    2      99        6        6     OUTCKTN
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1
.SUBCKT INV2 D E Q VCC
* USE THIS MODEL FOR 74LVT273 - 573 - 574
*    D   INTVCC   INTGND
X1   1     99        6                    IN_DN
*    D    INT   INTVCC   INTGND
X2   1     90     99        6           INVAN
*   INT    E    Q    INTVCC   INTGND   INTOGND
X4   90    3    2      99        6        6     OUTCKTN
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV2
.SUBCKT NINV D E Q VCC
* USE THIS MODEL FOR 74LVT240 (ONLY INVERTING PART)
*    D   INTVCC   INTGND
X1   1     99        6                    IN_DN
*    D    INT   INTVCC   INTGND
X2   1     90     99        6           INVBN
*    D    INT   INTVCC   INTGND
X3   90     91     99        6           INVBN
*   INT    E    Q    INTVCC   INTGND   INTOGND
X4   91    3    2      99        6        6     OUTCKTN
*
L1 2 Q 5NH
```

```
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINV
.SUBCKT A2BINV1 D E Q VCC
* USE THIS MODEL FOR 74LVT245 - 646
*   D  INTVCC  INTGND
X1  1    99       6                IN_DN
*   D   INT  INTVCC  INTGND
X2  1    90    99       6          INVDN
*  INT   E   Q  INTVCC  INTGND  INTOGND
X3  90   3   2    99       6       6    OUTCKTN
*   D  INTVCC  INTGND
X4  2    99       6                IN_DN
*   D   INT  INTVCC  INTGND
X5  2    91    99       6          INVDN
*  INT   E   Q  INTVCC  INTGND  INTOGND
X6  91   8   1    99       6       6    OUTCKTN
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV1
.SUBCKT A2BINV2 D E Q VCC
* USE THIS MODEL FOR 74LVT543
*   D  INTVCC  INTGND
X1  1    99       6                IN_DN
*   D   INT  INTVCC  INTGND
X2  1    90    99       6          INVCN
*  INT   E   Q   INTVCC  INTGND  INTOGND
X3  90   3   2    99       6       6    OUTCKTN
*   D  INTVCC  INTGND
X4  2    99       6                IN_DN
*   D   INT  INTVCC  INTGND
X5  2    91    99       6          INVCN
*  INT   E   Q   INTVCC  INTGND  INTOGND
X6  91   8   1    99       6       6    OUTCKTN
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV2
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.SUBCKT A2BINV3 D E Q VCC
* USE THIS MODEL FOR 74LVT652 - 2952
*   D  INTVCC  INTGND
X1  1    99       6                  IN_DN
*   D   INT  INTVCC  INTGND
X2  1    90    99      6           INVDN
*  INT   E   Q   INTVCC  INTGND  INTOGND
X3  90   3   2     99       6       6    OUTCKTN
*   D  INTVCC  INTGND
X4  2    99       6                  IN_DN
*   D   INT  INTVCC  INTGND
X5  2    91    99      6           INVDN
*  INT   E   Q   INTVCC  INTGND  INTOGND
X6  91   8   1     99       6       6    OUTCKTN
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV3

* Philips Semiconductors - IN_DN  - Nominal
.SUBCKT IN_DN 9902 9901 9904
X2Q1  9902 9902 9904 9904 ESDXXXXN
M1M1  9901 9902 1 9901 MHS4XPEN L=1.0U W=3.298U
+ AD=6.596P AS=6.596P PD=10.596U PS=10.596U NRD=0.606 NRS=0.606
M1M2  9901 1 2 9901 MHS4XPEN L=1.0U W=13.298U
+ AD=26.596P AS=26.596P PD=30.596U PS=30.596U NRD=0.150 NRS=0.150
M1M3  1 9902 9904 9904 MHS4XNEN L=1.0U W=1.926U
+ AD=3.852P AS=3.852P PD=7.852U PS=7.852U NRD=1.038 NRS=1.038
M1M4  9902 1 9904 9904 MHS4XNEN L=1.0U W=1.926U
+ AD=3.852P AS=3.852P PD=7.852U PS=7.852U NRD=1.038 NRS=1.038
Q1Q1  9902 2 2 DA04AASN
.ENDS IN_DN
* Philips Semiconductors - INVAN - Nominal
.SUBCKT INVAN 9902 9903 9901 9904
MM1     9901 9902 9903 9901 MHS4XPEN L=1.0U W=94.298U
+ AD=188.596P AS=188.596P PD=192.596U PS=192.596U NRD=0.021 NRS=0.021
MM2     9903 9902 9904 9904 MHS4XNEN L=1.0U W=33.926U
+ AD=67.852P AS=67.852P PD=71.852U PS=71.852U NRD=0.059 NRS=0.059
.ENDS INVAN
* Philips Semiconductors - INVBN
.SUBCKT INVBN 9902 9903 9901 9904
MM1     9901 9902 9903 9901 MHS4XPEN L=1.0U W=199.298U
+ AD=398.596P AS=398.596P PD=402.596U PS=402.596U NRD=0.010 NRS=0.010
MM2     9903 9902 9904 9904 MHS4XNEN L=1.0U W=104.926U
+ AD=209.852P AS=209.852P PD=213.852U PS=213.852U NRD=0.019 NRS=0.019
.ENDS INVBN
* Philips Semiconductors - INVCN
.SUBCKT INVCN 9902 9903 9901 9904
MM1     9901 9902 9903 9901 MHS4XPEN L=1.0U W=139.298U
+ AD=278.596P AS=278.596P PD=282.596U PS=282.596U NRD=0.014 NRS=0.014
MM2     9903 9902 9904 9904 MHS4XNEN L=1.0U W=149.926U
+ AD=299.852P AS=299.852P PD=303.852U PS=303.852U NRD=0.013 NRS=0.013
.ENDS INVCN
```

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* Philips Semiconductors - INVDN
.SUBCKT INVDN 9902 9903 9901 9904
MM1      9901 9902 9903 9901 MHS4XPEN L=1.0U W=239.298U
+ AD=478.596P AS=478.596P PD=482.596U PS=482.596U NRD=0.008 NRS=0.008
MM2      9903 9902 9904 9904 MHS4XNEN L=1.0U W=204.926U
+ AD=409.852P AS=409.852P PD=413.852U PS=413.852U NRD=0.010 NRS=0.010
.ENDS INVDN
* Philips Semiconductors - OUTCKTN
.SUBCKT OUTCKTN  9903 9911 9906 9901 9904 9917
X1Q1  9906 9906 9904 9904 ESDXXXN
M91M1  9901 9903 2 9907 MHS4XPEN L=1.0U W=69.298U
+ AD=138.596P AS=138.596P PD=142.596U PS=142.596U NRD=0.029 NRS=0.029
M91M2  2 49 3 9907 MHS4XPEN L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M91M3  9901 9903 4 9907 MHS4XPEN L=1.0U W=69.298U
+ AD=138.596P AS=138.596P PD=142.596U PS=142.596U NRD=0.029 NRS=0.029
M91M4  4 49 25 9907 MHS4XPEN L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M91M5  3 49 9904 9904 MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M91M6  25 9903 9904 9904 MHS4XNEN L=1.0U W=15.926U
+ AD=31.852P AS=31.852P PD=35.852U PS=35.852U NRD=0.126 NRS=0.126
M91M7  3 9903 9904 9904 MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M91M8  25 49 9904 9904 MHS4XNEN L=1.0U W=15.926U
+ AD=31.852P AS=31.852P PD=35.852U PS=35.852U NRD=0.126 NRS=0.126
M91M9  9901 39 47 9907 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M91M10  47 9901 9906 9907 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
Q91Q1  9901 3 25 DA0ACBSN
X91D1  9906 47 9904 DB3002AN
X91D2  9901 47 9904 DB3002AN
X91D3  9901 47 9904 DB3002AN
R93R1  9901 5 5K
M93M1  5 49 6 9901 MHS4XPEN L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M93M2  6 32 7 9901 MHS4XPEN L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M93M3  7 9 8 9901 MHS4XPEN L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M93M4  9901 9906 10 9901 MHS4XPEN L=1.0U W=11.298U
+ AD=22.596P AS=22.596P PD=26.596U PS=26.596U NRD=0.177 NRS=0.177
M93M5  9901 10 9 9901 MHS4XPEN L=1.0U W=11.298U
+ AD=22.596P AS=22.596P PD=26.596U PS=26.596U NRD=0.177 NRS=0.177
M93M6  8 49 9904 9904 MHS4XNEN L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M93M7  8 32 9904 9904 MHS4XNEN L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M93M8  8 9 9904 9904 MHS4XNEN L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M93M9  10 9906 9904 9904 MHS4XNEN L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M93M10  9 10 9904 9904 MHS4XNEN L=1.0U W=11.926U
+ AD=23.852P AS=23.852P PD=27.852U PS=27.852U NRD=0.168 NRS=0.168
Q93Q1  9901 8 35 DA06CBSN
Q93Q2  8 8 11 DA06CBSN
X93D1  11 9906 9904 DB0308AN
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M96M1  9901 13 12 9901 MHS4XPEN L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M96M2  9901 9911 12 9901 MHS4XPEN L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M96M3  9901 44 12 9901 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M96M4  47 13 26 9907 MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M96M5  47 9911 26 9907 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M96M6  47 44 26 9907 MHS4XPEN L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M96M7  12 13 14 9904 MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M96M8  14 9911 15 9904 MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M96M9  15 44 9904 9904 MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M96M10  26 44 16 9904 MHS4XNEN L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M96M11  16 9911 17 9904 MHS4XNEN L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M96M12  17 13 9904 9904 MHS4XNEN L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
Q96Q1  9901 12 26 DA08CBSN
M97M1  9901 39 18 9901 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M97M2  18 20 19 9901 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M97M3  19 49 21 9901 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M97M4  21 9903 22 9901 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M97M5  9901 26 20 9901 MHS4XPEN L=1.0U W=7.298U
+ AD=14.596P AS=14.596P PD=18.596U PS=18.596U NRD=0.274 NRS=0.274
M97M6  22 39 9904 9904 MHS4XNEN L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M7  22 9903 9904 9904 MHS4XNEN L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M8  23 9903 9904 9904 MHS4XNEN L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M9  22 49 9904 9904 MHS4XNEN L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M10  23 49 9904 9904 MHS4XNEN L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M11  23 39 9904 9904 MHS4XNEN L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M12  20 26 9904 9904 MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
Q97Q1  9901 22 23 DA04AASN
Q97Q2  26 23 9904 DA08CBSN
Q97Q3  22 22 24 DA04AASN
X97D1  24 26 9904 DB0308AN
M9M1  9901 9903 13 9901 MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M9M2  13 9903 9904 9904 MHS4XNEN L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
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M9M3  9901 9903 32 9901 MHS4XPEN L=1.0U W=79.298U
+ AD=158.596P AS=158.596P PD=162.596U PS=162.596U NRD=0.025 NRS=0.025
M9M4  32 9903 9904 9904 MHS4XNEN L=1.0U W=109.926U
+ AD=219.852P AS=219.852P PD=223.852U PS=223.852U NRD=0.018 NRS=0.018
M92M1  9901 26 25 9907 MHS4XPEN L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
M92M2  9901 26 9906 9907 MHS4XPEN L=1.0U W=999.298U
+ AD=1998.596P AS=1998.596P PD=2002.596U PS=2002.596U NRD=0.002 NRS=0.002
X92D1  9901 27 9904 DB3002AN
X92D2  9901 27 9904 DB3002AN
X92D3  9901 27 9904 DB3002AN
X92D4  9901 27 9904 DB3002AN
X92D5  9901 27 9904 DB3002AN
Q92Q1  28 25 9906 DA283ASN
Q92Q2  28 25 9906 DA283ASN
Q92Q3  9906 35 9917 DA283ASN
Q92Q4  9906 35 9917 DA283ASN
Q92Q5  9906 35 9917 DA283ASN
Q92Q6  9906 35 9917 DA283ASN
R92R1  35 9917 10K
R92R2  27 28 5
M9M11  9906 9903 1 9904 MHS4XNEN L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M9M12  1 9911 9917 9904 MHS4XNEN L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M99M1  30 49 29 9901 MHS4XPEN L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M99M2  29 32 31 9901 MHS4XPEN L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M99M5  9901 33 30 9901 MHS4XPEN L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
M99M6  9901 34 30 9901 MHS4XPEN L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M99M7  9901 9906 33 9901 MHS4XPEN L=1.0U W=2.298U
+ AD=4.596P AS=4.596P PD=8.596U PS=8.596U NRD=0.870 NRS=0.870
M99M8  33 9906 9904 9904 MHS4XNEN L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M99M9  35 32 9904 9904 MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M99M10  35 49 9904 9904 MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M99M11  31 32 9904 9904 MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M99M12  31 49 9904 9904 MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
Q99Q1  9901 31 35 DA0ACBSN
X99D1  31 9906 9904 DB0308AN
M99M13  9901 49 36 9901 MHS4XPEN L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M99M14  36 32 34 9901 MHS4XPEN L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M99M15  34 32 9904 9904 MHS4XNEN L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
M99M16  34 49 9904 9904 MHS4XNEN L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
C9C2  9917 9901 1U
C9C3  9917 9901 1U
E910E7  41 42 40 37 0.5
```

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V910V3  42 0   1.25
E910E8  38 0 41 0 3
E910E9  45 0 46 0 1
V910V4  47 46   0.5
E910E10  43 48 38 0 -1
V910V5  48 0   3
V910V6  40 9901   0.3
R910R5  9906 37 5K
M910M1  37 9911 0 9904 MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
R910R8  38 9904 10MEG
M910M11  39 38 9904 9904 MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M910M12  47 38 39 9901 MHS4XPEN L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
R910R10  41 0 10MEG
M910M13  44 43 9904 9904 MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M910M14  9901 43 44 9901 MHS4XPEN L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
X910D4  38 45 9904 DB3002AN
R910R11 46 0 10MEG
M2M1  9901 9911 49 9901 MHS4XPEN L=1.0U W=199.298U
+ AD=398.596P AS=398.596P PD=402.596U PS=402.596U NRD=0.010 NRS=0.010
M2M2  49 9911 9904 9904 MHS4XNEN L=1.0U W=104.926U
+ AD=209.852P AS=209.852P PD=213.852U PS=213.852U NRD=0.019 NRS=0.019
.ENDS OUTCKTN
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LVTFASBS.LIB Subcircuit

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*****************************************************************************
* LVT BERKELEY SPICE SUBCIRCUIT LIBRARY
* LVTFASBS.LIB
* FAST PROCESS CORNER
* STANDARD LOGIC PRODUCT GROUP
* PHILIPS SEMICONDUCTORS
* 4/5/95
*****************************************************************************
.SUBCKT INV1 D E Q VCC
* USE THIS MODEL FOR 74LVT125 - 244
*   D  INTVCC  INTGND
X1  1    99       6                  IN_DF
*   D   INT  INTVCC  INTGND
X2  1    90    99       6          INVBF
*  INT   E   Q   INTVCC  INTGND  INTOGND
X4  90   3   2     99       6       6    OUTCKTF
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1
.SUBCKT INV2 D E Q VCC
* USE THIS MODEL FOR 74LVT273 - 573 - 574
*   D  INTVCC  INTGND
X1  1    99       6                  IN_DF
*   D   INT  INTVCC  INTGND
X2  1    90    99       6          INVAF
*  INT   E   Q   INTVCC  INTGND  INTOGND
X4  90   3   2     99       6       6    OUTCKTF
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV2
.SUBCKT NINV D E Q VCC
* USE THIS MODEL FOR 74LVT240 (ONLY INVERTING PART)
*   D  INTVCC  INTGND
X1  1    99       6                  IN_DF
*   D   INT  INTVCC  INTGND
X2  1    90    99       6          INVBF
*   D   INT  INTVCC  INTGND
X3  90    91    99      6          INVBF
*  INT   E   Q   INTVCC  INTGND  INTOGND
X4  91   3   2     99       6       6    OUTCKTF
*
```

```
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINV
.SUBCKT A2BINV1 D Q VCC
* USE THIS MODEL FOR 74LVT245 - 646
*   D  INTVCC  INTGND
X1  1    99       6                  IN_DF
*   D   INT  INTVCC  INTGND
X2  1    90    99      6          INVDF
*  INT   E   Q  INTVCC  INTGND  INTOGND
X3  90   3   2    99       6       6    OUTCKTF
*   D  INTVCC  INTGND
X4  2    99       6                  IN_DF
*   D   INT  INTVCC  INTGND
X5  2    91    99      6          INVDF
*  INT   E   Q  INTVCC  INTGND  INTOGND
X6  91   8   1    99       6       6    OUTCKTF
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV1
.SUBCKT A2BINV2 D E Q VCC
* USE THIS MODEL FOR 74LVT543
*   D  INTVCC  INTGND
X1  1    99       6                  IN_DF
*   D   INT  INTVCC  INTGND
X2  1    90    99      6          INVCF
*  INT   E   Q   INTVCC  INTGND  INTOGND
X3  90   3   2     99       6       6    OUTCKTF
*   D  INTVCC  INTGND
X4  2    99       6                  IN_DF
*   D   INT  INTVCC  INTGND
X5  2    91    99      6          INVCF
*  INT   E   Q   INTVCC  INTGND  INTOGND
X6  91   8   1     99       6       6    OUTCKTF
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
```

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C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV2
.SUBCKT A2BINV3 D E Q VCC
* USE THIS MODEL FOR 74LVT652 - 2952
*   D  INTVCC  INTGND
X1  1    99       6                  IN_DF
*   D   INT  INTVCC  INTGND
X2  1    90    99       6           INVDF
*  INT   E   Q   INTVCC  INTGND  INTOGND
X3  90   3   2     99       6       6    OUTCKTF
*   D  INTVCC  INTGND
X4  2    99       6                  IN_DF
*   D   INT  INTVCC  INTGND
X5  2    91    99       6           INVDF
*  INT   E   Q   INTVCC  INTGND  INTOGND
X6  91   8   1     99       6       6    OUTCKTF
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV3
* Philips Semiconductors - IN_DF  - Nominal
.SUBCKT IN_DF 9902 9901 9904
X2Q1  9902 9902 9904 9904 ESDXXXF
M1M1  9901 9902 1 9901 MHS4XPEF L=1.0U W=3.298U
+ AD=6.596P AS=6.596P PD=10.596U PS=10.596U NRD=0.606 NRS=0.606
M1M2  9901 1 2 9901 MHS4XPEF L=1.0U W=13.298U
+ AD=26.596P AS=26.596P PD=30.596U PS=30.596U NRD=0.150 NRS=0.150
M1M3  1 9902 9904 9904 MHS4XNEF L=1.0U W=1.926U
+ AD=3.852P AS=3.852P PD=7.852U PS=7.852U NRD=1.038 NRS=1.038
M1M4  9902 1 9904 9904 MHS4XNEF L=1.0U W=1.926U
+ AD=3.852P AS=3.852P PD=7.852U PS=7.852U NRD=1.038 NRS=1.038
Q1Q1  9902 2 2 DA04AASF
.ENDS IN_DF
* Philips Semiconductors - INVAF - Nominal
.SUBCKT INVAF 9902 9903 9901 9904
MM1     9901 9902 9903 9901 MHS4XPEF L=1.0U W=94.298U
+ AD=188.596P AS=188.596P PD=192.596U PS=192.596U NRD=0.021 NRS=0.021
MM2     9903 9902 9904 9904 MHS4XNEF L=1.0U W=33.926U
+ AD=67.852P AS=67.852P PD=71.852U PS=71.852U NRD=0.059 NRS=0.059
.ENDS INVAF
* Philips Semiconductors - INVBF
.SUBCKT INVBF 9902 9903 9901 9904
MM1     9901 9902 9903 9901 MHS4XPEF L=1.0U W=199.298U
+ AD=398.596P AS=398.596P PD=402.596U PS=402.596U NRD=0.010 NRS=0.010
MM2     9903 9902 9904 9904 MHS4XNEF L=1.0U W=104.926U
+ AD=209.852P AS=209.852P PD=213.852U PS=213.852U NRD=0.019 NRS=0.019
.ENDS INVBF
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* Philips Semiconductors - INVCF
.SUBCKT INVCF 9902 9903 9901 9904
MM1      9901 9902 9903 9901 MHS4XPEF L=1.0U W=139.298U
+ AD=278.596P AS=278.596P PD=282.596U PS=282.596U NRD=0.014 NRS=0.014
MM2      9903 9902 9904 9904 MHS4XNEF L=1.0U W=149.926U
+ AD=299.852P AS=299.852P PD=303.852U PS=303.852U NRD=0.013 NRS=0.013
.ENDS INVCF
* Philips Semiconductors - INVDF
.SUBCKT INVDF 9902 9903 9901 9904
MM1      9901 9902 9903 9901 MHS4XPEF L=1.0U W=239.298U
+ AD=478.596P AS=478.596P PD=482.596U PS=482.596U NRD=0.008 NRS=0.008
MM2      9903 9902 9904 9904 MHS4XNEF L=1.0U W=204.926U
+ AD=409.852P AS=409.852P PD=413.852U PS=413.852U NRD=0.010 NRS=0.010
.ENDS INVDF
* Philips Semiconductors - OUTCKTF
.SUBCKT OUTCKTF  9903 9911 9906 9901 9904 9917
X1Q1  9906 9906 9904 9904 ESDXXXXN
M91M1  9901 9903 2 9907 MHS4XPEF L=1.0U W=69.298U
+ AD=138.596P AS=138.596P PD=142.596U PS=142.596U NRD=0.029 NRS=0.029
M91M2  2 49 3 9907 MHS4XPEF L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M91M3  9901 9903 4 9907 MHS4XPEF L=1.0U W=69.298U
+ AD=138.596P AS=138.596P PD=142.596U PS=142.596U NRD=0.029 NRS=0.029
M91M4  4 49 25 9907 MHS4XPEF L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M91M5  3 49 9904 9904 MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M91M6  25 9903 9904 9904 MHS4XNEF L=1.0U W=15.926U
+ AD=31.852P AS=31.852P PD=35.852U PS=35.852U NRD=0.126 NRS=0.126
M91M7  3 9903 9904 9904 MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M91M8  25 49 9904 9904 MHS4XNEF L=1.0U W=15.926U
+ AD=31.852P AS=31.852P PD=35.852U PS=35.852U NRD=0.126 NRS=0.126
M91M9  9901 39 47 9907 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M91M10  47 9901 9906 9907 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
Q91Q1  9901 3 25 DA0ACBSF
X91D1  9906 47 9904 DB3002AF
X91D2  9901 47 9904 DB3002AF
X91D3  9901 47 9904 DB3002AF
R93R1  9901 5 5K
M93M1  5 49 6 9901 MHS4XPEF L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M93M2  6 32 7 9901 MHS4XPEF L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M93M3  7 9 8 9901 MHS4XPEF L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M93M4  9901 9906 10 9901 MHS4XPEF L=1.0U W=11.298U
+ AD=22.596P AS=22.596P PD=26.596U PS=26.596U NRD=0.177 NRS=0.177
M93M5  9901 10 9 9901 MHS4XPEF L=1.0U W=11.298U
+ AD=22.596P AS=22.596P PD=26.596U PS=26.596U NRD=0.177 NRS=0.177
M93M6  8 49 9904 9904 MHS4XNEF L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M93M7  8 32 9904 9904 MHS4XNEF L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M93M8  8 9 9904 9904 MHS4XNEF L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
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M93M9  10 9906 9904 9904 MHS4XNEF L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M93M10  9 10 9904 9904 MHS4XNEF L=1.0U W=11.926U
+ AD=23.852P AS=23.852P PD=27.852U PS=27.852U NRD=0.168 NRS=0.168
Q93Q1  9901 8 35 DA06CBSF
Q93Q2  8 8 11 DA06CBSF
X93D1  11 9906 9904 DB0308AF
M96M1  9901 13 12 9901 MHS4XPEF L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M96M2  9901 9911 12 9901 MHS4XPEF L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M96M3  9901 44 12 9901 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M96M4  47 13 26 9907 MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M96M5  47 9911 26 9907 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M96M6  47 44 26 9907 MHS4XPEF L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M96M7  12 13 14 9904 MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M96M8  14 9911 15 9904 MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M96M9  15 44 9904 9904 MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M96M10  26 44 16 9904 MHS4XNEF L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M96M11  16 9911 17 9904 MHS4XNEF L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M96M12  17 13 9904 9904 MHS4XNEF L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
Q96Q1  9901 12 26 DA08CBSF
M97M1  9901 39 18 9901 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M97M2  18 20 19 9901 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M97M3  19 49 21 9901 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M97M4  21 9903 22 9901 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M97M5  9901 26 20 9901 MHS4XPEF L=1.0U W=7.298U
+ AD=14.596P AS=14.596P PD=18.596U PS=18.596U NRD=0.274 NRS=0.274
M97M6  22 39 9904 9904 MHS4XNEF L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M7  22 9903 9904 9904 MHS4XNEF L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M8  23 9903 9904 9904 MHS4XNEF L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M9  22 49 9904 9904 MHS4XNEF L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M10  23 49 9904 9904 MHS4XNEF L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M11  23 39 9904 9904 MHS4XNEF L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M12  20 26 9904 9904 MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
Q97Q1  9901 22 23 DA04AASF
Q97Q2  26 23 9904 DA08CBSF
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Q97Q3   22 22 24 DA04AASF
X97D1   24 26 9904 DB0308AF
M9M1   9901 9903 13 9901 MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M9M2   13 9903 9904 9904 MHS4XNEF L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
M9M3   9901 9903 32 9901 MHS4XPEF L=1.0U W=79.298U
+ AD=158.596P AS=158.596P PD=162.596U PS=162.596U NRD=0.025 NRS=0.025
M9M4   32 9903 9904 9904 MHS4XNEF L=1.0U W=109.926U
+ AD=219.852P AS=219.852P PD=223.852U PS=223.852U NRD=0.018 NRS=0.018
M92M1   9901 26 25 9907 MHS4XPEF L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
M92M2   9901 26 9906 9907 MHS4XPEF L=1.0U W=999.298U
+ AD=1998.596P AS=1998.596P PD=2002.596U PS=2002.596U NRD=0.002 NRS=0.002
X92D1   9901 27 9904 DB3002AF
X92D2   9901 27 9904 DB3002AF
X92D3   9901 27 9904 DB3002AF
X92D4   9901 27 9904 DB3002AF
X92D5   9901 27 9904 DB3002AF
Q92Q1   28 25 9906 DA283ASF
Q92Q2   28 25 9906 DA283ASF
Q92Q3   9906 35 9917 DA283ASF
Q92Q4   9906 35 9917 DA283ASF
Q92Q5   9906 35 9917 DA283ASF
Q92Q6   9906 35 9917 DA283ASF
R92R1   35 9917 10K
R92R2   27 28 5
M9M11   9906 9903 1 9904 MHS4XNEF L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M9M12   1 9911 9917 9904 MHS4XNEF L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M99M1   30 49 29 9901 MHS4XPEF L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M99M2   29 32 31 9901 MHS4XPEF L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M99M5   9901 33 30 9901 MHS4XPEF L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
M99M6   9901 34 30 9901 MHS4XPEF L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M99M7   9901 9906 33 9901 MHS4XPEF L=1.0U W=2.298U
+ AD=4.596P AS=4.596P PD=8.596U PS=8.596U NRD=0.870 NRS=0.870
M99M8   33 9906 9904 9904 MHS4XNEF L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M99M9   35 32 9904 9904 MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M99M10   35 49 9904 9904 MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M99M11   31 32 9904 9904 MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M99M12   31 49 9904 9904 MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
Q99Q1   9901 31 35 DA0ACBSF
X99D1   31 9906 9904 DB0308AF
M99M13   9901 49 36 9901 MHS4XPEF L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M99M14   36 32 34 9901 MHS4XPEF L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
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M99M15  34 32 9904 9904 MHS4XNEF L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
M99M16  34 49 9904 9904 MHS4XNEF L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
C9C2  9917 9901 1U
C9C3  9917 9901 1U
E910E7  41 42 40 37 0.5
V910V3  42 0   1.25
E910E8  38 0 41 0 3
E910E9  45 0 46 0 1
V910V4  47 46   0.5
E910E10  43 48 38 0 -1
V910V5  48 0   3
V910V6  40 9901   0.3
R910R5  9906 37 5K
M910M1  37 9911 0 9904 MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
R910R8  38 9904 10MEG
M910M11  39 38 9904 9904 MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M910M12  47 38 39 9901 MHS4XPEF L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
R910R10  41 0 10MEG
M910M13  44 43 9904 9904 MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M910M14  9901 43 44 9901 MHS4XPEF L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
X910D4  38 45 9904 DB3002AF
R910R11 46 0 10MEG
M2M1  9901 9911 49 9901 MHS4XPEF L=1.0U W=199.298U
+ AD=398.596P AS=398.596P PD=402.596U PS=402.596U NRD=0.010 NRS=0.010
M2M2  49 9911 9904 9904 MHS4XNEF L=1.0U W=104.926U
+ AD=209.852P AS=209.852P PD=213.852U PS=213.852U NRD=0.019 NRS=0.019
.ENDS OUTCKTF
```

LVTSLOBS.LIB Subcircuit

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*************************************************************************
* LVT BERKELEY SPICE SUBCIRCUIT LIBRARY
* LVTSLOBS.LIB
* SLOW PROCESS CORNER
* STANDARD LOGIC PRODUCT GROUP
* PHILIPS SEMICONDUCTORS
* 4/5/95
*************************************************************************
.SUBCKT INV1 D E Q VCC
* USE THIS MODEL FOR 74LVT125 - 244
*   D  INTVCC  INTGND
X1  1    99       6                  IN_DS
*   D   INT  INTVCC  INTGND
X2  1    90    99      6           INVBS
*  INT   E   Q   INTVCC  INTGND  INTOGND
X4  90   3   2     99       6       6    OUTCKTS
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1
.SUBCKT INV2 D E Q VCC
* USE THIS MODEL FOR 74LVT273 - 573 - 574
*   D  INTVCC  INTGND
X1  1    99       6                  IN_DS
*   D   INT  INTVCC  INTGND
X2  1    90    99      6           INVAS
*  INT   E   Q   INTVCC  INTGND  INTOGND
X4  90   3   2     99       6       6    OUTCKTS
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV2
.SUBCKT NINV D E Q VCC
* USE THIS MODEL FOR 74LVT240 (ONLY INVERTING PART)
*   D  INTVCC  INTGND
X1  1    99       6                  IN_DS
*   D   INT  INTVCC  INTGND
X2  1    90    99      6           INVBS
*   D   INT  INTVCC  INTGND
X3  90    91    99     6           INVBS
*  INT   E   Q   INTVCC  INTGND  INTOGND
X4  91   3   2     99       6       6    OUTCKTS
```

```
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINV
.SUBCKT A2BINV1 D E Q VCC
* USE THIS MODEL FOR 74LVT245 - 646
*   D  INTVCC  INTGND
X1  1    99       6                IN_DS
*   D   INT  INTVCC  INTGND
X2  1    90    99      6          INVDS
*  INT   E   Q  INTVCC  INTGND  INTOGND
X3  90   3   2    99       6       6    OUTCKTS
*   D  INTVCC  INTGND
X4  2    99       6                IN_DS
*   D   INT  INTVCC  INTGND
X5  2    91    99      6          INVDS
*  INT   E   Q  INTVCC  INTGND  INTOGND
X6  91   8   1    99       6       6    OUTCKTS
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV1
.SUBCKT A2BINV2 D E Q VCC
* USE THIS MODEL FOR 74LVT543
*   D  INTVCC  INTGND
X1  1    99       6                IN_DS
*   D   INT  INTVCC  INTGND
X2  1    90    99      6          INVCS
*  INT   E   Q   INTVCC  INTGND  INTOGND
X3  90   3   2     99       6       6    OUTCKTS
*   D  INTVCC  INTGND
X4  2    99       6                IN_DS
*   D   INT  INTVCC  INTGND
X5  2    91    99      6          INVCS
*  INT   E   Q   INTVCC  INTGND  INTOGND
X6  91   8   1     99       6       6    OUTCKTS
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
```

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C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV2
.SUBCKT A2BINV3 D E Q VCC
* USE THIS MODEL FOR 74LVT652 - 2952
*   D  INTVCC  INTGND
X1  1    99       6                IN_DS
*   D   INT  INTVCC  INTGND
X2  1    90    99       6          INVDS
*  INT   E   Q   INTVCC  INTGND  INTOGND
X3  90   3   2     99       6       6    OUTCKTS
*   D  INTVCC  INTGND
X4  2    99       6                IN_DS
*   D   INT  INTVCC  INTGND
X5  2    91    99       6          INVDS
*  INT   E   Q   INTVCC  INTGND  INTOGND
X6  91   8   1     99       6       6    OUTCKTS
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV3

* Philips Semiconductors - IN_DS  - Slow
.SUBCKT IN_DS 9902 9901 9904
X2Q1  9902 9902 9904 9904 ESDXXXXS
M1M1  9901 9902 1 9901 MHS4XPES L=1.0U W=3.298U
+ AD=6.596P AS=6.596P PD=10.596U PS=10.596U NRD=0.606 NRS=0.606
M1M2  9901 1 2 9901 MHS4XPES L=1.0U W=13.298U
+ AD=26.596P AS=26.596P PD=30.596U PS=30.596U NRD=0.150 NRS=0.150
M1M3  1 9902 9904 9904 MHS4XNES L=1.0U W=1.926U
+ AD=3.852P AS=3.852P PD=7.852U PS=7.852U NRD=1.038 NRS=1.038
M1M4  9902 1 9904 9904 MHS4XNES L=1.0U W=1.926U
+ AD=3.852P AS=3.852P PD=7.852U PS=7.852U NRD=1.038 NRS=1.038
Q1Q1  9902 2 2 DA04AASS
.ENDS IN_DS
* Philips Semiconductors - INVAS - Nominal
.SUBCKT INVAS 9902 9903 9901 9904
MM1     9901 9902 9903 9901 MHS4XPES L=1.0U W=94.298U
+ AD=188.596P AS=188.596P PD=192.596U PS=192.596U NRD=0.021 NRS=0.021
MM2     9903 9902 9904 9904 MHS4XNES L=1.0U W=33.926U
+ AD=67.852P AS=67.852P PD=71.852U PS=71.852U NRD=0.059 NRS=0.059
.ENDS INVAS
* Philips Semiconductors - INVBS
.SUBCKT INVBS 9902 9903 9901 9904
MM1     9901 9902 9903 9901 MHS4XPES L=1.0U W=199.298U
+ AD=398.596P AS=398.596P PD=402.596U PS=402.596U NRD=0.010 NRS=0.010
MM2     9903 9902 9904 9904 MHS4XNES L=1.0U W=104.926U
+ AD=209.852P AS=209.852P PD=213.852U PS=213.852U NRD=0.019 NRS=0.019
.ENDS INVBS
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* Philips Semiconductors - INVCS
.SUBCKT INVCS 9902 9903 9901 9904
MM1      9901 9902 9903 9901 MHS4XPES L=1.0U W=139.298U
+ AD=278.596P AS=278.596P PD=282.596U PS=282.596U NRD=0.014 NRS=0.014
MM2      9903 9902 9904 9904 MHS4XNES L=1.0U W=149.926U
+ AD=299.852P AS=299.852P PD=303.852U PS=303.852U NRD=0.013 NRS=0.013
.ENDS INVCS
* Philips Semiconductors - INVDS
.SUBCKT INVDS 9902 9903 9901 9904
MM1      9901 9902 9903 9901 MHS4XPES L=1.0U W=239.298U
+ AD=478.596P AS=478.596P PD=482.596U PS=482.596U NRD=0.008 NRS=0.008
MM2      9903 9902 9904 9904 MHS4XNES L=1.0U W=204.926U
+ AD=409.852P AS=409.852P PD=413.852U PS=413.852U NRD=0.010 NRS=0.010
.ENDS INVDS
* Philips Semiconductors - OUTCKTS
.SUBCKT OUTCKTS  9903 9911 9906 9901 9904 9917
X1Q1   9906 9906 9904 9904 ESDXXXXS
M91M1  9901 9903 2 9907 MHS4XPES L=1.0U W=69.298U
+ AD=138.596P AS=138.596P PD=142.596U PS=142.596U NRD=0.029 NRS=0.029
M91M2  2 49 3 9907 MHS4XPES L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M91M3  9901 9903 4 9907 MHS4XPES L=1.0U W=69.298U
+ AD=138.596P AS=138.596P PD=142.596U PS=142.596U NRD=0.029 NRS=0.029
M91M4  4 49 25 9907 MHS4XPES L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M91M5  3 49 9904 9904 MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M91M6  25 9903 9904 9904 MHS4XNES L=1.0U W=15.926U
+ AD=31.852P AS=31.852P PD=35.852U PS=35.852U NRD=0.126 NRS=0.126
M91M7  3 9903 9904 9904 MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M91M8  25 49 9904 9904 MHS4XNES L=1.0U W=15.926U
+ AD=31.852P AS=31.852P PD=35.852U PS=35.852U NRD=0.126 NRS=0.126
M91M9  9901 39 47 9907 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M91M10  47 9901 9906 9907 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
Q91Q1  9901 3 25 DA0ACBSS
X91D1  9906 47 9904 DB3002AS
X91D2  9901 47 9904 DB3002AS
X91D3  9901 47 9904 DB3002AS
R93R1  9901 5 5K
M93M1  5 49 6 9901 MHS4XPES L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M93M2  6 32 7 9901 MHS4XPES L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M93M3  7 9 8 9901 MHS4XPES L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M93M4  9901 9906 10 9901 MHS4XPES L=1.0U W=11.298U
+ AD=22.596P AS=22.596P PD=26.596U PS=26.596U NRD=0.177 NRS=0.177
M93M5  9901 10 9 9901 MHS4XPES L=1.0U W=11.298U
+ AD=22.596P AS=22.596P PD=26.596U PS=26.596U NRD=0.177 NRS=0.177
M93M6  8 49 9904 9904 MHS4XNES L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M93M7  8 32 9904 9904 MHS4XNES L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M93M8  8 9 9904 9904 MHS4XNES L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
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M93M9  10 9906 9904 9904 MHS4XNES L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M93M10  9 10 9904 9904 MHS4XNES L=1.0U W=11.926U
+ AD=23.852P AS=23.852P PD=27.852U PS=27.852U NRD=0.168 NRS=0.168
Q93Q1  9901 8 35 DA06CBSS
Q93Q2  8 8 11 DA06CBSS
X93D1  11 9906 9904 DB0308AS
M96M1  9901 13 12 9901 MHS4XPES L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M96M2  9901 9911 12 9901 MHS4XPES L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M96M3  9901 44 12 9901 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M96M4  47 13 26 9907 MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M96M5  47 9911 26 9907 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M96M6  47 44 26 9907 MHS4XPES L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M96M7  12 13 14 9904 MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M96M8  14 9911 15 9904 MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M96M9  15 44 9904 9904 MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M96M10  26 44 16 9904 MHS4XNES L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M96M11  16 9911 17 9904 MHS4XNES L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M96M12  17 13 9904 9904 MHS4XNES L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
Q96Q1  9901 12 26 DA08CBSS
M97M1  9901 39 18 9901 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M97M2  18 20 19 9901 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M97M3  19 49 21 9901 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M97M4  21 9903 22 9901 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M97M5  9901 26 20 9901 MHS4XPES L=1.0U W=7.298U
+ AD=14.596P AS=14.596P PD=18.596U PS=18.596U NRD=0.274 NRS=0.274
M97M6  22 39 9904 9904 MHS4XNES L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M7  22 9903 9904 9904 MHS4XNES L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M8  23 9903 9904 9904 MHS4XNES L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M9  22 49 9904 9904 MHS4XNES L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M10  23 49 9904 9904 MHS4XNES L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M11  23 39 9904 9904 MHS4XNES L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M12  20 26 9904 9904 MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
Q97Q1  9901 22 23 DA04AASS
Q97Q2  26 23 9904 DA08CBSS
Q97Q3  22 22 24 DA04AASS
X97D1  24 26 9904 DB0308AS
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M9M1  9901 9903 13 9901 MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M9M2  13 9903 9904 9904 MHS4XNES L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
M9M3  9901 9903 32 9901 MHS4XPES L=1.0U W=79.298U
+ AD=158.596P AS=158.596P PD=162.596U PS=162.596U NRD=0.025 NRS=0.025
M9M4  32 9903 9904 9904 MHS4XNES L=1.0U W=109.926U
+ AD=219.852P AS=219.852P PD=223.852U PS=223.852U NRD=0.018 NRS=0.018
M92M1  9901 26 25 9907 MHS4XPES L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
M92M2  9901 26 9906 9907 MHS4XPES L=1.0U W=999.298U
+ AD=1998.596P AS=1998.596P PD=2002.596U PS=2002.596U NRD=0.002 NRS=0.002
X92D1  9901 27 9904 DB3002AS
X92D2  9901 27 9904 DB3002AS
X92D3  9901 27 9904 DB3002AS
X92D4  9901 27 9904 DB3002AS
X92D5  9901 27 9904 DB3002AS
Q92Q1  28 25 9906 DA283ASS
Q92Q2  28 25 9906 DA283ASS
Q92Q3  9906 35 9917 DA283ASS
Q92Q4  9906 35 9917 DA283ASS
Q92Q5  9906 35 9917 DA283ASS
Q92Q6  9906 35 9917 DA283ASS
R92R1  35 9917 10K
R92R2  27 28 5
M9M11  9906 9903 1 9904 MHS4XNES L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M9M12  1 9911 9917 9904 MHS4XNES L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M99M1  30 49 29 9901 MHS4XPES L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M99M2  29 32 31 9901 MHS4XPES L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M99M5  9901 33 30 9901 MHS4XPES L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
M99M6  9901 34 30 9901 MHS4XPES L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M99M7  9901 9906 33 9901 MHS4XPES L=1.0U W=2.298U
+ AD=4.596P AS=4.596P PD=8.596U PS=8.596U NRD=0.870 NRS=0.870
M99M8  33 9906 9904 9904 MHS4XNES L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M99M9  35 32 9904 9904 MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M99M10  35 49 9904 9904 MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M99M11  31 32 9904 9904 MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M99M12  31 49 9904 9904 MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
Q99Q1  9901 31 35 DA0ACBSS
X99D1  31 9906 9904 DB0308AS
M99M13  9901 49 36 9901 MHS4XPES L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M99M14  36 32 34 9901 MHS4XPES L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M99M15  34 32 9904 9904 MHS4XNES L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
M99M16  34 49 9904 9904 MHS4XNES L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
```

```
C9C2  9917 9901 1U
C9C3  9917 9901 1U
E910E7  41 42 40 37 0.5
V910V3  42 0   1.25
E910E8  38 0 41 0 3
E910E9  45 0 46 0 1
V910V4  47 46   0.5
E910E10  43 48 38 0 -1
V910V5  48 0   3
V910V6  40 9901   0.3
R910R5  9906 37 5K
M910M1  37 9911 0 9904 MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
R910R8  38 9904 10MEG
M910M11  39 38 9904 9904 MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M910M12  47 38 39 9901 MHS4XPES L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
R910R10  41 0 10MEG
M910M13  44 43 9904 9904 MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M910M14  9901 43 44 9901 MHS4XPES L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
X910D4  38 45 9904 DB3002AS
R910R11 46 0 10MEG
M2M1  9901 9911 49 9901 MHS4XPES L=1.0U W=199.298U
+ AD=398.596P AS=398.596P PD=402.596U PS=402.596U NRD=0.010 NRS=0.010
M2M2  49 9911 9904 9904 MHS4XNES L=1.0U W=104.926U
+ AD=209.852P AS=209.852P PD=213.852U PS=213.852U NRD=0.019 NRS=0.019
.ENDS OUTCKTS
```

LVTMOMHS.LIB Subcircuit

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*****************************************************************************
* LVT HSPICE SUBCIRCUIT LIBRARY
* LVTMOMHS.LIB
* NOMINAL PROCESS CORNER
* STANDARD PRODUCT LOGIC GROUP
* PHILIPS SEMICONDUCTORS
* 4/5/95
*****************************************************************************
.SUBCKT INV1 D E Q VCC
* USE THIS MODEL FOR 74LVT125 - 244
*   D  INTVCC  INTGND
X1  1    99       6                  IN_DN
*   D   INT  INTVCC  INTGND
X2  1    90    99      6           INVBN
*  INT   E   Q   INTVCC  INTGND  INTOGND
X4  90   3   2     99       6       6    OUTCKTN
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1
.SUBCKT INV2 D E Q VCC
* USE THIS MODEL FOR 74LVT273 - 573 - 574
*   D  INTVCC  INTGND
X1  1    99       6                  IN_DN
*   D   INT  INTVCC  INTGND
X2  1    90    99      6           INVAN
*  INT   E   Q   INTVCC  INTGND  INTOGND
X4  90   3   2     99       6       6    OUTCKTN
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV2
.SUBCKT NINV D E Q VCC
* USE THIS MODEL FOR 74LVT240 (ONLY INVERTING PART)
*   D  INTVCC  INTGND
X1  1    99       6                  IN_DN
*   D   INT  INTVCC  INTGND
X2  1    90    99      6           INVBN
*   D   INT  INTVCC  INTGND
X3  90   91    99      6           INVBN
*   INT   E   Q   INTVCC  INTGND  INTOGND
X4  91   3   2     99       6       6    OUTCKTN
*
L1 2 Q 5NH
```

```
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINV
.SUBCKT A2BINV1 D E Q VCC
* USE THIS MODEL FOR 74LVT245 - 646
*   D  INTVCC  INTGND
X1  1    99       6                IN_DN
*   D   INT  INTVCC  INTGND
X2  1    90    99      6          INVDN
*  INT   E   Q  INTVCC  INTGND  INTOGND
X3  90   3   2    99       6       6    OUTCKTN
*   D  INTVCC  INTGND
X4  2    99       6                IN_DN
*   D   INT  INTVCC  INTGND
X5  2    91    99      6          INVDN
*  INT   E   Q  INTVCC  INTGND  INTOGND
X6  91   8   1    99       6       6    OUTCKTN
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV1
.SUBCKT A2BINV2 D E Q VCC
* USE THIS MODEL FOR 74LVT543
*   D  INTVCC  INTGND
X1  1    99       6                IN_DN
*   D   INT  INTVCC  INTGND
X2  1    90    99      6          INVCN
*  INT   E   Q   INTVCC  INTGND  INTOGND
X3  90   3   2     99       6       6    OUTCKTN
*   D  INTVCC  INTGND
X4  2    99       6                IN_DN
*   D   INT  INTVCC  INTGND
X5  2    91    99      6          INVCN
*  INT   E   Q   INTVCC  INTGND  INTOGND
X6  91   8   1     99       6       6    OUTCKTN
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV2
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.SUBCKT A2BINV3 D E Q VCC
* USE THIS MODEL FOR 74LVT652 - 2952
*   D  INTVCC  INTGND
X1  1    99       6                IN_DN
*   D   INT  INTVCC  INTGND
X2  1    90    99       6          INVDN
*  INT   E   Q   INTVCC  INTGND  INTOGND
X3  90   3   2     99       6       6    OUTCKTN
*   D  INTVCC  INTGND
X4  2    99       6                IN_DN
*   D   INT  INTVCC  INTGND
X5  2    91    99       6          INVDN
*  INT   E   Q   INTVCC  INTGND  INTOGND
X6  91   8   1     99       6       6    OUTCKTN
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV3
* Philips Semiconductors - IN_D - Nominal
.MACRO IN_DN D INTVCC INTGND
X2Q1  D D INTGND INTGND ESDXXXXN
M1M1  INTVCC D 1 INTVCC MHS4XPEN L=1.0U W=3.298U
+ AD=6.596P AS=6.596P PD=10.596U PS=10.596U NRD=0.606 NRS=0.606
M1M2  INTVCC 1 2 INTVCC MHS4XPEN L=1.0U W=13.298U
+ AD=26.596P AS=26.596P PD=30.596U PS=30.596U NRD=0.150 NRS=0.150
M1M3  1 D INTGND INTGND MHS4XNEN L=1.0U W=1.926U
+ AD=3.852P AS=3.852P PD=7.852U PS=7.852U NRD=1.038 NRS=1.038
M1M4  D 1 INTGND INTGND MHS4XNEN L=1.0U W=1.926U
+ AD=3.852P AS=3.852P PD=7.852U PS=7.852U NRD=1.038 NRS=1.038
Q1Q1  D 2 2 DA04AASN
.EOM IN_DN
* Philips Semiconductors - INVA - Nominal
.MACRO INVAN D INT INTVCC INTGND
MM1     INTVCC D INT INTVCC MHS4XPEN L=1.0U W=94.298U
+ AD=188.596P AS=188.596P PD=192.596U PS=192.596U NRD=0.021 NRS=0.021
MM2     INT D INTGND INTGND MHS4XNEN L=1.0U W=33.926U
+ AD=67.852P AS=67.852P PD=71.852U PS=71.852U NRD=0.059 NRS=0.059
.EOM INVAN
* Philips Semiconductors - INVB - Nominal
.MACRO INVBN D INT INTVCC INTGND
MM1     INTVCC D INT INTVCC MHS4XPEN L=1.0U W=199.298U
+ AD=398.596P AS=398.596P PD=402.596U PS=402.596U NRD=0.010 NRS=0.010
MM2     INT D INTGND INTGND MHS4XNEN L=1.0U W=104.926U
+ AD=209.852P AS=209.852P PD=213.852U PS=213.852U NRD=0.019 NRS=0.019
.EOM INVBN
* Philips Semiconductors - INVC - Nominal
.MACRO INVCN D INT INTVCC INTGND
MM1     INTVCC D INT INTVCC MHS4XPEN L=1.0U W=139.298U
+ AD=278.596P AS=278.596P PD=282.596U PS=282.596U NRD=0.014 NRS=0.014
MM2     INT D INTGND INTGND MHS4XNEN L=1.0U W=149.926U
+ AD=299.852P AS=299.852P PD=303.852U PS=303.852U NRD=0.013 NRS=0.013
.EOM INVCN
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* Philips Semiconductors - INVD - Nominal
.MACRO INVDN D INT INTVCC INTGND
MM1      INTVCC D INT INTVCC MHS4XPEN L=1.0U W=239.298U
+ AD=478.596P AS=478.596P PD=482.596U PS=482.596U NRD=0.008 NRS=0.008
MM2      INT D INTGND INTGND MHS4XNEN L=1.0U W=204.926U
+ AD=409.852P AS=409.852P PD=413.852U PS=413.852U NRD=0.010 NRS=0.010
.EOM INVDN
* Philips Semiconductors - OUTCKT - NOMINAL
.MACRO OUTCKTN INT E Q INTVCC INTGND INTOGND
X1Q1  Q Q INTGND INTGND ESDXXXXN
M91M1  INTVCC INT 2 PWR MHS4XPEN L=1.0U W=69.298U
+ AD=138.596P AS=138.596P PD=142.596U PS=142.596U NRD=0.029 NRS=0.029
M91M2  2 49 3 PWR MHS4XPEN L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M91M3  INTVCC INT 4 PWR MHS4XPEN L=1.0U W=69.298U
+ AD=138.596P AS=138.596P PD=142.596U PS=142.596U NRD=0.029 NRS=0.029
M91M4  4 49 25 PWR MHS4XPEN L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M91M5  3 49 INTGND INTGND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M91M6  25 INT INTGND INTGND MHS4XNEN L=1.0U W=15.926U
+ AD=31.852P AS=31.852P PD=35.852U PS=35.852U NRD=0.126 NRS=0.126
M91M7  3 INT INTGND INTGND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M91M8  25 49 INTGND INTGND MHS4XNEN L=1.0U W=15.926U
+ AD=31.852P AS=31.852P PD=35.852U PS=35.852U NRD=0.126 NRS=0.126
M91M9  INTVCC 39 47 PWR MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M91M10  47 INTVCC Q PWR MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
Q91Q1  INTVCC 3 25 DA0ACBSN
X91D1  Q 47 INTGND DB3002AN
X91D2  INTVCC 47 INTGND DB3002AN
X91D3  INTVCC 47 INTGND DB3002AN
X93R1  INTVCC 5 INTGND DC00600N  RES=5K
M93M1  5 49 6 INTVCC MHS4XPEN L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M93M2  6 32 7 INTVCC MHS4XPEN L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M93M3  7 9 8 INTVCC MHS4XPEN L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M93M4  INTVCC Q 10 INTVCC MHS4XPEN L=1.0U W=11.298U
+ AD=22.596P AS=22.596P PD=26.596U PS=26.596U NRD=0.177 NRS=0.177
M93M5  INTVCC 10 9 INTVCC MHS4XPEN L=1.0U W=11.298U
+ AD=22.596P AS=22.596P PD=26.596U PS=26.596U NRD=0.177 NRS=0.177
M93M6  8 49 INTGND INTGND MHS4XNEN L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M93M7  8 32 INTGND INTGND MHS4XNEN L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M93M8  8 9 INTGND INTGND MHS4XNEN L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M93M9  10 Q INTGND INTGND MHS4XNEN L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M93M10  9 10 INTGND INTGND MHS4XNEN L=1.0U W=11.926U
+ AD=23.852P AS=23.852P PD=27.852U PS=27.852U NRD=0.168 NRS=0.168
Q93Q1  INTVCC 8 35 DA06CBSN
Q93Q2  8 8 11 DA06CBSN
X93D1  11 Q INTGND DB0308AN
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M96M1  INTVCC 13 12 INTVCC MHS4XPEN L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M96M2  INTVCC E 12 INTVCC MHS4XPEN L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M96M3  INTVCC 44 12 INTVCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M96M4  47 13 26 PWR MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M96M5  47 E 26 PWR MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M96M6  47 44 26 PWR MHS4XPEN L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M96M7  12 13 14 INTGND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M96M8  14 E 15 INTGND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M96M9  15 44 INTGND INTGND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M96M10  26 44 16 INTGND MHS4XNEN L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M96M11  16 E 17 INTGND MHS4XNEN L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M96M12  17 13 INTGND INTGND MHS4XNEN L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
Q96Q1  INTVCC 12 26 DA08CBSN
M97M1  INTVCC 39 18 INTVCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M97M2  18 20 19 INTVCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M97M3  19 49 21 INTVCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M97M4  21 INT 22 INTVCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M97M5  INTVCC 26 20 INTVCC MHS4XPEN L=1.0U W=7.298U
+ AD=14.596P AS=14.596P PD=18.596U PS=18.596U NRD=0.274 NRS=0.274
M97M6  22 39 INTGND INTGND MHS4XNEN L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M7  22 INT INTGND INTGND MHS4XNEN L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M8  23 INT INTGND INTGND MHS4XNEN L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M9  22 49 INTGND INTGND MHS4XNEN L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M10  23 49 INTGND INTGND MHS4XNEN L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M11  23 39 INTGND INTGND MHS4XNEN L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M12  20 26 INTGND INTGND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
Q97Q1  INTVCC 22 23 DA04AASN
Q97Q2  26 23 INTGND DA08CBSN
Q97Q3  22 22 24 DA04AASN
X97D1  24 26 INTGND DB0308AN
M9M1  INTVCC INT 13 INTVCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M9M2  13 INT INTGND INTGND MHS4XNEN L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
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M9M3  INTVCC INT 32 INTVCC MHS4XPEN L=1.0U W=79.298U
+ AD=158.596P AS=158.596P PD=162.596U PS=162.596U NRD=0.025 NRS=0.025
M9M4  32 INT INTGND INTGND MHS4XNEN L=1.0U W=109.926U
+ AD=219.852P AS=219.852P PD=223.852U PS=223.852U NRD=0.018 NRS=0.018
M92M1  INTVCC 26 25 PWR MHS4XPEN L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
M92M2  INTVCC 26 Q PWR MHS4XPEN L=1.0U W=999.298U
+ AD=1998.596P AS=1998.596P PD=2002.596U PS=2002.596U NRD=0.002 NRS=0.002
X92D1  INTVCC 27 INTGND DB3002AN
X92D2  INTVCC 27 INTGND DB3002AN
X92D3  INTVCC 27 INTGND DB3002AN
X92D4  INTVCC 27 INTGND DB3002AN
X92D5  INTVCC 27 INTGND DB3002AN
Q92Q1  28 25 Q DA283ASN
Q92Q2  28 25 Q DA283ASN
Q92Q3  Q 35 INTOGND DA283ASN
Q92Q4  Q 35 INTOGND DA283ASN
Q92Q5  Q 35 INTOGND DA283ASN
Q92Q6  Q 35 INTOGND DA283ASN
X92R1  35 INTOGND INTGND DC00600N  RES=10K
X92R2  27 28 INTGND DB01E00N  RES=5
M9M11  Q INT 1 INTGND MHS4XNEN L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M9M12  1 E INTOGND INTGND MHS4XNEN L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M99M1  30 49 29 INTVCC MHS4XPEN L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M99M2  29 32 31 INTVCC MHS4XPEN L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M99M5  INTVCC 33 30 INTVCC MHS4XPEN L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
M99M6  INTVCC 34 30 INTVCC MHS4XPEN L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M99M7  INTVCC Q 33 INTVCC MHS4XPEN L=1.0U W=2.298U
+ AD=4.596P AS=4.596P PD=8.596U PS=8.596U NRD=0.870 NRS=0.870
M99M8  33 Q INTGND INTGND MHS4XNEN L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M99M9  35 32 INTGND INTGND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M99M10  35 49 INTGND INTGND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M99M11  31 32 INTGND INTGND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M99M12  31 49 INTGND INTGND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
Q99Q1  INTVCC 31 35 DA0ACBSN
X99D1  31 Q INTGND DB0308AN
M99M13  INTVCC 49 36 INTVCC MHS4XPEN L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M99M14  36 32 34 INTVCC MHS4XPEN L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M99M15  34 32 INTGND INTGND MHS4XNEN L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
M99M16  34 49 INTGND INTGND MHS4XNEN L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
C9C2  INTOGND INTVCC 1U
C9C3  INTOGND INTVCC 1U
```

```
R910R1  E  0 10MEG
E910E7  41 42 40 37 0.5
V910V3  42 0   1.25
E910E8  38 0 41 0 3
E910E9  45 0 46 0 1
V910V4  47 46   0.5
E910E10  43 48 38 0 -1
V910V5  48 0   3
V910V6  40 INTVCC   0.3
R910R5  Q 37 5K
M910M1  37 E 0 INTGND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
R910R8  38 INTGND 10MEG
M910M11  39 38 INTGND INTGND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M910M12  47 38 39 INTVCC MHS4XPEN L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
R910R10  41 0 10MEG
M910M13  44 43 INTGND INTGND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M910M14  INTVCC 43 44 INTVCC MHS4XPEN L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
X910D4  38 45 INTGND DB3002AN
R910R11  46 0 10MEG
M2M1  INTVCC E 49 INTVCC MHS4XPEN L=1.0U W=199.298U
+ AD=398.596P AS=398.596P PD=402.596U PS=402.596U NRD=0.010 NRS=0.010
M2M2  49 E INTGND INTGND MHS4XNEN L=1.0U W=104.926U
+ AD=209.852P AS=209.852P PD=213.852U PS=213.852U NRD=0.019 NRS=0.019
.EOM OUTCKTN
```

LVTFASHS.LIB Subcircuit

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*****************************************************************************
* LVT HSPICE SUBCIRCUIT LIBRARY
* LVTFASHS.LIB
* FAST PROCESS CORNER
* STANDARD PRODUCT LOGIC GROUP
* PHILIPS SEMICONDUCTORS
* 4/5/95
*****************************************************************************
.SUBCKT INV1 D E Q VCC
* USE THIS MODEL FOR 74LVT125 - 244
*    D   INTVCC   INTGND
X1   1     99        6                    IN_DF
*    D    INT   INTVCC   INTGND
X2   1     90     99       6             INVBF
*   INT    E    Q    INTVCC   INTGND   INTOGND
X4   90    3    2      99        6        6     OUTCKTF
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1
.SUBCKT INV2 D E Q VCC
* USE THIS MODEL FOR 74LVT273 - 573 - 574
*    D   INTVCC   INTGND
X1   1     99        6                    IN_DF
*    D    INT   INTVCC   INTGND
X2   1     90     99        6            INVAF
*   INT    E    Q    INTVCC   INTGND   INTOGND
X4   90    3    2      99        6        6     OUTCKTF
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV2
.SUBCKT NINV D E Q VCC
* USE THIS MODEL FOR 74LVT240 (ONLY INVERTING PART)
*    D   INTVCC   INTGND
X1   1     99        6                    IN_DF
*    D    INT   INTVCC   INTGND
X2   1     90     99        6            INVBF
*    D    INT   INTVCC   INTGND
X3   90     91     99       6            INVBF
*   INT    E    Q    INTVCC   INTGND   INTOGND
X4   91    3    2      99        6        6     OUTCKTF
*
L1 2 Q 5NH
L2 VCC 99 6NH
```

```
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINV
.SUBCKT A2BINV1 D Q VCC
* USE THIS MODEL FOR 74LVT245 - 646
*   D  INTVCC  INTGND
X1  1    99       6                IN_DF
*   D   INT  INTVCC  INTGND
X2  1    90    99       6          INVDF
*  INT   E   Q  INTVCC  INTGND  INTOGND
X3  90   3   2    99       6       6    OUTCKTF
*   D  INTVCC  INTGND
X4  2    99       6                IN_DF
*   D   INT  INTVCC  INTGND
X5  2    91    99       6          INVDF
*  INT   E   Q  INTVCC  INTGND  INTOGND
X6  91   8   1    99       6       6    OUTCKTF
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV1
.SUBCKT A2BINV2 D E Q VCC
* USE THIS MODEL FOR 74LVT543
*   D  INTVCC  INTGND
X1  1    99       6                IN_DF
*   D   INT  INTVCC  INTGND
X2  1    90    99       6          INVCF
*  INT   E    Q   INTVCC  INTGND  INTOGND
X3  90   3    2     99       6       6    OUTCKTF
*   D  INTVCC  INTGND
X4  2    99       6                IN_DF
*   D   INT  INTVCC  INTGND
X5  2    91    99       6          INVCF
*  INT   E   Q  INTVCC  INTGND  INTOGND
X6  91   8   1    99       6       6    OUTCKTF
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV2
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.SUBCKT A2BINV3 D E Q VCC
* USE THIS MODEL FOR 74LVT652 - 2952
*    D   INTVCC   INTGND
X1   1     99         6                    IN_DF
*    D    INT   INTVCC   INTGND
X2   1     90     99         6           INVDF
*   INT    E    Q    INTVCC   INTGND   INTOGND
X3   90    3    2      99         6        6     OUTCKTF
*    D   INTVCC   INTGND
X4   2     99         6                    IN_DF
*    D    INT   INTVCC   INTGND
X5   2     91     99         6           INVDF
*   INT    E    Q    INTVCC   INTGND   INTOGND
X6   91    8    1      99         6        6     OUTCKTF
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV3


* Philips Semiconductors - IN_D - Fast
.MACRO IN_DF D INTVCC INTGND
X2Q1   D D INTGND INTGND ESDXXXF
M1M1   INTVCC D 1 INTVCC MHS4XPEF L=1.0U W=3.298U
+ AD=6.596P AS=6.596P PD=10.596U PS=10.596U NRD=0.606 NRS=0.606
M1M2   INTVCC 1 2 INTVCC MHS4XPEF L=1.0U W=13.298U
+ AD=26.596P AS=26.596P PD=30.596U PS=30.596U NRD=0.150 NRS=0.150
M1M3   1 D INTGND INTGND MHS4XNEF L=1.0U W=1.926U
+ AD=3.852P AS=3.852P PD=7.852U PS=7.852U NRD=1.038 NRS=1.038
M1M4   D 1 INTGND INTGND MHS4XNEF L=1.0U W=1.926U
+ AD=3.852P AS=3.852P PD=7.852U PS=7.852U NRD=1.038 NRS=1.038
Q1Q1   D 2 2 DA04AASF
.EOM IN_DF
* Philips Semiconductors - INVA - Fast
.MACRO INVAF D INT INTVCC INTGND
MM1      INTVCC D INT INTVCC MHS4XPEF L=1.0U W=94.298U
+ AD=188.596P AS=188.596P PD=192.596U PS=192.596U NRD=0.021 NRS=0.021
MM2      INT D INTGND INTGND MHS4XNEF L=1.0U W=33.926U
+ AD=67.852P AS=67.852P PD=71.852U PS=71.852U NRD=0.059 NRS=0.059
.EOM INVAF
* Philips Semiconductors - INVB - Fast
.MACRO INVBF D INT INTVCC INTGND
MM1      INTVCC D INT INTVCC MHS4XPEF L=1.0U W=199.298U
+ AD=398.596P AS=398.596P PD=402.596U PS=402.596U NRD=0.010 NRS=0.010
MM2      INT D INTGND INTGND MHS4XNEF L=1.0U W=104.926U
+ AD=209.852P AS=209.852P PD=213.852U PS=213.852U NRD=0.019 NRS=0.019
.EOM INVBF
* Philips Semiconductors - INVC - Fast
.MACRO INVCF D INT INTVCC INTGND
MM1      INTVCC D INT INTVCC MHS4XPEF L=1.0U W=139.298U
+ AD=278.596P AS=278.596P PD=282.596U PS=282.596U NRD=0.014 NRS=0.014
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MM2      INT D INTGND INTGND MHS4XNEF L=1.0U W=149.926U
+ AD=299.852P AS=299.852P PD=303.852U PS=303.852U NRD=0.013 NRS=0.013
.EOM INVCF
* Philips Semiconductors - INVD - Fast
.MACRO INVDF D INT INTVCC INTGND
MM1      INTVCC D INT INTVCC MHS4XPEF L=1.0U W=239.298U
+ AD=478.596P AS=478.596P PD=482.596U PS=482.596U NRD=0.008 NRS=0.008
MM2      INT D INTGND INTGND MHS4XNEF L=1.0U W=204.926U
+ AD=409.852P AS=409.852P PD=413.852U PS=413.852U NRD=0.010 NRS=0.010
.EOM INVDF
* Philips Semiconductors - OUTCKT - FAST
.MACRO OUTCKTF INT E Q INTVCC INTGND INTOGND
X1Q1  Q Q INTGND INTGND ESDXXXXF
M91M1  INTVCC INT 2 PWR MHS4XPEF L=1.0U W=69.298U
+ AD=138.596P AS=138.596P PD=142.596U PS=142.596U NRD=0.029 NRS=0.029
M91M2  2 49 3 PWR MHS4XPEF L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M91M3  INTVCC INT 4 PWR MHS4XPEF L=1.0U W=69.298U
+ AD=138.596P AS=138.596P PD=142.596U PS=142.596U NRD=0.029 NRS=0.029
M91M4  4 49 25 PWR MHS4XPEF L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M91M5  3 49 INTGND INTGND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M91M6  25 INT INTGND INTGND MHS4XNEF L=1.0U W=15.926U
+ AD=31.852P AS=31.852P PD=35.852U PS=35.852U NRD=0.126 NRS=0.126
M91M7  3 INT INTGND INTGND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M91M8  25 49 INTGND INTGND MHS4XNEF L=1.0U W=15.926U
+ AD=31.852P AS=31.852P PD=35.852U PS=35.852U NRD=0.126 NRS=0.126
M91M9  INTVCC 39 47 PWR MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M91M10  47 INTVCC Q PWR MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
Q91Q1  INTVCC 3 25 DA0ACBSF
X91D1  Q 47 INTGND DB3002AF
X91D2  INTVCC 47 INTGND DB3002AF
X91D3  INTVCC 47 INTGND DB3002AF
X93R1  INTVCC 5 INTGND DC00600F  RES=5K
M93M1  5 49 6 INTVCC MHS4XPEF L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M93M2  6 32 7 INTVCC MHS4XPEF L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M93M3  7 9 8 INTVCC MHS4XPEF L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M93M4  INTVCC Q 10 INTVCC MHS4XPEF L=1.0U W=11.298U
+ AD=22.596P AS=22.596P PD=26.596U PS=26.596U NRD=0.177 NRS=0.177
M93M5  INTVCC 10 9 INTVCC MHS4XPEF L=1.0U W=11.298U
+ AD=22.596P AS=22.596P PD=26.596U PS=26.596U NRD=0.177 NRS=0.177
M93M6  8 49 INTGND INTGND MHS4XNEF L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M93M7  8 32 INTGND INTGND MHS4XNEF L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M93M8  8 9 INTGND INTGND MHS4XNEF L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M93M9  10 Q INTGND INTGND MHS4XNEF L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M93M10  9 10 INTGND INTGND MHS4XNEF L=1.0U W=11.926U
+ AD=23.852P AS=23.852P PD=27.852U PS=27.852U NRD=0.168 NRS=0.168
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Q93Q1  INTVCC 8 35 DA06CBSF
Q93Q2  8 8 11 DA06CBSF
X93D1  11 Q INTGND DB0308AF
M96M1  INTVCC 13 12 INTVCC MHS4XPEF L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M96M2  INTVCC E 12 INTVCC MHS4XPEF L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M96M3  INTVCC 44 12 INTVCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M96M4  47 13 26 PWR MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M96M5  47 E 26 PWR MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M96M6  47 44 26 PWR MHS4XPEF L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M96M7  12 13 14 INTGND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M96M8  14 E 15 INTGND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M96M9  15 44 INTGND INTGND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M96M10  26 44 16 INTGND MHS4XNEF L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M96M11  16 E 17 INTGND MHS4XNEF L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M96M12  17 13 INTGND INTGND MHS4XNEF L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
Q96Q1  INTVCC 12 26 DA08CBSF
M97M1  INTVCC 39 18 INTVCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M97M2  18 20 19 INTVCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M97M3  19 49 21 INTVCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M97M4  21 INT 22 INTVCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M97M5  INTVCC 26 20 INTVCC MHS4XPEF L=1.0U W=7.298U
+ AD=14.596P AS=14.596P PD=18.596U PS=18.596U NRD=0.274 NRS=0.274
M97M6  22 39 INTGND INTGND MHS4XNEF L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M7  22 INT INTGND INTGND MHS4XNEF L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M8  23 INT INTGND INTGND MHS4XNEF L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M9  22 49 INTGND INTGND MHS4XNEF L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M10  23 49 INTGND INTGND MHS4XNEF L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M11  23 39 INTGND INTGND MHS4XNEF L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M12  20 26 INTGND INTGND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
Q97Q1  INTVCC 22 23 DA04AASF
Q97Q2  26 23 INTGND DA08CBSF
Q97Q3  22 22 24 DA04AASF
X97D1  24 26 INTGND DB0308AF
M9M1  INTVCC INT 13 INTVCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
```

```
M9M2  13 INT INTGND INTGND MHS4XNEF L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
M9M3  INTVCC INT 32 INTVCC MHS4XPEF L=1.0U W=79.298U
+ AD=158.596P AS=158.596P PD=162.596U PS=162.596U NRD=0.025 NRS=0.025
M9M4  32 INT INTGND INTGND MHS4XNEF L=1.0U W=109.926U
+ AD=219.852P AS=219.852P PD=223.852U PS=223.852U NRD=0.018 NRS=0.018
M92M1  INTVCC 26 25 PWR MHS4XPEF L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
M92M2  INTVCC 26 Q PWR MHS4XPEF L=1.0U W=999.298U
+ AD=1998.596P AS=1998.596P PD=2002.596U PS=2002.596U NRD=0.002 NRS=0.002
X92D1  INTVCC 27 INTGND DB3002AF
X92D2  INTVCC 27 INTGND DB3002AF
X92D3  INTVCC 27 INTGND DB3002AF
X92D4  INTVCC 27 INTGND DB3002AF
X92D5  INTVCC 27 INTGND DB3002AF
Q92Q1  28 25 Q DA283ASF
Q92Q2  28 25 Q DA283ASF
Q92Q3  Q 35 INTOGND DA283ASF
Q92Q4  Q 35 INTOGND DA283ASF
Q92Q5  Q 35 INTOGND DA283ASF
Q92Q6  Q 35 INTOGND DA283ASF
X92R1  35 INTOGND INTGND DC00600F  RES=10K
X92R2  27 28 INTGND DB01E00F  RES=5
M9M11  Q INT 1 INTGND MHS4XNEF L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M9M12  1 E INTOGND INTGND MHS4XNEF L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M99M1  30 49 29 INTVCC MHS4XPEF L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M99M2  29 32 31 INTVCC MHS4XPEF L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M99M5  INTVCC 33 30 INTVCC MHS4XPEF L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
M99M6  INTVCC 34 30 INTVCC MHS4XPEF L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M99M7  INTVCC Q 33 INTVCC MHS4XPEF L=1.0U W=2.298U
+ AD=4.596P AS=4.596P PD=8.596U PS=8.596U NRD=0.870 NRS=0.870
M99M8  33 Q INTGND INTGND MHS4XNEF L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M99M9  35 32 INTGND INTGND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M99M10  35 49 INTGND INTGND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M99M11  31 32 INTGND INTGND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M99M12  31 49 INTGND INTGND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
Q99Q1  INTVCC 31 35 DA0ACBSF
X99D1  31 Q INTGND DB0308AF
M99M13  INTVCC 49 36 INTVCC MHS4XPEF L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M99M14  36 32 34 INTVCC MHS4XPEF L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M99M15  34 32 INTGND INTGND MHS4XNEF L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
M99M16  34 49 INTGND INTGND MHS4XNEF L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
```

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C9C2  INTOGND INTVCC 1U
C9C3  INTOGND INTVCC 1U
E910E7  41 42 40 37 0.5
V910V3  42 0   1.25
E910E8  38 0 41 0 3
E910E9  45 0 46 0 1
V910V4  47 46   0.5
E910E10  43 48 38 0 -1
V910V5  48 0   3
V910V6  40 INTVCC   0.3
R910R5  Q 37 5K
M910M1  37 E 0 INTGND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
R910R8  38 INTGND 10MEG
M910M11  39 38 INTGND INTGND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M910M12  47 38 39 INTVCC MHS4XPEF L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
R910R10  41 0 10MEG
M910M13  44 43 INTGND INTGND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M910M14  INTVCC 43 44 INTVCC MHS4XPEF L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
X910D4  38 45 INTGND DB3002AF
R910R11  46 0 10MEG
M2M1  INTVCC E 49 INTVCC MHS4XPEF L=1.0U W=199.298U
+ AD=398.596P AS=398.596P PD=402.596U PS=402.596U NRD=0.010 NRS=0.010
M2M2  49 E INTGND INTGND MHS4XNEF L=1.0U W=104.926U
+ AD=209.852P AS=209.852P PD=213.852U PS=213.852U NRD=0.019 NRS=0.019
.EOM OUTCKTF
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LVTSLOHS.LIB Subcircuit

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*****************************************************************************
* LVT HSPICE SUBCIRCUIT LIBRARY
* LVTSLOHS.LIB
* SLOW PROCESS CORNER
* STANDARD PRODUCT LOGIC GROUP
* PHILIPS SEMICONDUCTORS
* 4/5/95
*****************************************************************************
.SUBCKT INV1 D E Q VCC
* USE THIS MODEL FOR 74LVT125 - 244
*    D  INTVCC  INTGND
X1   1     99       6                  IN_DS
*    D   INT  INTVCC  INTGND
X2   1     90     99       6          INVBS
*  INT    E    Q   INTVCC  INTGND  INTOGND
X4   90    3    2     99       6       6    OUTCKTS
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1
.SUBCKT INV2 D E Q VCC
* USE THIS MODEL FOR 74LVT273 - 573 - 574
*    D  INTVCC  INTGND
X1   1     99       6                  IN_DS
*    D   INT  INTVCC  INTGND
X2   1     90     99       6          INVAS
*  INT    E    Q   INTVCC  INTGND  INTOGND
X4   90    3    2     99       6       6    OUTCKTS
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV2
.SUBCKT NINV D E Q VCC
* USE THIS MODEL FOR 74LVT240 (ONLY INVERTING PART)
*    D  INTVCC  INTGND
X1   1     99       6                  IN_DS
*    D   INT  INTVCC  INTGND
X2   1     90     99       6          INVBS
*    D   INT  INTVCC  INTGND
X3   90    91     99       6          INVBS
*  INT    E    Q   INTVCC  INTGND  INTOGND
X4   91    3    2     99       6       6    OUTCKTS
*
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```
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINV
.SUBCKT A2BINV1 D E Q VCC
* USE THIS MODEL FOR 74LVT245 - 646
*   D  INTVCC  INTGND
X1  1    99       6                IN_DS
*   D   INT  INTVCC  INTGND
X2  1    90    99       6          INVDS
*  INT   E   Q  INTVCC  INTGND  INTOGND
X3  90   3   2    99       6       6    OUTCKTS
*   D  INTVCC  INTGND
X4  2    99       6                IN_DS
*   D   INT  INTVCC  INTGND
X5  2    91    99       6          INVDS
*  INT   E   Q  INTVCC  INTGND  INTOGND
X6  91   8   1    99       6       6    OUTCKTS
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV1
.SUBCKT A2BINV2 D E Q VCC
* USE THIS MODEL FOR 74LVT543
*   D  INTVCC  INTGND
X1  1    99       6                IN_DS
*   D   INT  INTVCC  INTGND
X2  1    90    99       6          INVCS
*  INT   E   Q   INTVCC  INTGND  INTOGND
X3  90   3   2    99       6       6    OUTCKTS
*   D  INTVCC  INTGND
X4  2    99       6                IN_DS
*   D   INT  INTVCC  INTGND
X5  2    91    99       6          INVCS
*  INT   E   Q   INTVCC  INTGND  INTOGND
X6  91   8   1    99       6       6    OUTCKTS
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
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C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV2
.SUBCKT A2BINV3 D E Q VCC
* USE THIS MODEL FOR 74LVT652 - 2952
*   D  INTVCC  INTGND
X1  1    99       6                  IN_DS
*   D   INT  INTVCC  INTGND
X2  1    90    99       6          INVDS
*  INT   E   Q   INTVCC  INTGND  INTOGND
X3  90   3   2     99       6       6    OUTCKTS
*   D  INTVCC  INTGND
X4  2    99       6                  IN_DS
*   D   INT  INTVCC  INTGND
X5  2    91    99       6          INVDS
*  INT  E   Q   INTVCC  INTGND  INTOGND
X6  91  8   1     99       6       6    OUTCKTS
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV3

* Philips Semiconductors - IN_D - Slow
.MACRO IN_DS D INTVCC INTGND
X2Q1  D D INTGND INTGND ESDXXXXS
M1M1  INTVCC D 1 INTVCC MHS4XPES L=1.0U W=3.298U
+ AD=6.596P AS=6.596P PD=10.596U PS=10.596U NRD=0.606 NRS=0.606
M1M2  INTVCC 1 2 INTVCC MHS4XPES L=1.0U W=13.298U
+ AD=26.596P AS=26.596P PD=30.596U PS=30.596U NRD=0.150 NRS=0.150
M1M3  1 D INTGND INTGND MHS4XNES L=1.0U W=1.926U
+ AD=3.852P AS=3.852P PD=7.852U PS=7.852U NRD=1.038 NRS=1.038
M1M4  D 1 INTGND INTGND MHS4XNES L=1.0U W=1.926U
+ AD=3.852P AS=3.852P PD=7.852U PS=7.852U NRD=1.038 NRS=1.038
Q1Q1  D 2 2 DA04AASS
.EOM IN_DS
* Philips Semiconductors - INVA - Slow
.MACRO INVAS D INT INTVCC INTGND
MM1     INTVCC D INT INTVCC MHS4XPES L=1.0U W=94.298U
+ AD=188.596P AS=188.596P PD=192.596U PS=192.596U NRD=0.021 NRS=0.021
MM2     INT D INTGND INTGND MHS4XNES L=1.0U W=33.926U
+ AD=67.852P AS=67.852P PD=71.852U PS=71.852U NRD=0.059 NRS=0.059
.EOM INVAS
* Philips Semiconductors - INVB - Slow
.MACRO INVBS D INT INTVCC INTGND
MM1     INTVCC D INT INTVCC MHS4XPES L=1.0U W=199.298U
+ AD=398.596P AS=398.596P PD=402.596U PS=402.596U NRD=0.010 NRS=0.010
MM2     INT D INTGND INTGND MHS4XNES L=1.0U W=104.926U
+ AD=209.852P AS=209.852P PD=213.852U PS=213.852U NRD=0.019 NRS=0.019
.EOM INVBS
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* Philips Semiconductors - INVC - Slow
.MACRO INVCS D INT INTVCC INTGND
MM1      INTVCC D INT INTVCC MHS4XPES L=1.0U W=139.298U
+ AD=278.596P AS=278.596P PD=282.596U PS=282.596U NRD=0.014 NRS=0.014
MM2      INT D INTGND INTGND MHS4XNES L=1.0U W=149.926U
+ AD=299.852P AS=299.852P PD=303.852U PS=303.852U NRD=0.013 NRS=0.013
.EOM INVCS
* Philips Semiconductors - INVD - Slow
.MACRO INVDS D INT INTVCC INTGND
MM1      INTVCC D INT INTVCC MHS4XPES L=1.0U W=239.298U
+ AD=478.596P AS=478.596P PD=482.596U PS=482.596U NRD=0.008 NRS=0.008
MM2      INT D INTGND INTGND MHS4XNES L=1.0U W=204.926U
+ AD=409.852P AS=409.852P PD=413.852U PS=413.852U NRD=0.010 NRS=0.010
.EOM INVDS
* Philips Semiconductors - BOUTCKT - SLOW
.MACRO OUTCKTS INT E Q INTVCC INTGND INTOGND
X1Q1   Q Q INTGND INTGND ESDXXXXS
M91M1   INTVCC INT 2 PWR MHS4XPES L=1.0U W=69.298U
+ AD=138.596P AS=138.596P PD=142.596U PS=142.596U NRD=0.029 NRS=0.029
M91M2   2 49 3 PWR MHS4XPES L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M91M3   INTVCC INT 4 PWR MHS4XPES L=1.0U W=69.298U
+ AD=138.596P AS=138.596P PD=142.596U PS=142.596U NRD=0.029 NRS=0.029
M91M4   4 49 25 PWR MHS4XPES L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M91M5   3 49 INTGND INTGND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M91M6   25 INT INTGND INTGND MHS4XNES L=1.0U W=15.926U
+ AD=31.852P AS=31.852P PD=35.852U PS=35.852U NRD=0.126 NRS=0.126
M91M7   3 INT INTGND INTGND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M91M8   25 49 INTGND INTGND MHS4XNES L=1.0U W=15.926U
+ AD=31.852P AS=31.852P PD=35.852U PS=35.852U NRD=0.126 NRS=0.126
M91M9   INTVCC 39 47 PWR MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M91M10   47 INTVCC Q PWR MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
Q91Q1   INTVCC 3 25 DA0ACBSS
X91D1   Q 47 INTGND DB3002AS
X91D2   INTVCC 47 INTGND DB3002AS
X91D3   INTVCC 47 INTGND DB3002AS
X93R1   INTVCC 5 INTGND DC00600S  RES=5K
M93M1   5 49 6 INTVCC MHS4XPES L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M93M2   6 32 7 INTVCC MHS4XPES L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M93M3   7 9 8 INTVCC MHS4XPES L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M93M4   INTVCC Q 10 INTVCC MHS4XPES L=1.0U W=11.298U
+ AD=22.596P AS=22.596P PD=26.596U PS=26.596U NRD=0.177 NRS=0.177
M93M5   INTVCC 10 9 INTVCC MHS4XPES L=1.0U W=11.298U
+ AD=22.596P AS=22.596P PD=26.596U PS=26.596U NRD=0.177 NRS=0.177
M93M6   8 49 INTGND INTGND MHS4XNES L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M93M7   8 32 INTGND INTGND MHS4XNES L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M93M8   8 9 INTGND INTGND MHS4XNES L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
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M93M9  10 Q INTGND INTGND MHS4XNES L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M93M10  9 10 INTGND INTGND MHS4XNES L=1.0U W=11.926U
+ AD=23.852P AS=23.852P PD=27.852U PS=27.852U NRD=0.168 NRS=0.168
Q93Q1  INTVCC 8 35 DA06CBSS
Q93Q2  8 8 11 DA06CBSS
X93D1  11 Q INTGND DB0308AS
M96M1  INTVCC 13 12 INTVCC MHS4XPES L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M96M2  INTVCC E 12 INTVCC MHS4XPES L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M96M3  INTVCC 44 12 INTVCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M96M4  47 13 26 PWR MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M96M5  47 E 26 PWR MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M96M6  47 44 26 PWR MHS4XPES L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M96M7  12 13 14 INTGND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M96M8  14 E 15 INTGND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M96M9  15 44 INTGND INTGND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M96M10  26 44 16 INTGND MHS4XNES L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M96M11  16 E 17 INTGND MHS4XNES L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M96M12  17 13 INTGND INTGND MHS4XNES L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
Q96Q1  INTVCC 12 26 DA08CBSS
M97M1  INTVCC 39 18 INTVCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M97M2  18 20 19 INTVCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M97M3  19 49 21 INTVCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M97M4  21 INT 22 INTVCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M97M5  INTVCC 26 20 INTVCC MHS4XPES L=1.0U W=7.298U
+ AD=14.596P AS=14.596P PD=18.596U PS=18.596U NRD=0.274 NRS=0.274
M97M6  22 39 INTGND INTGND MHS4XNES L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M7  22 INT INTGND INTGND MHS4XNES L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M8  23 INT INTGND INTGND MHS4XNES L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M9  22 49 INTGND INTGND MHS4XNES L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M10  23 49 INTGND INTGND MHS4XNES L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M11  23 39 INTGND INTGND MHS4XNES L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M97M12  20 26 INTGND INTGND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
Q97Q1  INTVCC 22 23 DA04AASS
Q97Q2  26 23 INTGND DA08CBSS
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Q97Q3  22 22 24 DA04AASS
X97D1  24 26 INTGND DB0308AS
M9M1  INTVCC INT 13 INTVCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M9M2  13 INT INTGND INTGND MHS4XNES L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
M9M3  INTVCC INT 32 INTVCC MHS4XPES L=1.0U W=79.298U
+ AD=158.596P AS=158.596P PD=162.596U PS=162.596U NRD=0.025 NRS=0.025
M9M4  32 INT INTGND INTGND MHS4XNES L=1.0U W=109.926U
+ AD=219.852P AS=219.852P PD=223.852U PS=223.852U NRD=0.018 NRS=0.018
M92M1  INTVCC 26 25 PWR MHS4XPES L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
M92M2  INTVCC 26 Q PWR MHS4XPES L=1.0U W=999.298U
+ AD=1998.596P AS=1998.596P PD=2002.596U PS=2002.596U NRD=0.002 NRS=0.002
X92D1  INTVCC 27 INTGND DB3002AS
X92D2  INTVCC 27 INTGND DB3002AS
X92D3  INTVCC 27 INTGND DB3002AS
X92D4  INTVCC 27 INTGND DB3002AS
X92D5  INTVCC 27 INTGND DB3002AS
Q92Q1  28 25 Q DA283ASS
Q92Q2  28 25 Q DA283ASS
Q92Q3  Q 35 INTOGND DA283ASS
Q92Q4  Q 35 INTOGND DA283ASS
Q92Q5  Q 35 INTOGND DA283ASS
Q92Q6  Q 35 INTOGND DA283ASS
X92R1  35 INTOGND INTGND DC00600S  RES=10K
X92R2  27 28 INTGND DB01E00S  RES=5
M9M11  Q INT 1 INTGND MHS4XNES L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M9M12  1 E INTOGND INTGND MHS4XNES L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M99M1  30 49 29 INTVCC MHS4XPES L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M99M2  29 32 31 INTVCC MHS4XPES L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M99M5  INTVCC 33 30 INTVCC MHS4XPES L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
M99M6  INTVCC 34 30 INTVCC MHS4XPES L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M99M7  INTVCC Q 33 INTVCC MHS4XPES L=1.0U W=2.298U
+ AD=4.596P AS=4.596P PD=8.596U PS=8.596U NRD=0.870 NRS=0.870
M99M8  33 Q INTGND INTGND MHS4XNES L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M99M9  35 32 INTGND INTGND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M99M10  35 49 INTGND INTGND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M99M11  31 32 INTGND INTGND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M99M12  31 49 INTGND INTGND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
Q99Q1  INTVCC 31 35 DA0ACBSS
X99D1  31 Q INTGND DB0308AS
M99M13  INTVCC 49 36 INTVCC MHS4XPES L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M99M14  36 32 34 INTVCC MHS4XPES L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
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M99M15  34 32 INTGND INTGND MHS4XNES L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
M99M16  34 49 INTGND INTGND MHS4XNES L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
C9C2  INTOGND INTVCC 1U
C9C3  INTOGND INTVCC 1U
E910E7  41 42 40 37 0.5
V910V3  42 0   1.25
E910E8  38 0 41 0 3
E910E9  45 0 46 0 1
V910V4  47 46   0.5
E910E10  43 48 38 0 -1
V910V5  48 0   3
V910V6  40 INTVCC   0.3
R910R5  Q 37 5K
M910M1  37 E 0 INTGND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
R910R8  38 INTGND 10MEG
M910M11  39 38 INTGND INTGND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M910M12  47 38 39 INTVCC MHS4XPES L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
R910R10  41 0 10MEG
M910M13  44 43 INTGND INTGND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M910M14  INTVCC 43 44 INTVCC MHS4XPES L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
X910D4  38 45 INTGND DB3002AS
R910R11  46 0 10MEG
M2M1  INTVCC E 49 INTVCC MHS4XPES L=1.0U W=199.298U
+ AD=398.596P AS=398.596P PD=402.596U PS=402.596U NRD=0.010 NRS=0.010
M2M2  49 E INTGND INTGND MHS4XNES L=1.0U W=104.926U
+ AD=209.852P AS=209.852P PD=213.852U PS=213.852U NRD=0.019 NRS=0.019
.EOM OUTCKTS
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LVTNOMPS.LIB Subcircuit

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*****************************************************************************
* LVT PSPICE SUBCIRCUIT LIBRARY
* LVTNOMPS.LIB
* NOMINAL PROCESS CORNER
* STANDARD PRODUCT LOGIC GROUP
* PHILIPS SEMICONDUCTORS
* 4/5/95
*****************************************************************************
.SUBCKT INV1 D E Q VCC
* USE THIS MODEL FOR 74LVT125 - 244
*   D  INT_VCC  INT_GND
X1  1    99       6                    IN_DN
*   D   INT  INT_VCC  INT_GND
X2  1    90    99       6           INVBN
*  INT   E   Q   INT_VCC  INT_GND  INT_OGND
X4  90   3   2     99       6       6    OUTCKTN
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1
.SUBCKT INV2 D E Q VCC
* USE THIS MODEL FOR 74LVT273 - 573 - 574
*   D  INT_VCC  INT_GND
X1  1    99       6                    IN_DN
*   D   INT  INT_VCC  INT_GND
X2  1    90    99       6           INVAN
*  INT   E   Q   INT_VCC  INT_GND  INT_OGND
X4  90   3   2     99       6       6    OUTCKTN
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV2
.SUBCKT NINV D E Q VCC
* USE THIS MODEL FOR 74LVT240 (ONLY INVERTING PART)
*   D  INT_VCC  INT_GND
X1  1    99       6                    IN_DN
*   D   INT  INT_VCC  INT_GND
X2  1    90    99       6           INVBN
*   D   INT  INT_VCC  INT_GND
X3  90    91    99       6           INVBN
*  INT   E   Q   INT_VCC  INT_GND  INT_OGND
X4  91   3   2     99       6       6    OUTCKTN
*
L1 2 Q 5NH
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L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINV
.SUBCKT A2BINV1 D E Q VCC
* USE THIS MODEL FOR 74LVT245 - 646
*    D   INT_VCC   INT_GND
X1   1     99        6                    IN_DN
*    D    INT   INT_VCC   INT_GND
X2   1     90     99        6            INVDN
*   INT    E    Q   INT_VCC   INT_GND   INT_OGND
X3   90    3    2     99        6        6     OUTCKTN
*    D   INT_VCC   INT_GND
X4   2     99        6                    IN_DN
*    D    INT   INT_VCC   INT_GND
X5   2     91     99        6            INVDN
*   INT    E    Q   INT_VCC   INT_GND   INT_OGND
X6   91    8    1     99        6        6     OUTCKTN
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV1
.SUBCKT A2BINV2 D E Q VCC
* USE THIS MODEL FOR 74LVT543
*    D   INT_VCC   INT_GND
X1   1     99        6                    IN_DN
*    D    INT   INT_VCC   INT_GND
X2   1     90     99        6            INVCN
*   INT    E    Q    INT_VCC   INT_GND   INT_OGND
X3   90    3    2      99        6        6     OUTCKTN
*    D   INT_VCC   INT_GND
X4   2     99        6                    IN_DN
*    D    INT   INT_VCC   INT_GND
X5   2     91     99        6            INVCN
*   INT    E    Q    INT_VCC   INT_GND   INT_OGND
X6   91    8    1     99        6        6     OUTCKTN
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV2
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.SUBCKT A2BINV3 D E Q VCC
* USE THIS MODEL FOR 74LVT652 - 2952
*   D  INTVCC  INTGND
X1  1    99       6                  IN_DN
*   D   INT  INTVCC  INTGND
X2  1    90    99       6          INVDN
*  INT   E   Q   INTVCC  INTGND  INTOGND
X3  90   3   2     99       6       6    OUTCKTN
*   D  INTVCC  INTGND
X4  2    99       6                  IN_DN
*   D   INT  INTVCC  INTGND
X5  2    91    99       6          INVDN
*  INT   E   Q   INTVCC  INTGND  INTOGND
X6  91   8   1     99       6       6    OUTCKTN
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV3
* Philips Semiconductors - IN_D
.SUBCKT IN_DN D INT_VCC INT_GND
X_U2_Q1  D D INT_GND [INT_GND] ESDXXXXN
M_U1_M1  INT_VCC D 01 INT_VCC MHS4XPEN L=1.0U W=3.298U
+ AD=6.596P AS=6.596P PD=10.596U PS=10.596U NRD=0.606 NRS=0.606
M_U1_M2  INT_VCC 01 02 INT_VCC MHS4XPEN L=1.0U W=13.298U
+ AD=26.596P AS=26.596P PD=30.596U PS=30.596U NRD=0.150 NRS=0.150
M_U1_M3  01 D INT_GND INT_GND MHS4XNEN L=1.0U W=1.926U
+ AD=3.852P AS=3.852P PD=7.852U PS=7.852U NRD=1.038 NRS=1.038
M_U1_M4  D 01 INT_GND INT_GND MHS4XNEN L=1.0U W=1.926U
+ AD=3.852P AS=3.852P PD=7.852U PS=7.852U NRD=1.038 NRS=1.038
Q_U1_Q1  D 02 02 DA04AASN
.ENDS IN_DN
* Philips Semiconductors - INVA
.SUBCKT INVAN D INT INT_VCC INT_GND
M_M1     INT_VCC D INT INT_VCC MHS4XPEN L=1.0U W=94.298U
+ AD=188.596P AS=188.596P PD=192.596U PS=192.596U NRD=0.021 NRS=0.021
M_M2     INT D INT_GND INT_GND MHS4XNEN L=1.0U W=33.926U
+ AD=67.852P AS=67.852P PD=71.852U PS=71.852U NRD=0.059 NRS=0.059
.ENDS INVAN
* Philips Semiconductors - INVB
.SUBCKT INVBN D INT INT_VCC INT_GND
M_M1     INT_VCC D INT INT_VCC MHS4XPEN L=1.0U W=199.298U
+ AD=398.596P AS=398.596P PD=402.596U PS=402.596U NRD=0.010 NRS=0.010
M_M2     INT D INT_GND INT_GND MHS4XNEN L=1.0U W=104.926U
+ AD=209.852P AS=209.852P PD=213.852U PS=213.852U NRD=0.019 NRS=0.019
.ENDS INVBN
* Philips Semiconductors - INVC
.SUBCKT INVCN D INT INT_VCC INT_GND
M_M1     INT_VCC D INT INT_VCC MHS4XPEN L=1.0U W=139.298U
+ AD=278.596P AS=278.596P PD=282.596U PS=282.596U NRD=0.014 NRS=0.014
M_M2     INT D INT_GND INT_GND MHS4XNEN L=1.0U W=149.926U
+ AD=299.852P AS=299.852P PD=303.852U PS=303.852U NRD=0.013 NRS=0.013
.ENDS INVCN
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* Philips Semiconductors - INVD
.SUBCKT INVDN D INT INT_VCC INT_GND
M_M1      INT_VCC D INT INT_VCC MHS4XPEN L=1.0U W=239.298U
+ AD=478.596P AS=478.596P PD=482.596U PS=482.596U NRD=0.008 NRS=0.008
M_M2      INT D INT_GND INT_GND MHS4XNEN L=1.0U W=204.926U
+ AD=409.852P AS=409.852P PD=413.852U PS=413.852U NRD=0.010 NRS=0.010
.ENDS INVDN
* Philips Semiconductors - OUTCKT
.SUBCKT OUTCKTN INT E Q INT_VCC INT_GND INT_OGND
X_U1_Q1  Q Q INT_GND [INT_GND] ESDXXXXN
M_U9_U1_M1  INT_VCC INT 02 PWR MHS4XPEN L=1.0U W=69.298U
+ AD=138.596P AS=138.596P PD=142.596U PS=142.596U NRD=0.029 NRS=0.029
M_U9_U1_M2  02 49 03 PWR MHS4XPEN L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M_U9_U1_M3  INT_VCC INT 04 PWR MHS4XPEN L=1.0U W=69.298U
+ AD=138.596P AS=138.596P PD=142.596U PS=142.596U NRD=0.029 NRS=0.029
M_U9_U1_M4  04 49 25 PWR MHS4XPEN L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M_U9_U1_M5  03 49 INT_GND INT_GND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_U9_U1_M6  25 INT INT_GND INT_GND MHS4XNEN L=1.0U W=15.926U
+ AD=31.852P AS=31.852P PD=35.852U PS=35.852U NRD=0.126 NRS=0.126
M_U9_U1_M7  03 INT INT_GND INT_GND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_U9_U1_M8  25 49 INT_GND INT_GND MHS4XNEN L=1.0U W=15.926U
+ AD=31.852P AS=31.852P PD=35.852U PS=35.852U NRD=0.126 NRS=0.126
M_U9_U1_M9  INT_VCC 39 47 PWR MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_U9_U1_M10  47 INT_VCC Q PWR MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
Q_U9_U1_Q1  INT_VCC 03 25 DA0ACBSN
X_U9_U1_D1  Q 47 INT_GND DB3002AN
X_U9_U1_D2  INT_VCC 47 INT_GND DB3002AN
X_U9_U1_D3  INT_VCC 47 INT_GND DB3002AN
X_U9_U3_R1  INT_VCC 05 INT_GND DC00600N PARAMS: RES=5K
M_U9_U3_M1  05 49 06 INT_VCC MHS4XPEN L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M_U9_U3_M2  06 32 07 INT_VCC MHS4XPEN L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M_U9_U3_M3  07 09 08 INT_VCC MHS4XPEN L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M_U9_U3_M4  INT_VCC Q 10 INT_VCC MHS4XPEN L=1.0U W=11.298U
+ AD=22.596P AS=22.596P PD=26.596U PS=26.596U NRD=0.177 NRS=0.177
M_U9_U3_M5  INT_VCC 10 09 INT_VCC MHS4XPEN L=1.0U W=11.298U
+ AD=22.596P AS=22.596P PD=26.596U PS=26.596U NRD=0.177 NRS=0.177
M_U9_U3_M6  08 49 INT_GND INT_GND MHS4XNEN L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M_U9_U3_M7  08 32 INT_GND INT_GND MHS4XNEN L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M_U9_U3_M8  08 09 INT_GND INT_GND MHS4XNEN L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M_U9_U3_M9  10 Q INT_GND INT_GND MHS4XNEN L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M_U9_U3_M10  09 10 INT_GND INT_GND MHS4XNEN L=1.0U W=11.926U
+ AD=23.852P AS=23.852P PD=27.852U PS=27.852U NRD=0.168 NRS=0.168
Q_U9_U3_Q1  INT_VCC 08 35 DA06CBSN
Q_U9_U3_Q2  08 08 11 DA06CBSN
X_U9_U3_D1  11 Q INT_GND DB0308AN
```

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M_U9_U6_M1  INT_VCC 13 12 INT_VCC MHS4XPEN L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M_U9_U6_M2  INT_VCC E 12 INT_VCC MHS4XPEN L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M_U9_U6_M3  INT_VCC 44 12 INT_VCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_U9_U6_M4  47 13 26 PWR MHS4XPEN L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_U9_U6_M5  47 E 26 PWR MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_U9_U6_M6  47 44 26 PWR MHS4XPEN L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M_U9_U6_M7  12 13 14 INT_GND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_U9_U6_M8  14 E 15 INT_GND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_U9_U6_M9  15 44 INT_GND INT_GND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_U9_U6_M10  26 44 16 INT_GND MHS4XNEN L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M_U9_U6_M11  16 E 17 INT_GND MHS4XNEN L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M_U9_U6_M12  17 13 INT_GND INT_GND MHS4XNEN L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
Q_U9_U6_Q1  INT_VCC 12 26 DA08CBSN
M_U9_U7_M1  INT_VCC 39 18 INT_VCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_U9_U7_M2  18 20 19 INT_VCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_U9_U7_M3  19 49 21 INT_VCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_U9_U7_M4  21 INT 22 INT_VCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_U9_U7_M5  INT_VCC 26 20 INT_VCC MHS4XPEN L=1.0U W=7.298U
+ AD=14.596P AS=14.596P PD=18.596U PS=18.596U NRD=0.274 NRS=0.274
M_U9_U7_M6  22 39 INT_GND INT_GND MHS4XNEN L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M_U9_U7_M7  22 INT INT_GND INT_GND MHS4XNEN L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M_U9_U7_M8  23 INT INT_GND INT_GND MHS4XNEN L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M_U9_U7_M9  22 49 INT_GND INT_GND MHS4XNEN L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M_U9_U7_M10  23 49 INT_GND INT_GND MHS4XNEN L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M_U9_U7_M11  23 39 INT_GND INT_GND MHS4XNEN L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M_U9_U7_M12  20 26 INT_GND INT_GND MHS4XNEN L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
Q_U9_U7_Q1  INT_VCC 22 23 DA04AASN
Q_U9_U7_Q2  26 23 INT_GND DA08CBSN
Q_U9_U7_Q3  22 22 24 DA04AASN
X_U9_U7_D1  24 26 INT_GND DB0308AN
M_U9_M1  INT_VCC INT 13 INT_VCC MHS4XPEN L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_U9_M2  13 INT INT_GND INT_GND MHS4XNEN L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
```

```
M_U9_M3  INT_VCC INT 32 INT_VCC MHS4XPEN L=1.0U W=79.298U
+ AD=158.596P AS=158.596P PD=162.596U PS=162.596U NRD=0.025 NRS=0.025
M_U9_M4  32 INT INT_GND INT_GND MHS4XNEN L=1.0U W=109.926U
+ AD=219.852P AS=219.852P PD=223.852U PS=223.852U NRD=0.018 NRS=0.018
M_U9_U2_M1  INT_VCC 26 25 PWR MHS4XPEN L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
M_U9_U2_M2  INT_VCC 26 Q PWR MHS4XPEN L=1.0U W=999.298U
+ AD=1998.596P AS=1998.596P PD=2002.596U PS=2002.596U NRD=0.002 NRS=0.002
X_U9_U2_D1  INT_VCC 27 INT_GND DB3002AN
X_U9_U2_D2  INT_VCC 27 INT_GND DB3002AN
X_U9_U2_D3  INT_VCC 27 INT_GND DB3002AN
X_U9_U2_D4  INT_VCC 27 INT_GND DB3002AN
X_U9_U2_D5  INT_VCC 27 INT_GND DB3002AN
Q_U9_U2_Q1  28 25 Q DA283ASN
Q_U9_U2_Q2  28 25 Q DA283ASN
Q_U9_U2_Q3  Q 35 INT_OGND DA283ASN
Q_U9_U2_Q4  Q 35 INT_OGND DA283ASN
Q_U9_U2_Q5  Q 35 INT_OGND DA283ASN
Q_U9_U2_Q6  Q 35 INT_OGND DA283ASN
X_U9_U2_R1  35 INT_OGND INT_GND DC00600N PARAMS: RES=10K
X_U9_U2_R2  27 28 INT_GND DB01E00N PARAMS: RES=5
M_U9_M11  Q INT 01 INT_GND MHS4XNEN L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M_U9_M12  01 E INT_OGND INT_GND MHS4XNEN L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M_U9_U9_M1  30 49 29 INT_VCC MHS4XPEN L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M_U9_U9_M2  29 32 31 INT_VCC MHS4XPEN L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M_U9_U9_M5  INT_VCC 33 30 INT_VCC MHS4XPEN L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
M_U9_U9_M6  INT_VCC 34 30 INT_VCC MHS4XPEN L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M_U9_U9_M7  INT_VCC Q 33 INT_VCC MHS4XPEN L=1.0U W=2.298U
+ AD=4.596P AS=4.596P PD=8.596U PS=8.596U NRD=0.870 NRS=0.870
M_U9_U9_M8  33 Q INT_GND INT_GND MHS4XNEN L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M_U9_U9_M9  35 32 INT_GND INT_GND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_U9_U9_M10  35 49 INT_GND INT_GND MHS4XNEN L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_U9_U9_M11  31 32 INT_GND INT_GND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_U9_U9_M12  31 49 INT_GND INT_GND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
Q_U9_U9_Q1  INT_VCC 31 35 DA0ACBSN
X_U9_U9_D1  31 Q INT_GND DB0308AN
M_U9_U9_M13  INT_VCC 49 36 INT_VCC MHS4XPEN L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M_U9_U9_M14  36 32 34 INT_VCC MHS4XPEN L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M_U9_U9_M15  34 32 INT_GND INT_GND MHS4XNEN L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
M_U9_U9_M16  34 49 INT_GND INT_GND MHS4XNEN L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
C_U9_C2  INT_OGND INT_VCC 1U
C_U9_C3  INT_OGND INT_VCC 1U
R_U9_U10_R5  Q 37 5K
```

```
E_U9_U10_E7  41 42 40 37 0.5
V_U9_U10_V3  42 0   1.25
E_U9_U10_E8  38 0 41 0 30
E_U9_U10_E9  45 0 46 0 1
V_U9_U10_V4  47 46   0.5
E_U9_U10_E10  43 48 38 0 -1
V_U9_U10_V5  48 0   3
V_U9_U10_V6  40 INT_VCC   0.3
R_U9_U10_R12  40 0 10MEG
M_U9_U10_M1  37 E 0 INT_GND MHS4XNEN L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
R_U9_U10_R8  38 INT_GND 10MEG
M_U9_U10_M11  39 38 INT_GND INT_GND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_U9_U10_M12  47 38 39 INT_VCC MHS4XPEN L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
R_U9_U10_R10  41 0 10MEG
M_U9_U10_M13  44 43 INT_GND INT_GND MHS4XNEN L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_U9_U10_M14  INT_VCC 43 44 INT_VCC MHS4XPEN L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
X_U9_U10_D4  38 45 INT_GND DB3002AN
R_U9_U10_R11  46 0 10MEG
M_U2_M1  INT_VCC E 49 INT_VCC MHS4XPEN L=1.0U W=199.298U
+ AD=398.596P AS=398.596P PD=402.596U PS=402.596U NRD=0.010 NRS=0.010
M_U2_M2  49 E INT_GND INT_GND MHS4XNEN L=1.0U W=104.926U
+ AD=209.852P AS=209.852P PD=213.852U PS=213.852U NRD=0.019 NRS=0.019
.ENDS OUTCKTN
```

LVTFASPS.LIB Subcircuit

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*****************************************************************************
* LVT PSPICE SUBCIRCUIT LIBRARY
* LVTFASPS.LIB
* FAST PROCESS CORNER
* STANDARD PRODUCT LOGIC GROUP
* PHILIPS SEMICONDUCTORS
* 4/5/95
*****************************************************************************
.SUBCKT INV1 D E Q VCC
* USE THIS MODEL FOR 74LVT125 - 244
*   D  INT_VCC  INT_GND
X1  1    99       6                  IN_DF
*   D   INT  INT_VCC  INT_GND
X2  1    90    99       6          INVBF
*  INT   E   Q   INT_VCC  INT_GND  INT_OGND
X4  90   3   2     99       6       6    OUTCKTF
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1
.SUBCKT INV2 D E Q VCC
* USE THIS MODEL FOR 74LVT273 - 573 - 574
*   D  INT_VCC  INT_GND
X1  1    99       6                  IN_DF
*   D   INT  INT_VCC  INT_GND
X2  1    90    99       6          INVAF
*  INT   E   Q   INT_VCC  INT_GND  INT_OGND
X4  90   3   2     99       6       6    OUTCKTF
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV2
.SUBCKT NINV D E Q VCC
* USE THIS MODEL FOR 74LVT240 (ONLY INVERTING PART)
*   D  INT_VCC  INT_GND
X1  1    99       6                  IN_DF
*   D   INT  INT_VCC  INT_GND
X2  1    90    99       6          INVBF
*   D   INT  INT_VCC  INT_GND
X3  90   91    99       6          INVBF
*  INT   E   Q   INT_VCC  INT_GND  INT_OGND
X4  91   3   2     99       6       6    OUTCKTF
*
```

```
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINV
.SUBCKT A2BINV1 D E Q VCC
* USE THIS MODEL FOR 74LVT245 - 646
*   D  INT_VCC  INT_GND
X1  1    99       6                IN_DF
*   D   INT  INT_VCC  INT_GND
X2  1    90    99       6          INVDF
*  INT   E   Q  INT_VCC  INT_GND  INT_OGND
X3  90   3   2    99       6       6    OUTCKTF
*   D  INT_VCC  INT_GND
X4  2    99       6                IN_DF
*   D   INT  INT_VCC  INT_GND
X5  2    91    99       6          INVDF
*  INT   E   Q  INT_VCC  INT_GND  INT_OGND
X6  91   8   1    99       6       6    OUTCKTF
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV1
.SUBCKT A2BINV2 D E Q VCC
* USE THIS MODEL FOR 74LVT543
*   D  INT_VCC  INT_GND
X1  1    99       6                IN_DF
*   D   INT  INT_VCC  INT_GND
X2  1    90    99       6          INVCF
*  INT   E   Q   INT_VCC  INT_GND  INT_OGND
X3  90   3   2     99       6       6    OUTCKTF
*   D  INT_VCC  INT_GND
X4  2    99       6                IN_DF
*   D   INT  INT_VCC  INT_GND
X5  2    91    99       6          INVCF
*  INT   E   Q   INT_VCC  INT_GND  INT_OGND
X6  91   8   1     99       6       6    OUTCKTF
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
```

```
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV2
.SUBCKT A2BINV3 D E Q VCC
* USE THIS MODEL FOR 74LVT652 - 2952
*   D  INTVCC  INTGND
X1  1    99       6                  IN_DF
*   D   INT  INTVCC  INTGND
X2  1    90    99      6          INVDF
*  INT   E   Q   INTVCC  INTGND  INTOGND
X3  90   3   2     99       6       6    OUTCKTF
*   D  INTVCC  INTGND
X4  2    99       6                  IN_DF
*   D   INT  INTVCC  INTGND
X5  2    91    99      6          INVDF
*  INT   E   Q   INTVCC  INTGND  INTOGND
X6  91   8   1     99       6       6    OUTCKTF
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV3
* Philips Semiconductors - IN_D
.SUBCKT IN_DF D INT_VCC INT_GND
X_U2_Q1  D D INT_GND [INT_GND] ESDXXXF
M_U1_M1  INT_VCC D 01 INT_VCC MHS4XPEF L=1.0U W=3.298U
+ AD=6.596P AS=6.596P PD=10.596U PS=10.596U NRD=0.606 NRS=0.606
M_U1_M2  INT_VCC 01 02 INT_VCC MHS4XPEF L=1.0U W=13.298U
+ AD=26.596P AS=26.596P PD=30.596U PS=30.596U NRD=0.150 NRS=0.150
M_U1_M3  01 D INT_GND INT_GND MHS4XNEF L=1.0U W=1.926U
+ AD=3.852P AS=3.852P PD=7.852U PS=7.852U NRD=1.038 NRS=1.038
M_U1_M4  D 01 INT_GND INT_GND MHS4XNEF L=1.0U W=1.926U
+ AD=3.852P AS=3.852P PD=7.852U PS=7.852U NRD=1.038 NRS=1.038
Q_U1_Q1  D 02 02 DA04AASF
.ENDS IN_DF
* Philips Semiconductors - INVA
.SUBCKT INVAF D INT INT_VCC INT_GND
M_M1     INT_VCC D INT INT_VCC MHS4XPEF L=1.0U W=94.298U
+ AD=188.596P AS=188.596P PD=192.596U PS=192.596U NRD=0.021 NRS=0.021
M_M2     INT D INT_GND INT_GND MHS4XNEF L=1.0U W=33.926U
+ AD=67.852P AS=67.852P PD=71.852U PS=71.852U NRD=0.059 NRS=0.059
.ENDS INVAF
* Philips Semiconductors - INVB
.SUBCKT INVBF D INT INT_VCC INT_GND
M_M1     INT_VCC D INT INT_VCC MHS4XPEF L=1.0U W=199.298U
+ AD=398.596P AS=398.596P PD=402.596U PS=402.596U NRD=0.010 NRS=0.010
M_M2     INT D INT_GND INT_GND MHS4XNEF L=1.0U W=104.926U
+ AD=209.852P AS=209.852P PD=213.852U PS=213.852U NRD=0.019 NRS=0.019
.ENDS INVBF
```

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* Philips Semiconductors - INVC
.SUBCKT INVCF D INT INT_VCC INT_GND
M_M1      INT_VCC D INT INT_VCC MHS4XPEF L=1.0U W=139.298U
+ AD=278.596P AS=278.596P PD=282.596U PS=282.596U NRD=0.014 NRS=0.014
M_M2      INT D INT_GND INT_GND MHS4XNEF L=1.0U W=149.926U
+ AD=299.852P AS=299.852P PD=303.852U PS=303.852U NRD=0.013 NRS=0.013
.ENDS INVCF
* Philips Semiconductors - INVD
.SUBCKT INVDF D INT INT_VCC INT_GND
M_M1      INT_VCC D INT INT_VCC MHS4XPEF L=1.0U W=239.298U
+ AD=478.596P AS=478.596P PD=482.596U PS=482.596U NRD=0.008 NRS=0.008
M_M2      INT D INT_GND INT_GND MHS4XNEF L=1.0U W=204.926U
+ AD=409.852P AS=409.852P PD=413.852U PS=413.852U NRD=0.010 NRS=0.010
.ENDS INVDF
* Philips Semiconductors - OUTCKT
.SUBCKT OUTCKTF INT E Q INT_VCC INT_GND INT_OGND
X_U1_Q1   Q Q INT_GND [INT_GND] ESDXXXXF
M_U9_U1_M1   INT_VCC INT 02 PWR MHS4XPEF L=1.0U W=69.298U
+ AD=138.596P AS=138.596P PD=142.596U PS=142.596U NRD=0.029 NRS=0.029
M_U9_U1_M2   02 49 03 PWR MHS4XPEF L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M_U9_U1_M3   INT_VCC INT 04 PWR MHS4XPEF L=1.0U W=69.298U
+ AD=138.596P AS=138.596P PD=142.596U PS=142.596U NRD=0.029 NRS=0.029
M_U9_U1_M4   04 49 25 PWR MHS4XPEF L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M_U9_U1_M5   03 49 INT_GND INT_GND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_U9_U1_M6   25 INT INT_GND INT_GND MHS4XNEF L=1.0U W=15.926U
+ AD=31.852P AS=31.852P PD=35.852U PS=35.852U NRD=0.126 NRS=0.126
M_U9_U1_M7   03 INT INT_GND INT_GND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_U9_U1_M8   25 49 INT_GND INT_GND MHS4XNEF L=1.0U W=15.926U
+ AD=31.852P AS=31.852P PD=35.852U PS=35.852U NRD=0.126 NRS=0.126
M_U9_U1_M9   INT_VCC 39 47 PWR MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_U9_U1_M10   47 INT_VCC Q PWR MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
Q_U9_U1_Q1   INT_VCC 03 25 DA0ACBSF
X_U9_U1_D1   Q 47 INT_GND DB3002AF
X_U9_U1_D2   INT_VCC 47 INT_GND DB3002AF
X_U9_U1_D3   INT_VCC 47 INT_GND DB3002AF
X_U9_U3_R1   INT_VCC 05 INT_GND DC00600F PARAMS: RES=5K
M_U9_U3_M1   05 49 06 INT_VCC MHS4XPEF L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M_U9_U3_M2   06 32 07 INT_VCC MHS4XPEF L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M_U9_U3_M3   07 09 08 INT_VCC MHS4XPEF L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M_U9_U3_M4   INT_VCC Q 10 INT_VCC MHS4XPEF L=1.0U W=11.298U
+ AD=22.596P AS=22.596P PD=26.596U PS=26.596U NRD=0.177 NRS=0.177
M_U9_U3_M5   INT_VCC 10 09 INT_VCC MHS4XPEF L=1.0U W=11.298U
+ AD=22.596P AS=22.596P PD=26.596U PS=26.596U NRD=0.177 NRS=0.177
M_U9_U3_M6   08 49 INT_GND INT_GND MHS4XNEF L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M_U9_U3_M7   08 32 INT_GND INT_GND MHS4XNEF L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M_U9_U3_M8   08 09 INT_GND INT_GND MHS4XNEF L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
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M_U9_U3_M9  10 Q INT_GND INT_GND MHS4XNEF L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M_U9_U3_M10  09 10 INT_GND INT_GND MHS4XNEF L=1.0U W=11.926U
+ AD=23.852P AS=23.852P PD=27.852U PS=27.852U NRD=0.168 NRS=0.168
Q_U9_U3_Q1  INT_VCC 08 35 DA06CBSF
Q_U9_U3_Q2  08 08 11 DA06CBSF
X_U9_U3_D1  11 Q INT_GND DB0308AF
M_U9_U6_M1  INT_VCC 13 12 INT_VCC MHS4XPEF L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M_U9_U6_M2  INT_VCC E 12 INT_VCC MHS4XPEF L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M_U9_U6_M3  INT_VCC 44 12 INT_VCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_U9_U6_M4  47 13 26 PWR MHS4XPEF L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_U9_U6_M5  47 E 26 PWR MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_U9_U6_M6  47 44 26 PWR MHS4XPEF L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M_U9_U6_M7  12 13 14 INT_GND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_U9_U6_M8  14 E 15 INT_GND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_U9_U6_M9  15 44 INT_GND INT_GND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_U9_U6_M10  26 44 16 INT_GND MHS4XNEF L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M_U9_U6_M11  16 E 17 INT_GND MHS4XNEF L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M_U9_U6_M12  17 13 INT_GND INT_GND MHS4XNEF L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
Q_U9_U6_Q1  INT_VCC 12 26 DA08CBSF
M_U9_U7_M1  INT_VCC 39 18 INT_VCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_U9_U7_M2  18 20 19 INT_VCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_U9_U7_M3  19 49 21 INT_VCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_U9_U7_M4  21 INT 22 INT_VCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_U9_U7_M5  INT_VCC 26 20 INT_VCC MHS4XPEF L=1.0U W=7.298U
+ AD=14.596P AS=14.596P PD=18.596U PS=18.596U NRD=0.274 NRS=0.274
M_U9_U7_M6  22 39 INT_GND INT_GND MHS4XNEF L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M_U9_U7_M7  22 INT INT_GND INT_GND MHS4XNEF L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M_U9_U7_M8  23 INT INT_GND INT_GND MHS4XNEF L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M_U9_U7_M9  22 49 INT_GND INT_GND MHS4XNEF L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M_U9_U7_M10  23 49 INT_GND INT_GND MHS4XNEF L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M_U9_U7_M11  23 39 INT_GND INT_GND MHS4XNEF L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M_U9_U7_M12  20 26 INT_GND INT_GND MHS4XNEF L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
Q_U9_U7_Q1  INT_VCC 22 23 DA04AASF
Q_U9_U7_Q2  26 23 INT_GND DA08CBSF
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Q_U9_U7_Q3  22 22 24 DA04AASF
X_U9_U7_D1  24 26 INT_GND DB0308AF
M_U9_M1  INT_VCC INT 13 INT_VCC MHS4XPEF L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_U9_M2  13 INT INT_GND INT_GND MHS4XNEF L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
M_U9_M3  INT_VCC INT 32 INT_VCC MHS4XPEF L=1.0U W=79.298U
+ AD=158.596P AS=158.596P PD=162.596U PS=162.596U NRD=0.025 NRS=0.025
M_U9_M4  32 INT INT_GND INT_GND MHS4XNEF L=1.0U W=109.926U
+ AD=219.852P AS=219.852P PD=223.852U PS=223.852U NRD=0.018 NRS=0.018
M_U9_U2_M1  INT_VCC 26 25 PWR MHS4XPEF L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
M_U9_U2_M2  INT_VCC 26 Q PWR MHS4XPEF L=1.0U W=999.298U
+ AD=1998.596P AS=1998.596P PD=2002.596U PS=2002.596U NRD=0.002 NRS=0.002
X_U9_U2_D1  INT_VCC 27 INT_GND DB3002AF
X_U9_U2_D2  INT_VCC 27 INT_GND DB3002AF
X_U9_U2_D3  INT_VCC 27 INT_GND DB3002AF
X_U9_U2_D4  INT_VCC 27 INT_GND DB3002AF
X_U9_U2_D5  INT_VCC 27 INT_GND DB3002AF
Q_U9_U2_Q1  28 25 Q DA283ASF
Q_U9_U2_Q2  28 25 Q DA283ASF
Q_U9_U2_Q3  Q 35 INT_OGND DA283ASF
Q_U9_U2_Q4  Q 35 INT_OGND DA283ASF
Q_U9_U2_Q5  Q 35 INT_OGND DA283ASF
Q_U9_U2_Q6  Q 35 INT_OGND DA283ASF
X_U9_U2_R1  35 INT_OGND INT_GND DC00600F PARAMS: RES=10K
X_U9_U2_R2  27 28 INT_GND DB01E00F PARAMS: RES=5
M_U9_M11  Q INT 01 INT_GND MHS4XNEF L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M_U9_M12  01 E INT_OGND INT_GND MHS4XNEF L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M_U9_U9_M1  30 49 29 INT_VCC MHS4XPEF L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M_U9_U9_M2  29 32 31 INT_VCC MHS4XPEF L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M_U9_U9_M5  INT_VCC 33 30 INT_VCC MHS4XPEF L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
M_U9_U9_M6  INT_VCC 34 30 INT_VCC MHS4XPEF L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M_U9_U9_M7  INT_VCC Q 33 INT_VCC MHS4XPEF L=1.0U W=2.298U
+ AD=4.596P AS=4.596P PD=8.596U PS=8.596U NRD=0.870 NRS=0.870
M_U9_U9_M8  33 Q INT_GND INT_GND MHS4XNEF L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M_U9_U9_M9  35 32 INT_GND INT_GND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_U9_U9_M10  35 49 INT_GND INT_GND MHS4XNEF L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_U9_U9_M11  31 32 INT_GND INT_GND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_U9_U9_M12  31 49 INT_GND INT_GND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
Q_U9_U9_Q1  INT_VCC 31 35 DA0ACBSF
X_U9_U9_D1  31 Q INT_GND DB0308AF
M_U9_U9_M13  INT_VCC 49 36 INT_VCC MHS4XPEF L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M_U9_U9_M14  36 32 34 INT_VCC MHS4XPEF L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
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M_U9_U9_M15  34 32 INT_GND INT_GND MHS4XNEF L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
M_U9_U9_M16  34 49 INT_GND INT_GND MHS4XNEF L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
C_U9_C2  INT_OGND INT_VCC 1U
C_U9_C3  INT_OGND INT_VCC 1U
R_U9_U10_R5  Q 37 5K
E_U9_U10_E7  41 42 40 37 0.5
V_U9_U10_V3  42 0   1.25
E_U9_U10_E8  38 0 41 0 30
E_U9_U10_E9  45 0 46 0 1
V_U9_U10_V4  47 46   0.5
E_U9_U10_E10  43 48 38 0 -1
V_U9_U10_V5  48 0   3
V_U9_U10_V6  40 INT_VCC   0.3
R_U9_U10_R12  40 0 10MEG
M_U9_U10_M1  37 E 0 INT_GND MHS4XNEF L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
R_U9_U10_R8  38 INT_GND 10MEG
M_U9_U10_M11  39 38 INT_GND INT_GND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_U9_U10_M12  47 38 39 INT_VCC MHS4XPEF L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
R_U9_U10_R10  41 0 10MEG
M_U9_U10_M13  44 43 INT_GND INT_GND MHS4XNEF L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_U9_U10_M14  INT_VCC 43 44 INT_VCC MHS4XPEF L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
X_U9_U10_D4  38 45 INT_GND DB3002AF
R_U9_U10_R11  46 0 10MEG
M_U2_M1  INT_VCC E 49 INT_VCC MHS4XPEF L=1.0U W=199.298U
+ AD=398.596P AS=398.596P PD=402.596U PS=402.596U NRD=0.010 NRS=0.010
M_U2_M2  49 E INT_GND INT_GND MHS4XNEF L=1.0U W=104.926U
+ AD=209.852P AS=209.852P PD=213.852U PS=213.852U NRD=0.019 NRS=0.019
.ENDS OUTCKTF
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LVTSLOPS.LIB Subcircuit

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*****************************************************************************
* LVT PSPICE SUBCIRCUIT LIBRARY
* LVTSLOPS.LIB
* SLOW PROCESS CORNER
* STANDARD PRODUCT LOGIC GROUP
* PHILIPS SEMICONDUCTORS
* 4/5/95
*****************************************************************************
.SUBCKT INV1 D E Q VCC
* USE THIS MODEL FOR 74LVT125 - 244
*    D   INT_VCC   INT_GND
X1   1     99        6                    IN_DS
*    D    INT   INT_VCC   INT_GND
X2   1     90     99        6           INVBS
*   INT    E    Q    INT_VCC   INT_GND   INT_OGND
X4   90    3    2      99        6        6     OUTCKTS
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV1
.SUBCKT INV2 D E Q VCC
* USE THIS MODEL FOR 74LVT273 - 573 - 574
*    D   INT_VCC   INT_GND
X1   1     99        6                    IN_DS
*    D    INT   INT_VCC   INT_GND
X2   1     90     99        6           INVAS
*   INT    E    Q    INT_VCC   INT_GND   INT_OGND
X4   90    3    2      99        6        6     OUTCKTS
*
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS INV2
.SUBCKT NINV D E Q VCC
* USE THIS MODEL FOR 74LVT240 (ONLY INVERTING PART)
*    D   INT_VCC   INT_GND
X1   1     99        6                    IN_DS
*    D    INT   INT_VCC   INT_GND
X2   1     90     99        6           INVBS
*    D    INT   INT_VCC   INT_GND
X3   90     91     99        6           INVBS
*   INT    E    Q    INT_VCC   INT_GND   INT_OGND
X4   91    3    2      99        6        6     OUTCKTS
*
L1 2 Q 5NH
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L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS NINV
.SUBCKT A2BINV1 D E Q VCC
* USE THIS MODEL FOR 74LVT245 - 646
*    D   INT_VCC   INT_GND
X1   1     99        6                    IN_DS
*    D    INT   INT_VCC   INT_GND
X2   1     90     99        6           INVDS
*   INT    E    Q   INT_VCC   INT_GND   INT_OGND
X3   90    3    2     99        6        6     OUTCKTS
*    D   INT_VCC   INT_GND
X4   2     99        6                    IN_DS
*    D    INT   INT_VCC   INT_GND
X5   2     91     99        6           INVDS
*   INT    E    Q   INT_VCC   INT_GND   INT_OGND
X6   91    8    1     99        6        6     OUTCKTS
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV1
.SUBCKT A2BINV2 D E Q VCC
* USE THIS MODEL FOR 74LVT543
*    D   INT_VCC   INT_GND
X1   1     99        6                    IN_DS
*    D    INT   INT_VCC   INT_GND
X2   1     90     99        6           INVCS
*   INT    E    Q    INT_VCC   INT_GND   INT_OGND
X3   90    3    2      99        6        6     OUTCKTS
*    D   INT_VCC   INT_GND
X4   2     99        6                    IN_DS
*    D    INT   INT_VCC   INT_GND
X5   2     91     99        6           INVCS
*   INT    E    Q    INT_VCC   INT_GND   INT_OGND
X6   91    8    1      99        6        6     OUTCKTS
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV2
```

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.SUBCKT A2BINV3 D E Q VCC
* USE THIS MODEL FOR 74LVT652 - 2952
*   D  INTVCC  INTGND
X1  1    99       6                  IN_DS
*   D   INT  INTVCC  INTGND
X2  1    90    99       6          INVDS
*  INT   E   Q   INTVCC  INTGND  INTOGND
X3  90   3   2     99       6       6    OUTCKTS
*   D  INTVCC  INTGND
X4  2    99       6                  IN_DS
*   D   INT  INTVCC  INTGND
X5  2    91    99       6          INVDS
*  INT   E   Q   INTVCC  INTGND  INTOGND
X6  91   8   1     99       6       6    OUTCKTS
VOE1 8 0 0.0
L1 2 Q 5NH
L2 VCC 99 6NH
L3 0 6 6NH
L4 D 1 6NH
L5 E 3 6NH
C1 2 0 1.5PF
C2 99 0 1.5PF
C3 6 0 1.5PF
C4 1 0 1.5PF
C5 3 0 1.5PF
.ENDS A2BINV3
* Philips Semiconductors - IN_D
.SUBCKT IN_DS D INT_VCC INT_GND
X_U2_Q1  D D INT_GND [INT_GND] ESDXXXS
M_U1_M1  INT_VCC D 01 INT_VCC MHS4XPES L=1.0U W=3.298U
+ AD=6.596P AS=6.596P PD=10.596U PS=10.596U NRD=0.606 NRS=0.606
M_U1_M2  INT_VCC 01 02 INT_VCC MHS4XPES L=1.0U W=13.298U
+ AD=26.596P AS=26.596P PD=30.596U PS=30.596U NRD=0.150 NRS=0.150
M_U1_M3  01 D INT_GND INT_GND MHS4XNES L=1.0U W=1.926U
+ AD=3.852P AS=3.852P PD=7.852U PS=7.852U NRD=1.038 NRS=1.038
M_U1_M4  D 01 INT_GND INT_GND MHS4XNES L=1.0U W=1.926U
+ AD=3.852P AS=3.852P PD=7.852U PS=7.852U NRD=1.038 NRS=1.038
Q_U1_Q1  D 02 02 DA04AASS
.ENDS IN_DS
* Philips Semiconductors - INVA
.SUBCKT INVAS D INT INT_VCC INT_GND
M_M1     INT_VCC D INT INT_VCC MHS4XPES L=1.0U W=94.298U
+ AD=188.596P AS=188.596P PD=192.596U PS=192.596U NRD=0.021 NRS=0.021
M_M2     INT D INT_GND INT_GND MHS4XNES L=1.0U W=33.926U
+ AD=67.852P AS=67.852P PD=71.852U PS=71.852U NRD=0.059 NRS=0.059
.ENDS INVAS
* Philips Semiconductors - INVB
.SUBCKT INVBS D INT INT_VCC INT_GND
M_M1     INT_VCC D INT INT_VCC MHS4XPES L=1.0U W=199.298U
+ AD=398.596P AS=398.596P PD=402.596U PS=402.596U NRD=0.010 NRS=0.010
M_M2     INT D INT_GND INT_GND MHS4XNES L=1.0U W=104.926U
+ AD=209.852P AS=209.852P PD=213.852U PS=213.852U NRD=0.019 NRS=0.019
.ENDS INVBS
* Philips Semiconductors - INVC
.SUBCKT INVCS D INT INT_VCC INT_GND
M_M1     INT_VCC D INT INT_VCC MHS4XPES L=1.0U W=139.298U
+ AD=278.596P AS=278.596P PD=282.596U PS=282.596U NRD=0.014 NRS=0.014
M_M2     INT D INT_GND INT_GND MHS4XNES L=1.0U W=149.926U
+ AD=299.852P AS=299.852P PD=303.852U PS=303.852U NRD=0.013 NRS=0.013
.ENDS INVCS
```

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* Philips Semiconductors - INVD
.SUBCKT INVDS D INT INT_VCC INT_GND
M_M1      INT_VCC D INT INT_VCC MHS4XPES L=1.0U W=239.298U
+ AD=478.596P AS=478.596P PD=482.596U PS=482.596U NRD=0.008 NRS=0.008
M_M2      INT D INT_GND INT_GND MHS4XNES L=1.0U W=204.926U
+ AD=409.852P AS=409.852P PD=413.852U PS=413.852U NRD=0.010 NRS=0.010
.ENDS INVDS
* Philips Semiconductors - OUTCKT
.SUBCKT OUTCKTS INT E Q INT_VCC INT_GND INT_OGND
X_U1_Q1  Q Q INT_GND [INT_GND] ESDXXXS
M_U9_U1_M1  INT_VCC INT 02 PWR MHS4XPES L=1.0U W=69.298U
+ AD=138.596P AS=138.596P PD=142.596U PS=142.596U NRD=0.029 NRS=0.029
M_U9_U1_M2  02 49 03 PWR MHS4XPES L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M_U9_U1_M3  INT_VCC INT 04 PWR MHS4XPES L=1.0U W=69.298U
+ AD=138.596P AS=138.596P PD=142.596U PS=142.596U NRD=0.029 NRS=0.029
M_U9_U1_M4  04 49 25 PWR MHS4XPES L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M_U9_U1_M5  03 49 INT_GND INT_GND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_U9_U1_M6  25 INT INT_GND INT_GND MHS4XNES L=1.0U W=15.926U
+ AD=31.852P AS=31.852P PD=35.852U PS=35.852U NRD=0.126 NRS=0.126
M_U9_U1_M7  03 INT INT_GND INT_GND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_U9_U1_M8  25 49 INT_GND INT_GND MHS4XNES L=1.0U W=15.926U
+ AD=31.852P AS=31.852P PD=35.852U PS=35.852U NRD=0.126 NRS=0.126
M_U9_U1_M9  INT_VCC 39 47 PWR MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_U9_U1_M10  47 INT_VCC Q PWR MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
Q_U9_U1_Q1  INT_VCC 03 25 DA0ACBSS
X_U9_U1_D1  Q 47 INT_GND DB3002AS
X_U9_U1_D2  INT_VCC 47 INT_GND DB3002AS
X_U9_U1_D3  INT_VCC 47 INT_GND DB3002AS
X_U9_U3_R1  INT_VCC 05 INT_GND DC00600F PARAMS: RES=5K
M_U9_U3_M1  05 49 06 INT_VCC MHS4XPES L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M_U9_U3_M2  06 32 07 INT_VCC MHS4XPES L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M_U9_U3_M3  07 09 08 INT_VCC MHS4XPES L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M_U9_U3_M4  INT_VCC Q 10 INT_VCC MHS4XPES L=1.0U W=11.298U
+ AD=22.596P AS=22.596P PD=26.596U PS=26.596U NRD=0.177 NRS=0.177
M_U9_U3_M5  INT_VCC 10 09 INT_VCC MHS4XPES L=1.0U W=11.298U
+ AD=22.596P AS=22.596P PD=26.596U PS=26.596U NRD=0.177 NRS=0.177
M_U9_U3_M6  08 49 INT_GND INT_GND MHS4XNES L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M_U9_U3_M7  08 32 INT_GND INT_GND MHS4XNES L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M_U9_U3_M8  08 09 INT_GND INT_GND MHS4XNES L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M_U9_U3_M9  10 Q INT_GND INT_GND MHS4XNES L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M_U9_U3_M10  09 10 INT_GND INT_GND MHS4XNES L=1.0U W=11.926U
+ AD=23.852P AS=23.852P PD=27.852U PS=27.852U NRD=0.168 NRS=0.168
Q_U9_U3_Q1  INT_VCC 08 35 DA06CBSS
Q_U9_U3_Q2  08 08 11 DA06CBSS
X_U9_U3_D1  11 Q INT_GND DB0308AS
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M_U9_U6_M1  INT_VCC 13 12 INT_VCC MHS4XPES L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M_U9_U6_M2  INT_VCC E 12 INT_VCC MHS4XPES L=1.0U W=29.298U
+ AD=58.596P AS=58.596P PD=62.596U PS=62.596U NRD=0.068 NRS=0.068
M_U9_U6_M3  INT_VCC 44 12 INT_VCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_U9_U6_M4  47 13 26 PWR MHS4XPES L=1.0U W=39.298U
+ AD=78.596P AS=78.596P PD=82.596U PS=82.596U NRD=0.051 NRS=0.051
M_U9_U6_M5  47 E 26 PWR MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_U9_U6_M6  47 44 26 PWR MHS4XPES L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M_U9_U6_M7  12 13 14 INT_GND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_U9_U6_M8  14 E 15 INT_GND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_U9_U6_M9  15 44 INT_GND INT_GND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_U9_U6_M10  26 44 16 INT_GND MHS4XNES L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M_U9_U6_M11  16 E 17 INT_GND MHS4XNES L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
M_U9_U6_M12  17 13 INT_GND INT_GND MHS4XNES L=1.0U W=7.926U
+ AD=15.852P AS=15.852P PD=19.852U PS=19.852U NRD=0.252 NRS=0.252
Q_U9_U6_Q1  INT_VCC 12 26 DA08CBSS
M_U9_U7_M1  INT_VCC 39 18 INT_VCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_U9_U7_M2  18 20 19 INT_VCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_U9_U7_M3  19 49 21 INT_VCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_U9_U7_M4  21 INT 22 INT_VCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_U9_U7_M5  INT_VCC 26 20 INT_VCC MHS4XPES L=1.0U W=7.298U
+ AD=14.596P AS=14.596P PD=18.596U PS=18.596U NRD=0.274 NRS=0.274
M_U9_U7_M6  22 39 INT_GND INT_GND MHS4XNES L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M_U9_U7_M7  22 INT INT_GND INT_GND MHS4XNES L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M_U9_U7_M8  23 INT INT_GND INT_GND MHS4XNES L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M_U9_U7_M9  22 49 INT_GND INT_GND MHS4XNES L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M_U9_U7_M10  23 49 INT_GND INT_GND MHS4XNES L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M_U9_U7_M11  23 39 INT_GND INT_GND MHS4XNES L=1.0U W=5.926U
+ AD=11.852P AS=11.852P PD=15.852U PS=15.852U NRD=0.337 NRS=0.337
M_U9_U7_M12  20 26 INT_GND INT_GND MHS4XNES L=1.0U W=19.926U
+ AD=39.852P AS=39.852P PD=43.852U PS=43.852U NRD=0.100 NRS=0.100
Q_U9_U7_Q1  INT_VCC 22 23 DA04AASS
Q_U9_U7_Q2  26 23 INT_GND DA08CBSS
Q_U9_U7_Q3  22 22 24 DA04AASS
X_U9_U7_D1  24 26 INT_GND DB0308AS
M_U9_M1  INT_VCC INT 13 INT_VCC MHS4XPES L=1.0U W=19.298U
+ AD=38.596P AS=38.596P PD=42.596U PS=42.596U NRD=0.104 NRS=0.104
M_U9_M2  13 INT INT_GND INT_GND MHS4XNES L=1.0U W=34.926U
+ AD=69.852P AS=69.852P PD=73.852U PS=73.852U NRD=0.057 NRS=0.057
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M_U9_M3  INT_VCC INT 32 INT_VCC MHS4XPES L=1.0U W=79.298U
+ AD=158.596P AS=158.596P PD=162.596U PS=162.596U NRD=0.025 NRS=0.025
M_U9_M4  32 INT INT_GND INT_GND MHS4XNES L=1.0U W=109.926U
+ AD=219.852P AS=219.852P PD=223.852U PS=223.852U NRD=0.018 NRS=0.018
M_U9_U2_M1  INT_VCC 26 25 PWR MHS4XPES L=1.0U W=99.298U
+ AD=198.596P AS=198.596P PD=202.596U PS=202.596U NRD=0.020 NRS=0.020
M_U9_U2_M2  INT_VCC 26 Q PWR MHS4XPES L=1.0U W=999.298U
+ AD=1998.596P AS=1998.596P PD=2002.596U PS=2002.596U NRD=0.002 NRS=0.002
X_U9_U2_D1  INT_VCC 27 INT_GND DB3002AS
X_U9_U2_D2  INT_VCC 27 INT_GND DB3002AS
X_U9_U2_D3  INT_VCC 27 INT_GND DB3002AS
X_U9_U2_D4  INT_VCC 27 INT_GND DB3002AS
X_U9_U2_D5  INT_VCC 27 INT_GND DB3002AS
Q_U9_U2_Q1  28 25 Q DA283ASS
Q_U9_U2_Q2  28 25 Q DA283ASS
Q_U9_U2_Q3  Q 35 INT_OGND DA283ASS
Q_U9_U2_Q4  Q 35 INT_OGND DA283ASS
Q_U9_U2_Q5  Q 35 INT_OGND DA283ASS
Q_U9_U2_Q6  Q 35 INT_OGND DA283ASS
X_U9_U2_R1  35 INT_OGND INT_GND DC00600S PARAMS: RES=10K
X_U9_U2_R2  27 28 INT_GND DB01E00S PARAMS: RES=5
M_U9_M11  Q INT 01 INT_GND MHS4XNES L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M_U9_M12  01 E INT_OGND INT_GND MHS4XNES L=1.0U W=49.926U
+ AD=99.852P AS=99.852P PD=103.852U PS=103.852U NRD=0.040 NRS=0.040
M_U9_U9_M1  30 49 29 INT_VCC MHS4XPES L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M_U9_U9_M2  29 32 31 INT_VCC MHS4XPES L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M_U9_U9_M5  INT_VCC 33 30 INT_VCC MHS4XPES L=1.0U W=4.298U
+ AD=8.596P AS=8.596P PD=12.596U PS=12.596U NRD=0.465 NRS=0.465
M_U9_U9_M6  INT_VCC 34 30 INT_VCC MHS4XPES L=1.0U W=119.298U
+ AD=238.596P AS=238.596P PD=242.596U PS=242.596U NRD=0.017 NRS=0.017
M_U9_U9_M7  INT_VCC Q 33 INT_VCC MHS4XPES L=1.0U W=2.298U
+ AD=4.596P AS=4.596P PD=8.596U PS=8.596U NRD=0.870 NRS=0.870
M_U9_U9_M8  33 Q INT_GND INT_GND MHS4XNES L=1.0U W=4.926U
+ AD=9.852P AS=9.852P PD=13.852U PS=13.852U NRD=0.406 NRS=0.406
M_U9_U9_M9  35 32 INT_GND INT_GND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_U9_U9_M10  35 49 INT_GND INT_GND MHS4XNES L=1.0U W=39.926U
+ AD=79.852P AS=79.852P PD=83.852U PS=83.852U NRD=0.050 NRS=0.050
M_U9_U9_M11  31 32 INT_GND INT_GND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
M_U9_U9_M12  31 49 INT_GND INT_GND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
Q_U9_U9_Q1  INT_VCC 31 35 DA0ACBSS
X_U9_U9_D1  31 Q INT_GND DB0308AS
M_U9_U9_M13  INT_VCC 49 36 INT_VCC MHS4XPES L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M_U9_U9_M14  36 32 34 INT_VCC MHS4XPES L=1.0U W=49.298U
+ AD=98.596P AS=98.596P PD=102.596U PS=102.596U NRD=0.041 NRS=0.041
M_U9_U9_M15  34 32 INT_GND INT_GND MHS4XNES L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
M_U9_U9_M16  34 49 INT_GND INT_GND MHS4XNES L=1.0U W=24.926U
+ AD=49.852P AS=49.852P PD=53.852U PS=53.852U NRD=0.080 NRS=0.080
C_U9_C2  INT_OGND INT_VCC 1U
C_U9_C3  INT_OGND INT_VCC 1U
R_U9_U10_R5  Q 37 5K
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```
E_U9_U10_E7  41 42 40 37 0.5
V_U9_U10_V3  42 0   1.25
E_U9_U10_E8  38 0 41 0 30
E_U9_U10_E9  45 0 46 0 1
V_U9_U10_V4  47 46   0.5
E_U9_U10_E10  43 48 38 0 -1
V_U9_U10_V5  48 0   3
V_U9_U10_V6  40 INT_VCC   0.3
R_U9_U10_R12  40 0 10MEG
M_U9_U10_M1  37 E 0 INT_GND MHS4XNES L=1.0U W=9.926U
+ AD=19.852P AS=19.852P PD=23.852U PS=23.852U NRD=0.201 NRS=0.201
R_U9_U10_R8  38 INT_GND 10MEG
M_U9_U10_M11  39 38 INT_GND INT_GND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_U9_U10_M12  47 38 39 INT_VCC MHS4XPES L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
R_U9_U10_R10  41 0 10MEG
M_U9_U10_M13  44 43 INT_GND INT_GND MHS4XNES L=1.0U W=29.926U
+ AD=59.852P AS=59.852P PD=63.852U PS=63.852U NRD=0.067 NRS=0.067
M_U9_U10_M14  INT_VCC 43 44 INT_VCC MHS4XPES L=1.0U W=59.298U
+ AD=118.596P AS=118.596P PD=122.596U PS=122.596U NRD=0.034 NRS=0.034
X_U9_U10_D4  38 45 INT_GND DB3002AS
R_U9_U10_R11  46 0 10MEG
M_U2_M1  INT_VCC E 49 INT_VCC MHS4XPES L=1.0U W=199.298U
+ AD=398.596P AS=398.596P PD=402.596U PS=402.596U NRD=0.010 NRS=0.010
M_U2_M2  49 E INT_GND INT_GND MHS4XNES L=1.0U W=104.926U
+ AD=209.852P AS=209.852P PD=213.852U PS=213.852U NRD=0.019 NRS=0.019
.ENDS OUTCKTS
```

Section 5
LVT16

SPICE

CONTENTS

Each LVT16 device requires some combination of an input stage, possibly an intermediate inverting stage, an output stage, and some package parasitics. Table 5-1 shows LVT16 model combinations that correlate input, inverting, and output structures for each part type.

Table 5-1. LVT16 Model Combinations

LVT	Input Circuit	Inverter Circuit	Output Circuit	Inverting Output	Subcircuit Name
240A	INV20	IOCL	OUTD	Yes	INV1
240A-1	INV20	IOCL	OUTD	Yes	INV1_1
244B	IOCL	–	OUTD	No	NINV1
244B-1	IOCL	–	OUTD	No	NINV1_1
245B	IOCL	–	OUTD	No	NINV1
245B-1	IOCL	–	OUTD	No	NINV1_1
373A	IOCL	–	OUTD	No	NINV1
374A	IOCL	–	OUTD	No	NINV1
500A	IOCL	–	OUTD	No	NINV1
501A	IOCL	–	OUTD	No	NINV1
543A	IOCL	–	OUTD	No	NINV1
646A	IOCL	–	OUTD	No	NINV1
652A	IOCL	–	OUTD	No	NINV1

The data sheet section provides information on each LVT16 part type. Each data sheet contains a part description, part features, quick reference data, ordering information, pin configuration, logic symbol or logic diagram, and function table.

To do simulations on a particular part type, refer to the LVT16 Netlists section of the book. That section contains files called "LVT16XX.CIR" that are simulation test circuits for individual device types. The files are also in the LVT directory in the attached diskette which also includes files for subcircuits and primitive elements. The "XX" in LVT16XX.CIR refers to HS or PS for HSPICE and PSPICE. The programs are written in Berkeley SPICE format and can be run on HSPICE or PSPICE simulators. See the HSPICE or PSPICE subdirectories for the appropriate program you need. Transient analysis statements are included but can be changed to suit the application. Values for V_{CC} and input voltages are also included and these may changed to suit the application. Figure 5-1 shows how the test circuits are assembled.

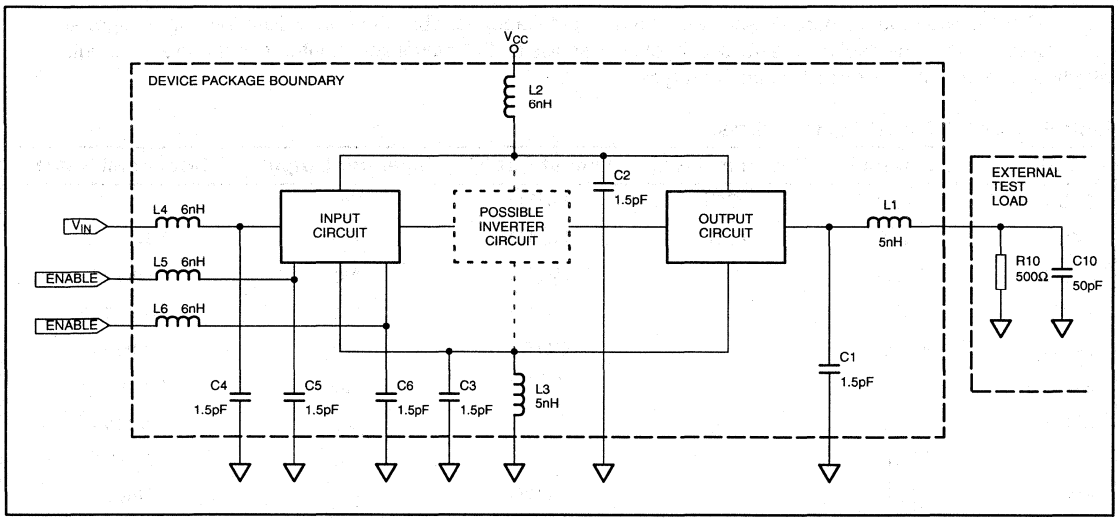


Figure 5-1. Examples of LVT16 Test Circuits

Also in the Netlists section of the book are files called LVT16SUB.SPC. These files contain subcircuits for each part type, input, output, and inverter blocks, and nominal value package parasitics to simulate a die in a package. The values may be changed for a particular package, and these values are listed in the Packaging section of the book.

Libraries for primitive elements, such as resistors, diodes and transistors, etc., are also included for reference. The file names are called "LVT16XXX.SPC". "XXX" refers to NOM, FAS, or SLO for nominal, fast, and slow process corners.

For clarification, the following illustration shows how the three programs interact with each other:

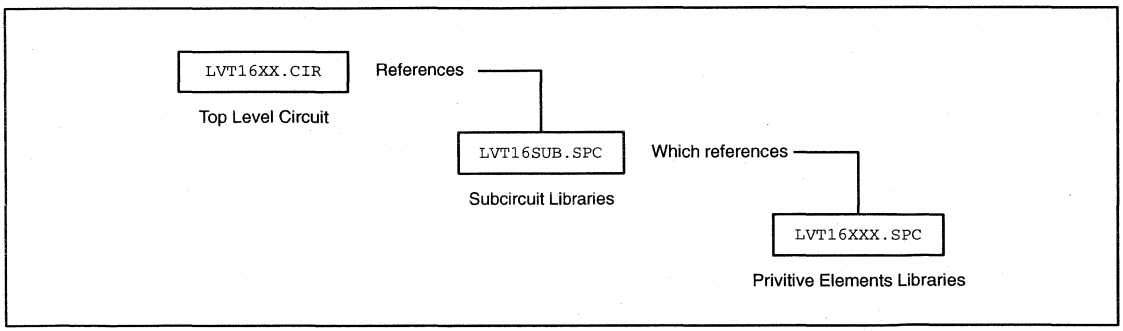


Figure 5-2. LVT16 SPICE Program Hierarchy

Note that in the top level program, LVT16XX.CIR, the ".INC" command that specifies the path to reference the other two programs should be modified to reflect your disk directory structure.

LVT16 Short-form Datasheets

3.3V LVT 16-bit inverting buffer/driver (3-State) 74LVT16240A

FEATURES

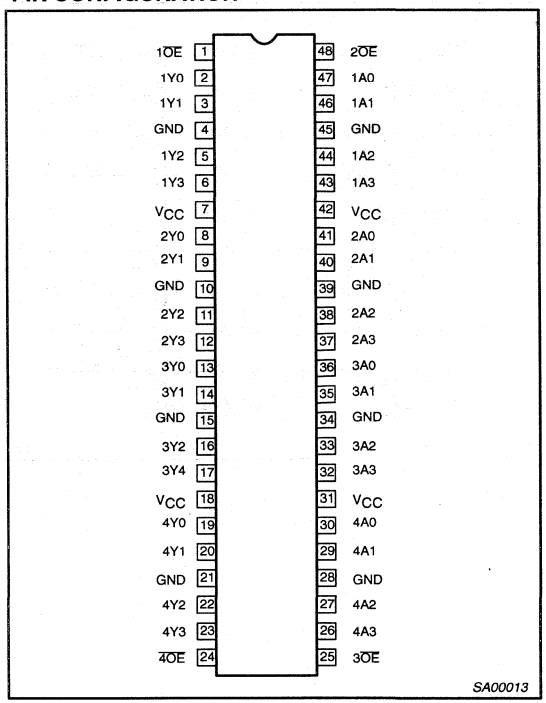
- 16-bit bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74LVT16240A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$), each controlling four of the 3-State outputs.

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0-1A3 2A0-2A3 3A0-3A3 4A0-4A3	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	$1\overline{Y}0$-$1\overline{Y}3$ $2\overline{Y}0$-$2\overline{Y}3$ $3\overline{Y}0$-$3\overline{Y}3$ $4\overline{Y}0$-$4\overline{Y}3$	Data outputs
1, 48, 25, 24	$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

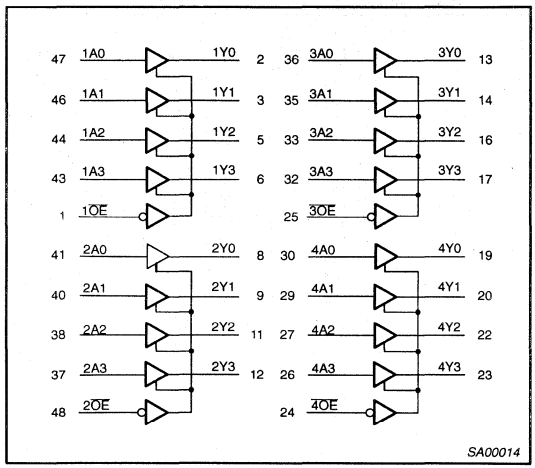
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	C_L = 50pF; V_{CC} = 3.3V	1.8 2.0	ns
C_{IN}	Input capacitance n$\overline{OE}$	V_I = 0V or 3.0V	3	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	9	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic Shrink Small Outline (SSOP) Type III	-40°C to +85°C	74LVT16240ADL	SOT370-1
48-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	-40°C to +85°C	74LVT16240ADGG	SOT362-1

LOGIC SYMBOL



FUNCTION TABLE

Inputs		Outputs
$n\overline{OE}$	nAx	$n\overline{Y}x$
L	L	H
L	H	L
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

3.3V LVT 16-bit inverting buffer/driver with 30Ω termination resistors (3-State)

74LVT16240A-1

FEATURES

- 16-bit bus interface
- 3-State buffers
- Output capability: +12mA/-12mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Outputs include series resistance of 30Ω making external termination resistors unnecessary
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74LVT16240A-1 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$), each controlling four of the 3-State outputs.

The 74LVT16240A-1 is designed with 30Ω series resistance in both the pull-up and pull-down output structures. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters.

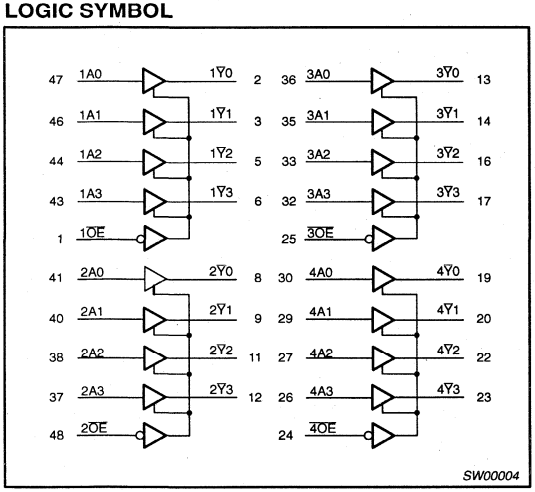
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	C_L = 50pF; V_{CC} = 3.3V	2.6 2.6	ns
C_{IN}	Input capacitance n$\overline{OE}$	V_I = 0V or 3.0V	3	pF
C_{OUT}	Output capacitance	V_O = 0V or 3.0V	9	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic Shrink Small Outline (SSOP) Type III	-40°C to +85°C	74LVT16240A-1DL	SOT370-1
48-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	-40°C to +85°C	74LVT16240A-1DGG	SOT362-1

LOGIC SYMBOL



FUNCTION TABLE

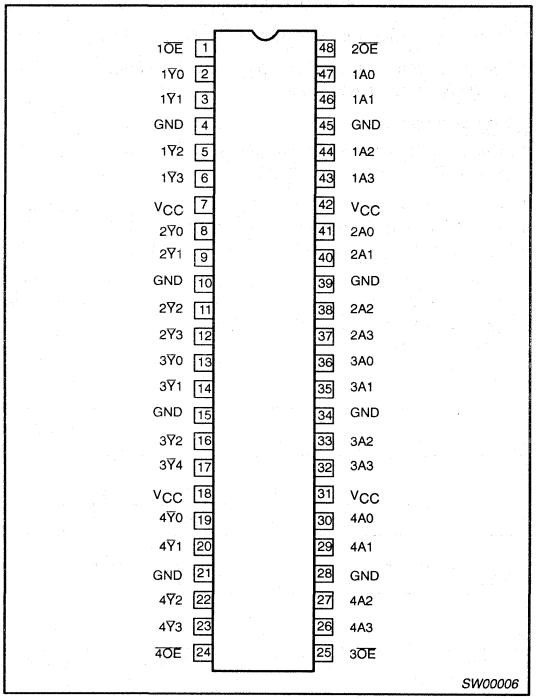
INPUTS		OUTPUTS
n$\overline{OE}$	nAx	n$\overline{Y}$x
L	L	H
L	H	L
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

3.3V LVT 16-bit inverting buffer/driver with 30Ω termination resistors (3-State)

74LVT16240A-1

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0 - 1A3 2A0 - 2A3 3A0 - 3A3 4A0 - 4A3	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1$\overline{Y}$0 - 1$\overline{Y}$3 2$\overline{Y}$0 - 2$\overline{Y}$3 3$\overline{Y}$0 - 3$\overline{Y}$3 4$\overline{Y}$0 - 4$\overline{Y}$3	Data outputs
1, 48 25, 24	1$\overline{OE}$, 2$\overline{OE}$, 3$\overline{OE}$, 4$\overline{OE}$	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

3.3V LVT 16-bit buffer/driver (3-State) 74LVT16244B

FEATURES

- 16-bit bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74LVT16244B is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is a 16-bit buffer and line driver featuring non-inverting 3-State bus outputs. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer.

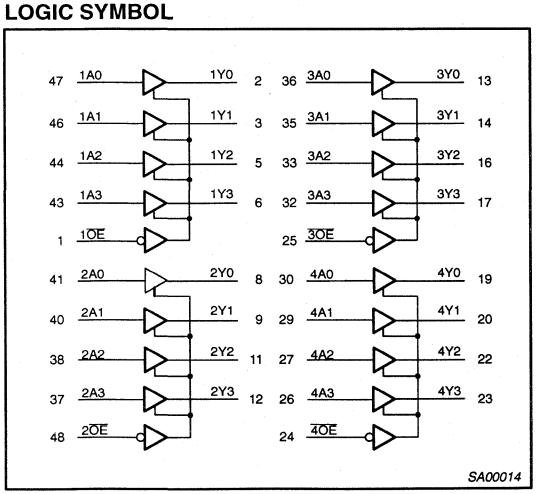
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 3.3V	1.8 1.7	ns
C_{IN}	Input capacitance $n\overline{OE}$	V_I = 0V or 3.0V	3	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	9	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic Shrink Small Outline (SSOP) Type III	-40°C to +85°C	74LVT16244BDL	SOT370-1
48-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	-40°C to +85°C	74LVT16244BDGG	SOT362-1

LOGIC SYMBOL

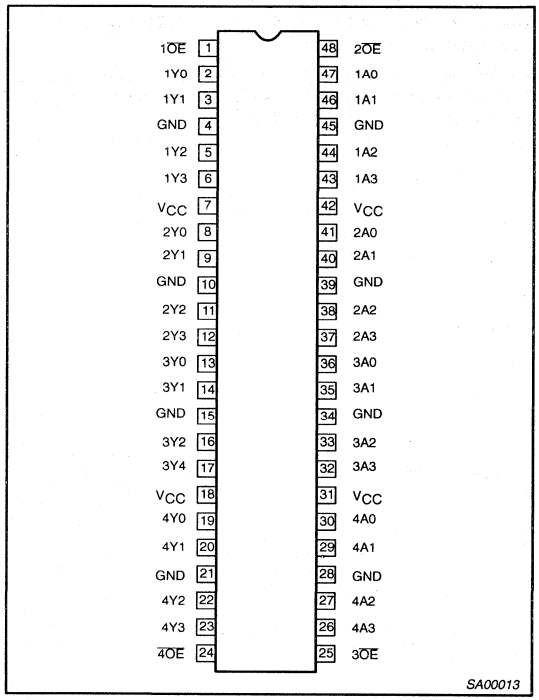


FUNCTION TABLE

INPUTS		OUTPUTS
$n\overline{OE}$	nAx	nYx
L	L	L
L	H	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43 41, 40, 38, 37 36, 35, 33, 32 30, 29, 27, 26	1A0 - 1A3, 2A0 - 2A3, 3A0 - 3A3, 4A0 - 4A3	Data inputs
2, 3, 5, 6 8, 9, 11, 12 13, 14, 16, 17 19, 20, 22, 23	1Y0 - 1Y3, 2Y0 - 2Y3, 3Y0 - 3Y3, 4Y0 - 4Y3	Data outputs
1, 48 25, 24	1$\overline{OE}$, 2$\overline{OE}$, 3$\overline{OE}$, 4$\overline{OE}$	Output enables
4, 10, 15, 21 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

3.3V LVT 16-bit buffer/driver with 30Ω termination resistors (3-State)

74LVT16244B-1

FEATURES

- 16-bit bus interface
- 3-State buffers
- Output capability: +12mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Outputs include series resistance of 30Ω making external terminating resistors unnecessary
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74LVT16244B-1 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

The 74LVT16244B-1 is designed with 30Ω series resistance in both the High and Low states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters.

This device is a 16-bit buffer and line driver featuring non-inverting 3-State bus outputs. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer.

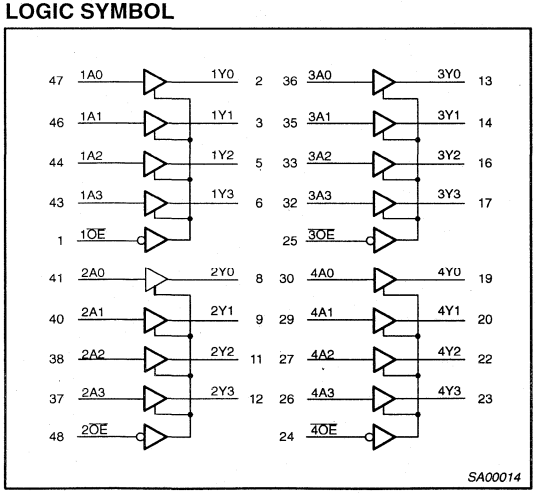
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 3.3V	2.8 2.5	ns
C_{IN}	Input capacitance $n\overline{OE}$	V_I = 0V or 3.0V	3	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	9	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic Shrink Small Outline (SSOP) Type III	-40°C to +85°C	74LVT16244B-1DL	SOT370-1
48-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	-40°C to +85°C	74LVT16244B-1DGG	SOT362-1

LOGIC SYMBOL



FUNCTION TABLE

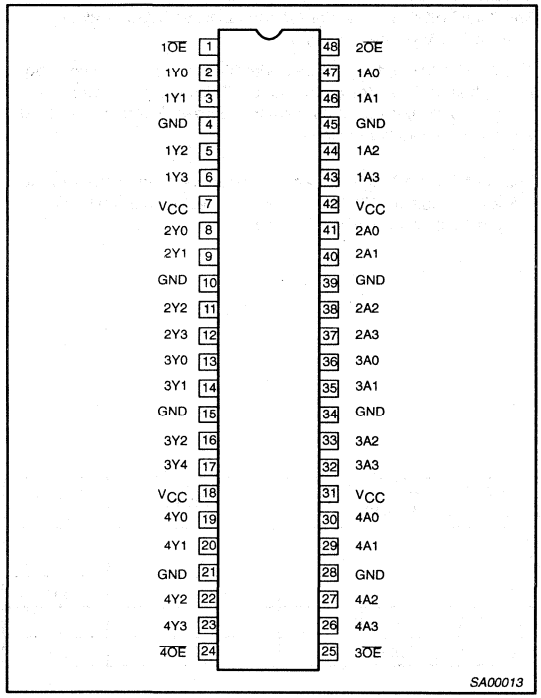
INPUTS		OUTPUTS
$n\overline{OE}$	nAx	nYx
L	L	L
L	H	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

3.3V LVT 16-bit buffer/driver with 30Ω termination resistors (3-State)

74LVT16244B-1

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43 41, 40, 38, 37 36, 35, 33, 32 30, 29, 27, 26	1A0 - 1A3, 2A0 - 2A3, 3A0 - 3A3, 4A0 - 4A3	Data inputs
2, 3, 5, 6 8, 9, 11, 12 13, 14, 16, 17 19, 20, 22, 23	1Y0 - 1Y3, 2Y0 - 2Y3, 3Y0 - 3Y3, 4Y0 - 4Y3	Data outputs
1, 48 25, 24	$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	Output enables
4, 10, 15, 21 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

3.3V ABT 16-bit transceiver (3-State) 74LVT16245B

FEATURES

- 16-bit bidirectional bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT16245B is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

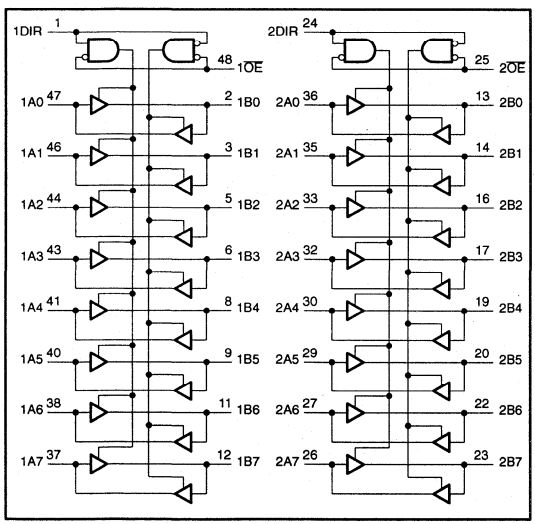
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF; V_{CC} = 3.3V	1.9	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	$V_{I/O}$ = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic Shrink Small Outline (SSOP) Type III	–40°C to +85°C	74LVT16245BDL	SOT370-1
48-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74LVT16245BDGG	SOT362-1

LOGIC SYMBOL

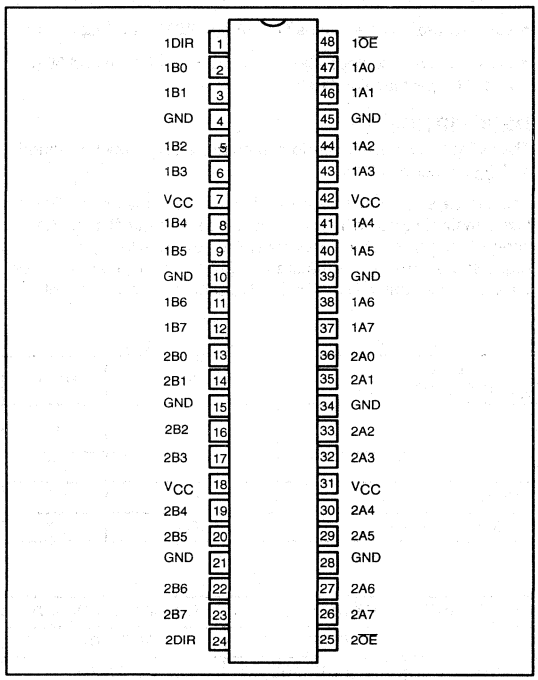


FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
n$\overline{OE}$	nDIR	nAx	nBx
L	L	nAx = nBx	Inputs
L	H	Inputs	nBx = nAx
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 24	nDIR	Direction control input
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	nA0 – nA7	Data inputs/outputs (A side)
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	nB0 – nB7	Data inputs/outputs (B side)
25, 48	$n\overline{OE}$	Output enable input (active-Low)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

3.3V LVT 16-bit transceiver with 30Ω termination resistors (3-State)

74LVT16245B-1

FEATURES

- 16-bit bidirectional bus interface
- 3-State buffers
- Output capability: +12mA/–12mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Outputs include series resistance of 30Ω making external termination resistors unnecessary
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74LVT16245B-1 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($n\overline{OE}$) input for easy cascading and a Direction (nDIR) input for direction control.

The 74LVT16245B-1 is designed with 30Ω series resistance in both the High and Low states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF; V_{CC} = 3.3V	2.5 2.1	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

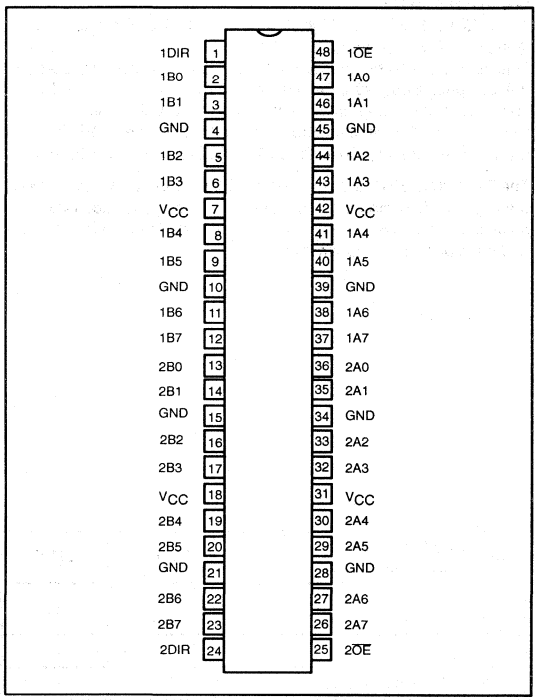
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic Shrink Small Outline (SSOP)	–40°C to +85°C	VT16245B-1 DL	SOT370-1
48-Pin Plastic Thin Shrink Small Outline (TSSOP)	–40°C to +85°C	VT16245B-1 DGG	SOT362-1

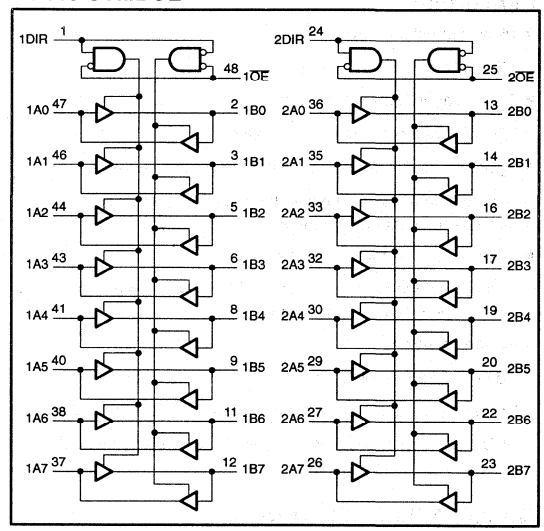
3.3V LVT 16-bit transceiver with 30Ω termination resistors (3-State)

74LVT16245B-1

PIN CONFIGURATION



LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 24	nDIR	Direction control input
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	nA0 – nA7	Data inputs/outputs (A side)
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	nB0 – nB7	Data inputs/outputs (B side)
25, 48	$\overline{nOE}$	Output enable input (active-Low)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

FUNCTION TABLE

Inputs		Inputs/Outputs	
$n\overline{OE}$	nDIR	nAx	nBx
L	L	nAx = nBx	Inputs
L	H	Inputs	nBx = nAx
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

3.3V ABT 16-bit D-type flip-flop | 74LVT16273A

FEATURES

- 16-bit D-type edge triggered flip-flops
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

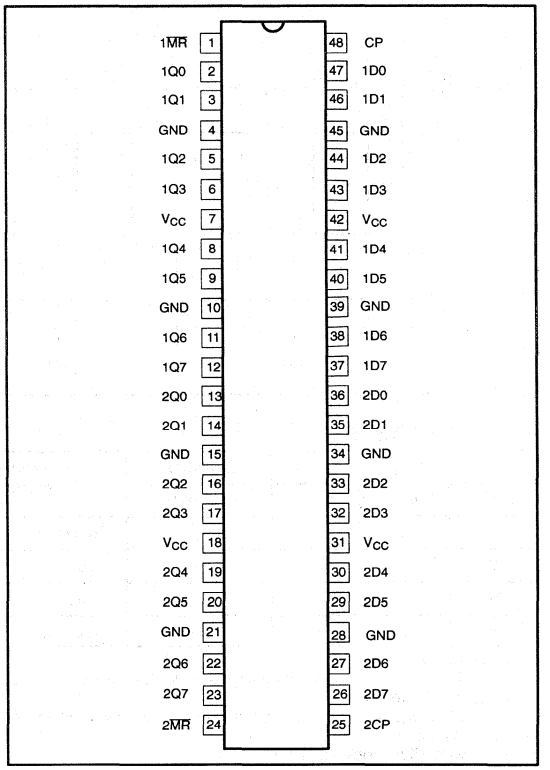
DESCRIPTION

The LVT16273A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This part is a 16-bit edge triggered D-type flip-flop with non-inverting high drive outputs. This device can be used as two 8-bit flip-flops or one 16-bit flip-flop. When the clock (CP) goes High, the data on the D inputs is stored and the Q outputs display the stored data.

This device also features a master reset ($\overline{MR}$) that resets all flip-flops to the Low state when $\overline{MR}$ is set to the Low state.

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 24	$1\overline{MR}$, $2\overline{MR}$	Master reset input (active-Low)
2, 3, 5, 6, 8, 9, 11, 12,13, 14, 16, 17, 19, 20, 22, 23	1Q0-1Q7 2Q0-2Q7	Data outputs
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1D0-1D7 2D0-2D-7	Data inputs
25, 48	1CP, 2CP	Clock pulse input (active rising edge)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

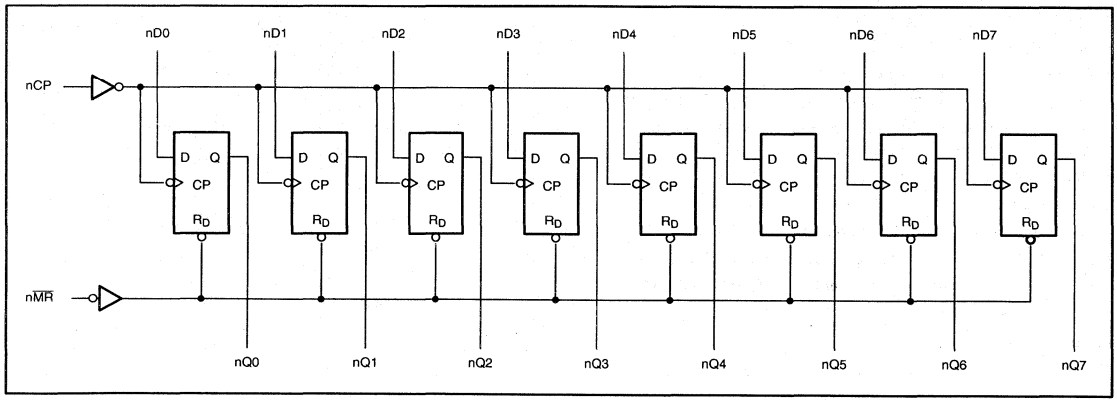
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 3.3V		ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
I_{CCH}	Total supply current	Outputs High; V_{CC} = 3.6V	0.13	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic Shrink Small Outline (SSOP) Type III	–40°C to +85°C	74LVT16273ADL	SOT370-1
48-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74LVT16273ADGG	SOT362-1

LOGIC DIAGRAM



FUNCTION TABLE

Inputs			Outputs	operating mode
$n\overline{MR}$	nCP	nDX	nQ0-nQ7	
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"
H	L	X	Q_0	Retain state

H = High voltage level
h = high voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
Q_0 = Output as it was

3.3V LVT 16-bit transparent D-type latch (3-State)

74LVT16373A

FEATURES

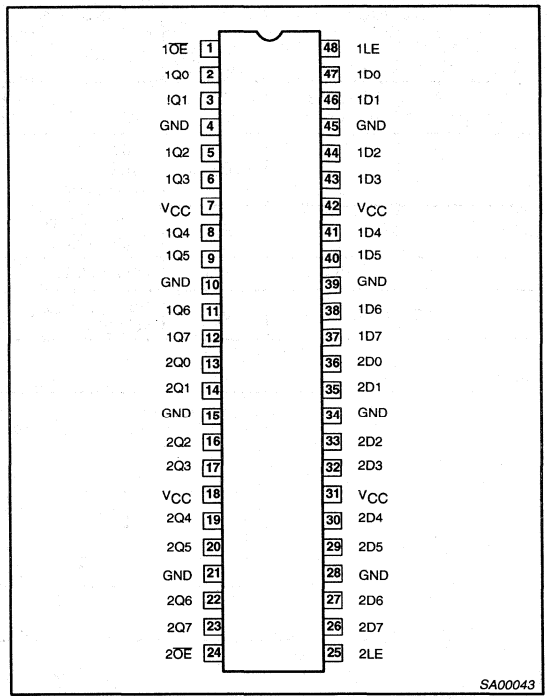
- 16-bit transparent latch
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74LVT16373A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is a 16-bit transparent D-type latch with non-inverting 3-State bus compatible outputs. The device can be used as two 8-bit latches or one 16-bit latch. When enable (E) input is High, the Q outputs follow the data (D) inputs. When enable is taken Low, the Q outputs are latched at the levels of the D inputs one setup time prior to the High-to-Low transition.

PIN CONFIGURATION



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	C_L = 50pF; V_{CC} = 3.3V	1.8 1.9	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	3	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	9	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

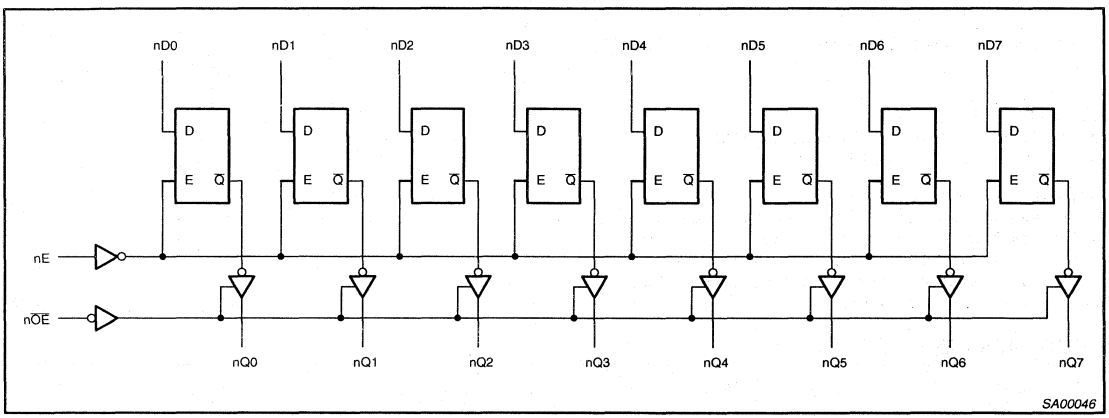
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic Shrink Small Outline (SSOP) Type III	–40°C to +85°C	74LVT16373ADL	SOT370-1
48-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74LVT16373ADGG	SOT362-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1D0 – 1D7 2D0 – 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Q0 – 1Q7 2Q0 – 2Q7	Data outputs
1, 24	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
48, 25	1E, 2E	Enable inputs (active-High)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$n\overline{OE}$	nE	nDx	REGISTER	nQ0 – nQ7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	l h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X nDx	NC nDx	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

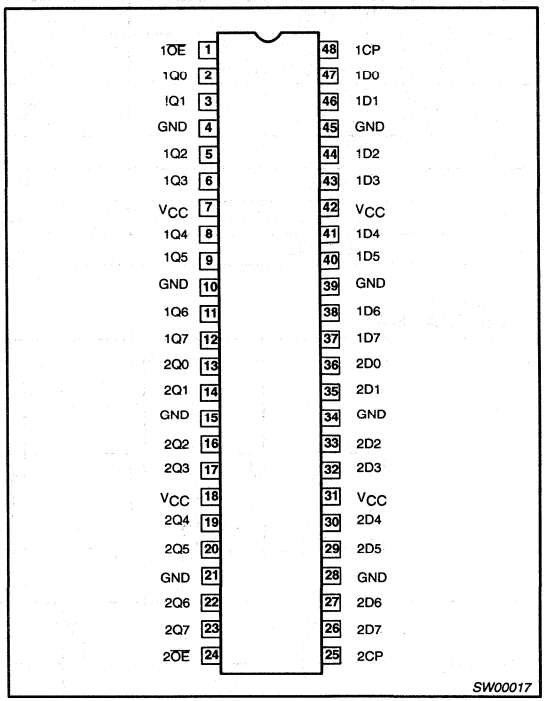
3.3V LVT 16-bit edge-triggered D-type flip-flop (3-State)

74LVT16374A

FEATURES

- 16-bit edge-triggered flip-flop
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

PIN CONFIGURATION



DESCRIPTION

The 74LVT16374A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is a 16-bit edge-triggered D-type flip-flop featuring non-inverting 3-State outputs. The device can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CP), the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	C_L = 50pF; V_{CC} = 3.3V	2.9 3.0	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	3	pF
C_{OUT}	Output pin capacitance	Outputs disabled; V_O = 0V or 3.0V	9	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

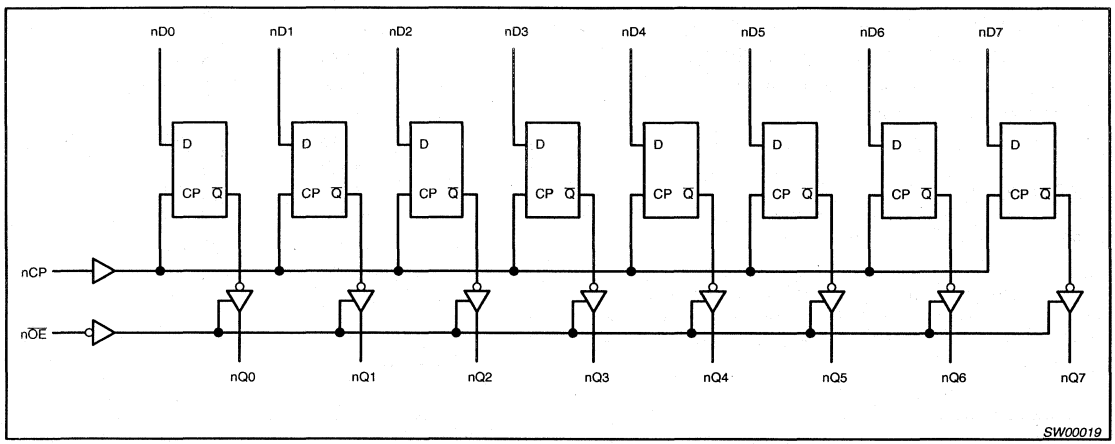
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic Shrink Small Outline (SSOP) Type III	-40°C to +85°C	74LVT16374ADL	SOT370-1
48-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	-40°C to +85°C	74LVT16374ADGG	SOT362-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37 36, 35, 33, 32, 30, 29, 27, 26	1D0 - 1D7 2D0 - 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12 13, 14, 16, 17, 19, 20, 22, 23	1Q0 - 1Q7 2Q0 - 2Q7	Data outputs
1, 24	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
48, 25	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$n\overline{OE}$	nCP	nDx	REGISTER	nQ0 - nQ7	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↧	X	NC	NC	Hold
H H	↧ ↑	X nDx	NC nDx	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↧ = Not a Low-to-High clock transition

3.3V LVT 18-bit universal bus transceiver (3-State) 74LVT16500A

FEATURES

- 18-bit bidirectional bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Positive edge-triggered clock inputs
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

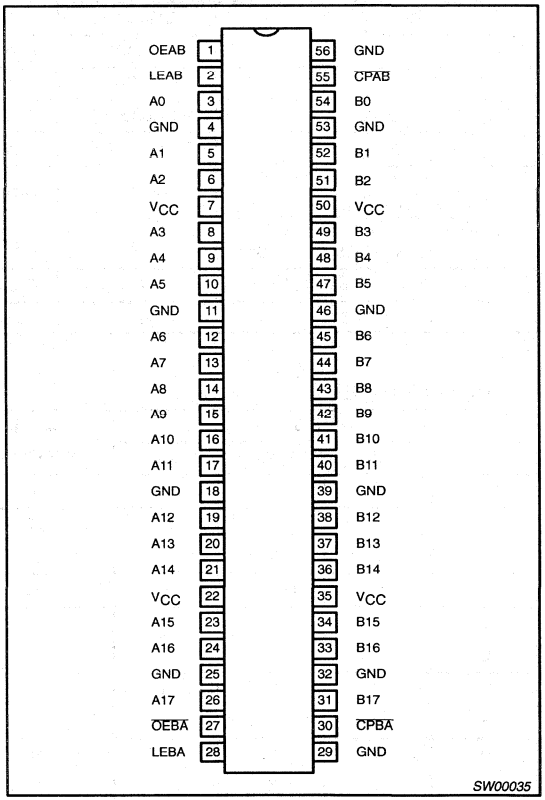
The LVT16500A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable (OEAB and $\overline{OEBA}$), latch enable (LEAB and LEBA), and clock ($\overline{CPAB}$ and $\overline{CPBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is High. When LEAB is Low, the A data is latched if $\overline{CPAB}$ is held at a High or Low logic level. If LEAB is Low, the A-bus data is stored in the latch/flip-flop on the Low-to-High transition of $\overline{CPAB}$. When OEAB is High, the outputs are active. When OEAB is Low, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{OEBA}$, LEBA and $\overline{CPBA}$. The output enables are complimentary (OEAB is active High, and $\overline{OEBA}$ is active Low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

PIN CONFIGURATION



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 3.3V	1.5 2.1	ns
C_{IN}	Input capacitance (Control pins)	V_I = 0V or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	9	pF
I_{CCL}	Quiescent supply current	Outputs disabled; V_{CC} = 3.6V	4	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-Pin Plastic Shrink Small Outline (SSOP) Type III	–40°C to +85°C	VT16500ADL	SOT371-1
56-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	VT16500ADGG	SOT364-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	A-to-B Output enable input
27	$\overline{OEBA}$	B-to-A Output enable input (active low)
2, 28	LEAB/LEBA	A-to-B/B-to-A Latch enable input
55,30	$\overline{CPAB}$/$\overline{CPBA}$	A-to-B/B-to-A Clock input (active falling edge)
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0-A17	Data inputs/outputs (A side)
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0-B17	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

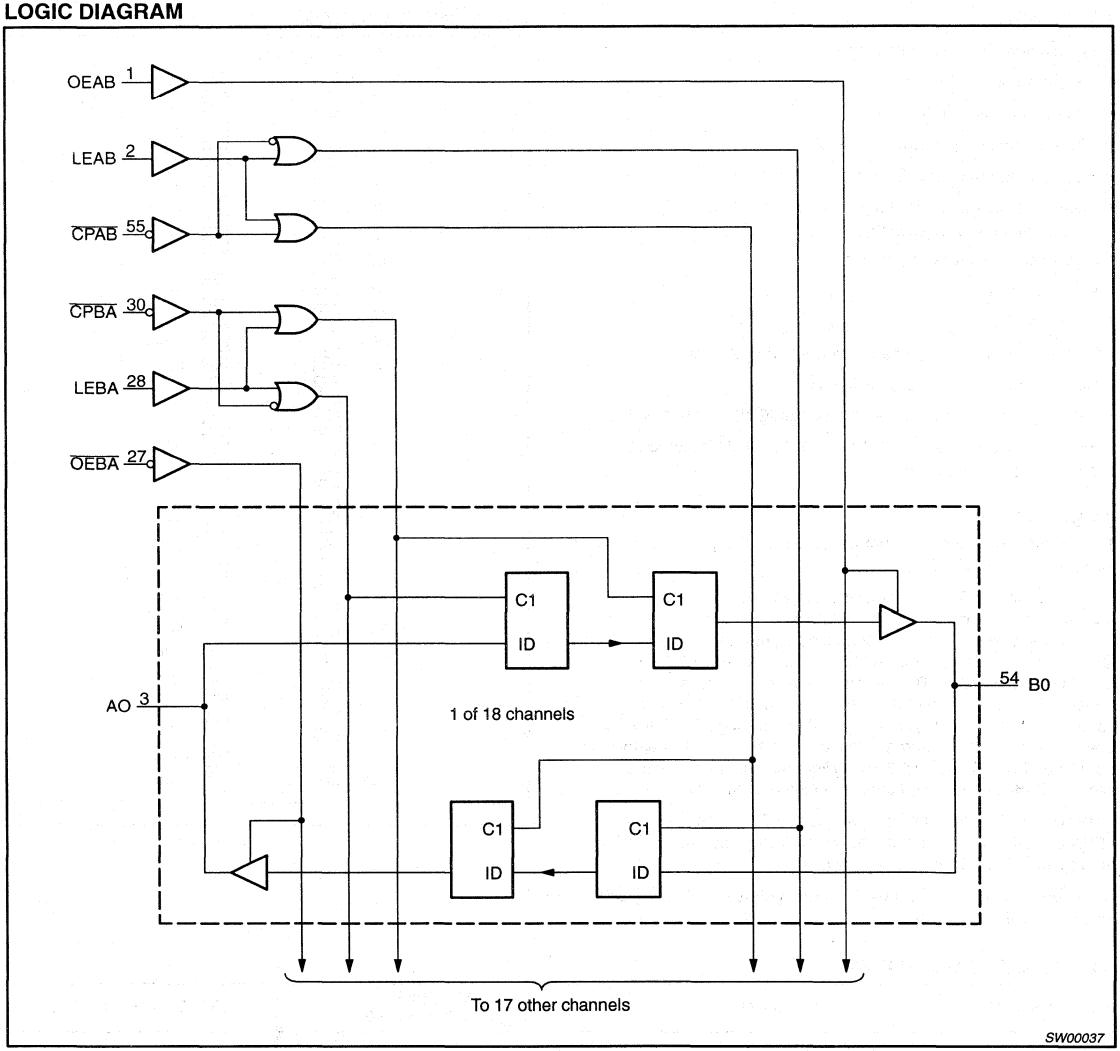
FUNCTION TABLE

INPUTS				Internal Registers	OUTPUTS	OPERATING MODE
OEAB	LEAB	$\overline{CPAB}$	An		Bn	
L	H	X	X	X	Z	Disabled
L	↓	X	h	H	Z	Disabled, Latch data
L	↓	X	l	L	Z	
L	L	H or L	X	NC	Z	Disabled, Hold data
L	L	↓	h	H	Z	Disabled, Clock data
L	L	↓	l	L	Z	
H	H	X	H	H	H	Transparent
H	H	X	L	L	L	
H	↓	X	h	H	H	Latch data & display
H	↓	X	l	L	L	
H	L	↓	h	H	H	Clock data & display
H	L	↓	l	L	L	
H	L	H or L	X	H	H	Hold data & display
H	L	H or L	X	L	L	

NOTE: A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CPBA}$.

H = High voltage level
h = High voltage level one set-up time prior to the Enable or Clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Enable or Clock transition
NC= No Change
X = Don't care
Z = High Impedance "off" state
↓ = High-to-Low Enable or Clock transition

LOGIC DIAGRAM

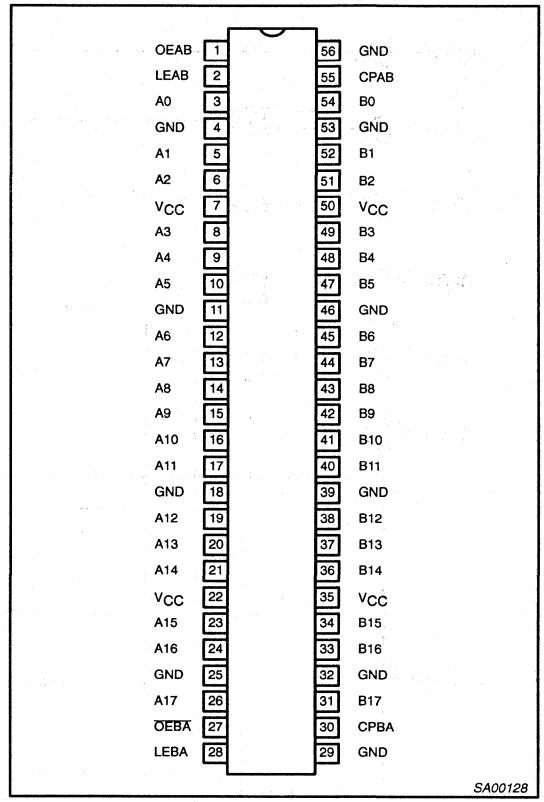


3.3V LVT 18-bit universal bus transceiver (3-State) 74LVT16501A

FEATURES

- 18-bit bidirectional bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Negative edge triggered clock inputs
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

PIN CONFIGURATION



DESCRIPTION

The LVT16501A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable (OEAB and $\overline{OEBA}$), latch enable (LEAB and LEBA), and clock (CPAB and CPBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is High. When LEAB is Low, the A data is latched if CPAB is held at a High or Low logic level. If EAB is Low, the A-bus data is stored in the latch/flip-flop on the Low-to-High transition of CPAB. When OEAB is High, the outputs are active. When OEAB is Low, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{OEBA}$, LEBA and CPBA. The output enables are complimentary (OEAB is active High, and $\overline{OEBA}$ is active Low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 3.3V	1.5 2.1	ns
C_{IN}	Input capacitance (Control pins)	V_I = 0V or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	9	pF
I_{CCL}	Quiescent supply current	Outputs disabled; V_{CC} = 3.6V	4	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-Pin Plastic Shrink Small Outline (SSOP) Type III	–40°C to +85°C	74LVT16501ADL	SOT371-1
56-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74LVT16501ADGG	SOT364-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	A-to-B Output enable input
27	$\overline{OEBA}$	B-to-A Output enable input (active low)
2, 28	LEAB/LEBA	A-to-B/B-to-A Latch enable input
55,30	CPAB/CPBA	A-to-B/B-to-A Clock input (active rising edge)
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0-A17	Data inputs/outputs (A side)
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0-B17	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

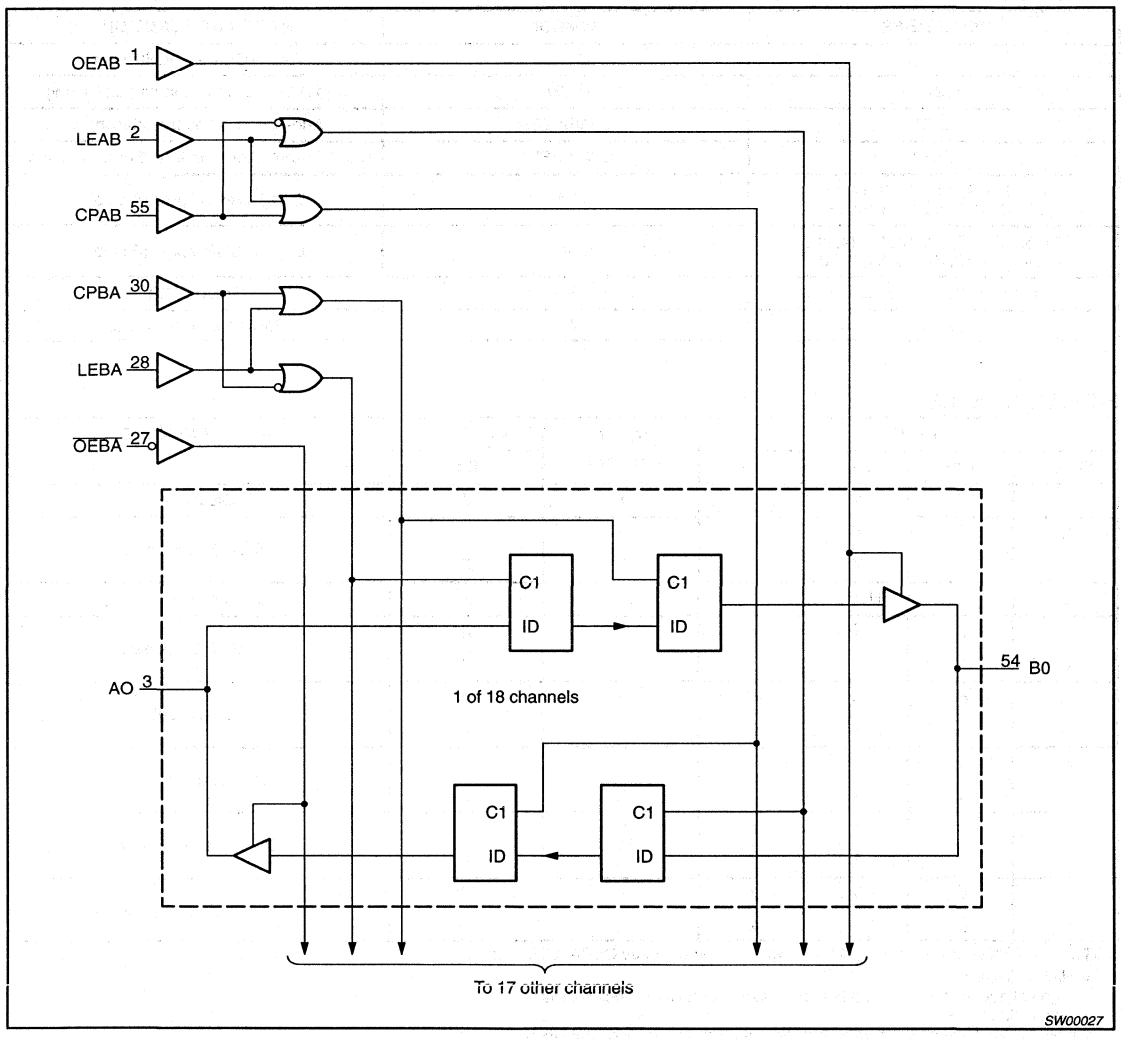
FUNCTION TABLE

INPUTS				Internal Registers	OUTPUTS	OPERATING MODE
OEAB	LEAB	CPAB	An		Bn	
L	H	X	X	X	Z	Disabled
L	↓	X	h	H	Z	Disabled, Latch data
L	↓	X	l	L	Z	
L	L	H or L	X	NC	Z	Disabled, Hold data
L	L	↑	h	H	Z	Disabled, Clock data
L	L	↑	l	L	Z	
H	H	X	H	H	H	Transparent
H	H	X	L	L	L	
H	↓	X	h	H	H	Latch data & display
H	↓	X	l	L	L	
H	L	↑	h	H	H	Clock data & display
H	L	↑	l	L	L	
H	L	H or L	X	H	H	Hold data & display
H	L	H or L	X	L	L	

NOTE: A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and CPBA.

H = High voltage level
h = High voltage level one set-up time prior to the Enable or Clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Enable or Clock transition
NC= No Change
X = Don't care
Z = High Impedence "off" state
↓ = High-to-Low Enable or Clock transition

LOGIC DIAGRAM



3.3V ABT 16-bit buffer/driver (3-State) 74LVT16541A

FEATURES

- 16-bit universal bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT16541A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device can be used as two octal buffers or one 16-bit buffer. The device is ideal for driving bus lines.

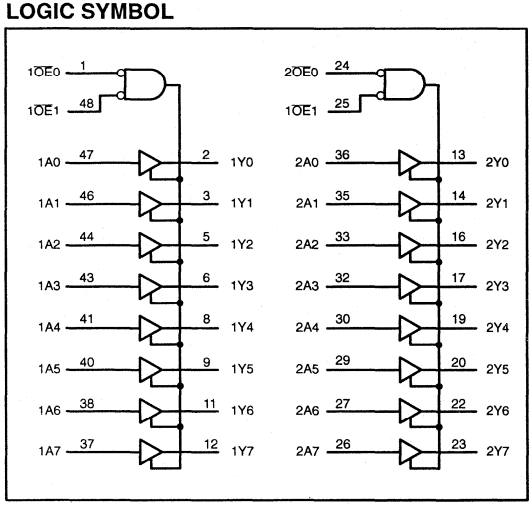
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 3.3V		ns
C_{IN}	Input capacitance $n\overline{OE}x$	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output pin capacitance	Outputs disabled; V_O = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic Shrink Small Outline (SSOP) Type III	–40°C to +85°C	74LVT16541ADL	SOT370-1
48-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74LVT16541ADGG	SOT362-1

LOGIC SYMBOL

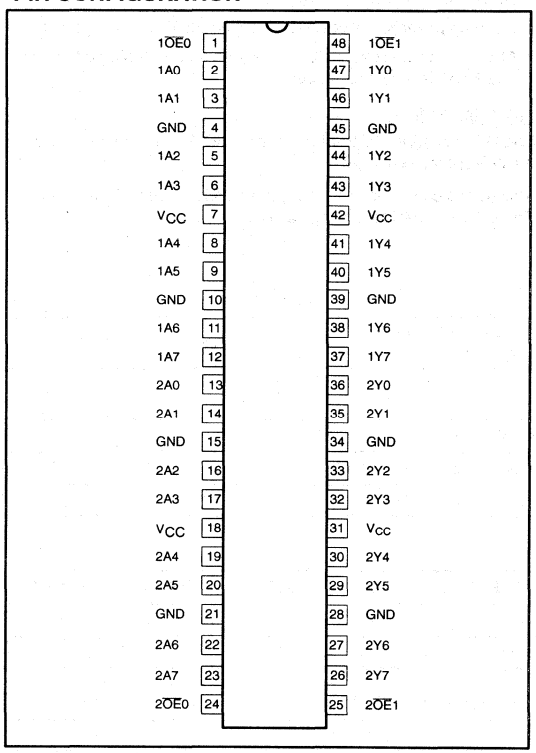


FUNCTION TABLE

INPUTS			OUTPUTS
$n\overline{OE}0$	$n\overline{OE}1$	nAx	nYx
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0–1A7 2A0–2A7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12,13, 14, 16, 17, 19, 20, 22, 23	1Y0–1Y7 2Y0–2Y7	Data outputs
1, 48 24, 25	1$\overline{OE}$0, 1$\overline{OE}$1, 2$\overline{OE}$0, 2$\overline{OE}$1	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

3.3V LVT 16-bit registered transceiver (3-State) 74LVT16543A

FEATURES

- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74LVT16543A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

The 74LVT16543A contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable ($n\overline{EAB}$) input and the A-to-B Latch Enable ($n\overline{LEAB}$) input are Low, the A-to-B path is transparent.

A subsequent Low-to-High transition of the $n\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $n\overline{EAB}$ and $n\overline{OEAB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the $n\overline{EBA}$, $n\overline{LEBA}$, and $n\overline{OEBA}$ inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

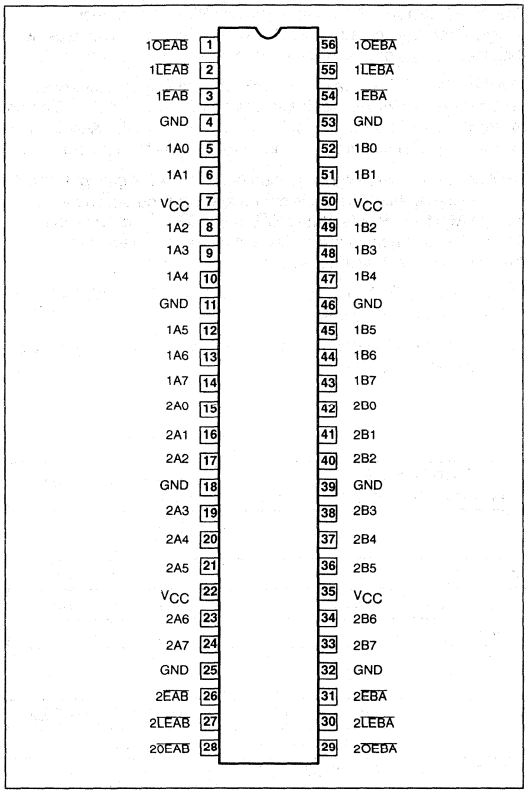
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF; V_{CC} = 3.3V	2.4 2.0	ns
C_{IN}	Input capacitance control pins	V_I = 0V or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	80	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-Pin Plastic Shrink Small Outline (SSOP)	–40°C to +85°C	VT16543A DL	SOT371-1
56-Pin Plastic Thin Shrink Small Outline (TSSOP)	–40°C to +85°C	VT16543A DGG	SOT364-1

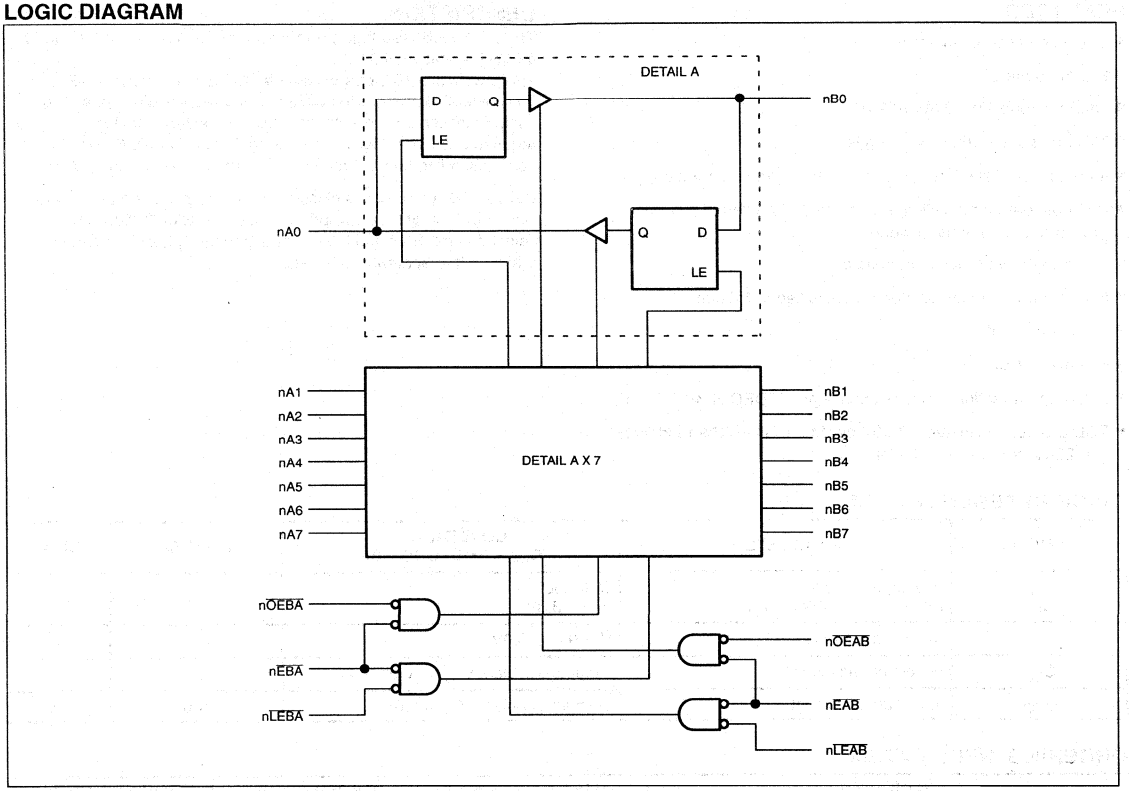
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	A Data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40,38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	B Data inputs/outputs
1, 56 28, 29	$1\overline{OEAB}$, $1\overline{OEBA}$, $2\overline{OEAB}$, $2\overline{OEBA}$	A to B / B to A Output Enable inputs (active-Low)
3, 54 26, 31	$1\overline{EAB}$, $1\overline{EBA}$, $2\overline{EAB}$, $2\overline{EBA}$	A to B / B to A Enable inputs (active-Low)
2, 55 27, 30	$1\overline{LEAB}$, $1\overline{LEBA}$, $2\overline{LEAB}$, $2\overline{LEBA}$	A to B / B to A Latch Enable inputs (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
nOEXX	nEXX	nLEXX	nAx or nBx	nBx or nAx	
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	H L	Latch + Display
L L	L L	L L	H L	H L	Transparent
L	L	H	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High transition of nLEXX or nEXX (XX = AB or BA)
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High transition of nLEXX or nEXX (XX = AB or BA)
X = Don't care
↑ = Low-to-High transition of nLEXX or nEXX (XX = AB or BA)
NC= No change
Z = High impedance or "off" state

3.3V ABT 16-bit bus transceiver (3-State) 74LVT16646A

FEATURES

- 16-bit universal bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up reset
- Power-up 3-State
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT16646A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

Data on the A or B bus is clocked into the registers on the Low to High transition of the appropriate clock (CPAB or CPBA). The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode data).

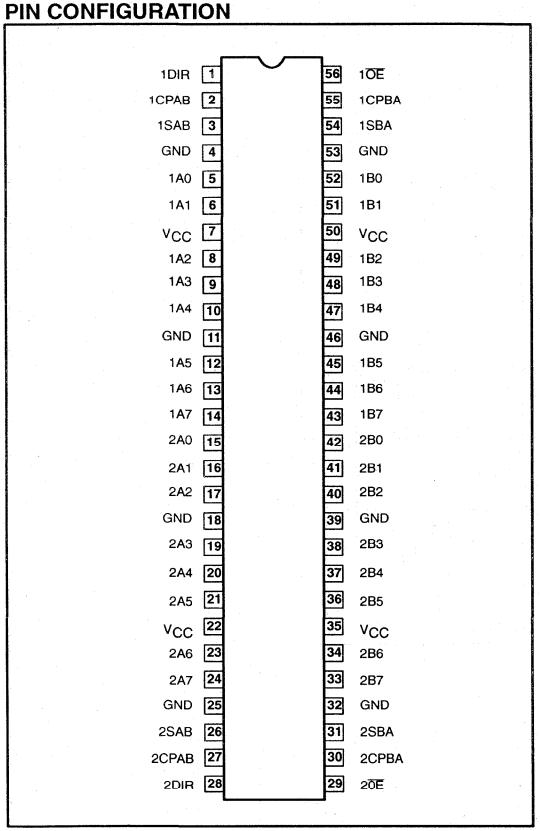
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF; V_{CC} = 3.3V	2.4	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-Pin Plastic Shrink Small Outline (SSOP) Type III	–40°C to +85°C	74LVT16646ADL	SOT371-1
56-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74LVT16646ADGG	SOT364-1

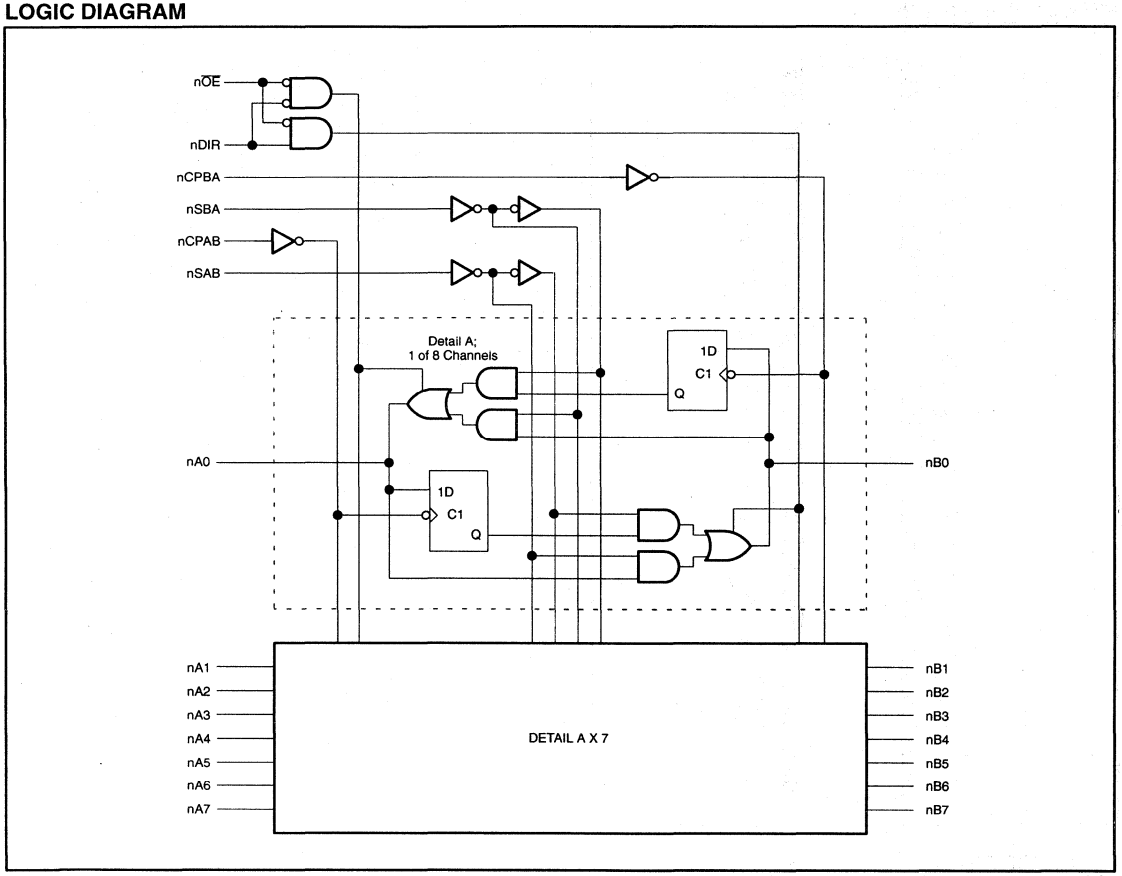
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 55, 27, 30	1CPAB, 1CPBA, 2CPAB, 2CPBA	Clock input A to B / Clock input B to A
3, 54, 26, 31	1SAB, 1SBA, 2SAB, 2SBA	Select input A to B / Select input B to A
1, 28	1DIR, 2DIR	Direction control inputs
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs (A side)
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	Data inputs/outputs (B side)
56, 29	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA	nAx	nBx	
X	X	↑	X	X	X	Input	Unspecified output*	Store A, B unspecified
X	X	X	↑	X	X	Unspecified output*	Input	Store B, A unspecified
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Stored A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the $n\overline{OE}$ input. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

3.3V LVT 16-bit bus transceiver/register (3-State) 74LVT16652A

FEATURES

- 16–bit bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74LVT16652A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complimentary output-enable (OEAB and $\overline{OEBA}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A Low-input level selects real-time data, and a High input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data.

Data on the A or B bus, or both, can be stored in the internal flip-flops by Low-to-High transitions at the appropriate clock (CPAB or CPBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last level configuration.

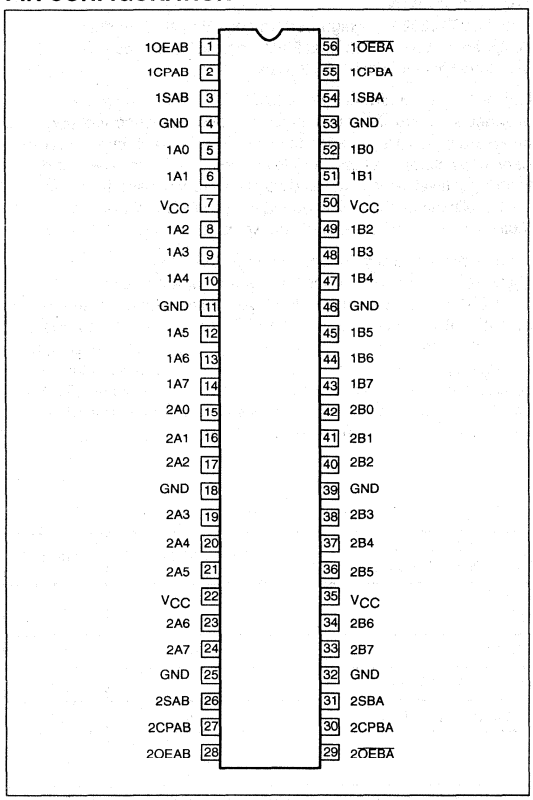
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF; V_{CC} = 3.3V	1.6 2.0	ns
C_{IN}	Input capacitance Control pins	V_I = 0V or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; V_I = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-Pin Plastic Shrink Small Outline (SSOP)	–40°C to +85°C	VT16652A DL	SOT371-1
56-Pin Plastic Thin Shrink Small Outline (TSSOP)	–40°C to +85°C	VT16652A DGG	SOT364-1

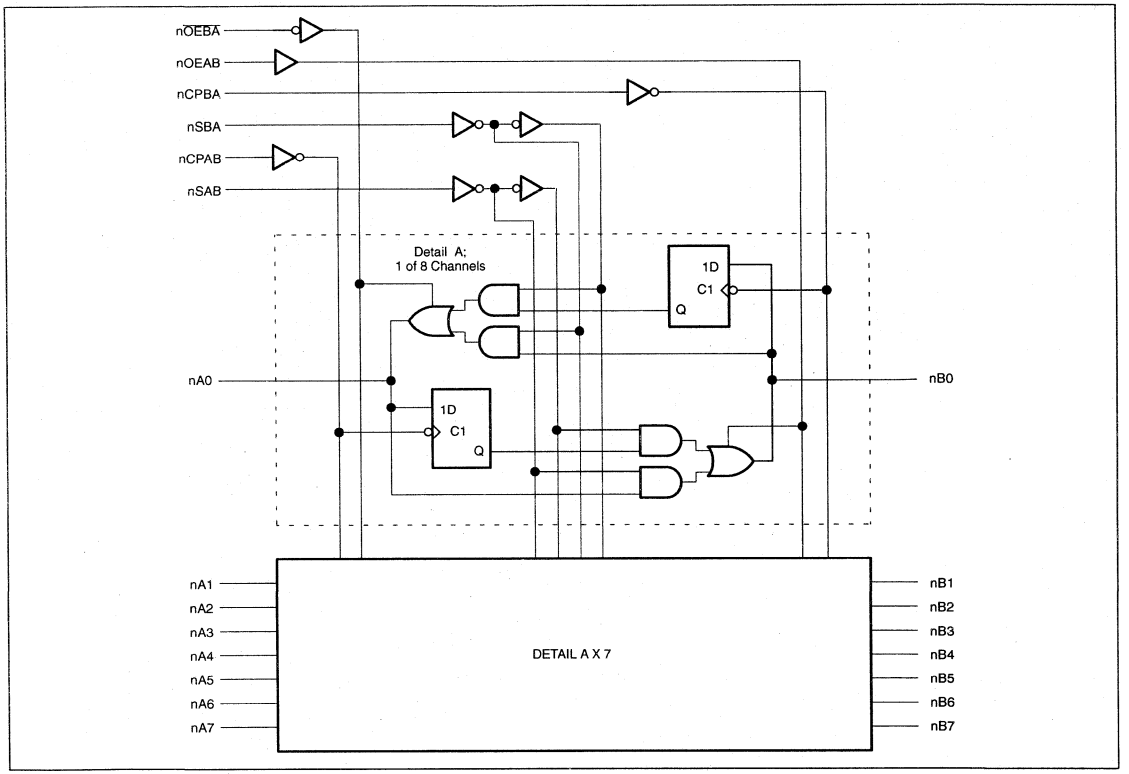
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 55, 27, 30	1CPAB, 1CPBA, 2CPAB, 2CPBA	Clock input A to B / Clock input B to A
3, 54, 26, 31	1SAB, 1SBA, 2SAB, 2SBA	Select input A to B / Select input B to A
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs (A side)
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	Data inputs/outputs (B side)
1, 56, 28, 29	1OEAB, 1$\overline{\text{OEBA}}$, 2OEAB, 2$\overline{\text{OEBA}}$	Output enable inputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
nOEAB	$\overline{nOEBA}$	nCPAB	nCPBA	nSAB	nSBA	nAx	nBx	
L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B data
X H	H H	↑ ↑	H or L ↑	X **	X X	Input	Unspecified output*	Store A, Hold B Store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X **	Unspecified output*	Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Store A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus Stored B data to A bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the $\overline{nOEBA}$ and nOEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
** If both Select controls (nSAB and nSBA) are Low, then clocks can occur simultaneously. If either Select control is High, the clocks must be staggered in order to load both registers.

LVT16 Netlists

LVT16 BERKELEY SPICE MODELS for HSPICE Simulation

```
*****************************************************************************
* LVT16HS.CIR
* Low Voltage BiCMOS Logic
* Standard Logic Product Group
* Philips Semiconductors
* 4/8/95
*****************************************************************************
* To simulate a particular device, locate the device in the section of
* this file titled "LVT16 Circuit Models.  Delete the comment mark, "*",
* in the leading column for that device only.  Make sure that the
* comment "*" is present for all other devices on the list.  To simulate
* with nominal, slow, or fast process parameters, go to the section of
* the file with the particular process corner you want and remove the
* "*".  Insure that the other parameters in the set are remarked out
* with the "*" added.  You may also wish to adjust the values of the
* load and parasitic inductors and capacitors as found in the
* LVT16SUB.SPC files according to the package chosen.  The basic files
* use nominal values.
*****************************************************************************
* Common Models for Nominal, Slow and Fast
* (Do not comment out this INCLUDE line)
.INCLUDE "C:\SPICE\LVT16\HSPICE\LVT16SUB.SPC"

*** LVT16 Circuit Models

* CHOOSE ONE & ONLY ONE DEVICE PARAMETER SET

* Nominal Parameters
.INCLUDE "C:\SPICE\LVT16\HSPICE\LVT16NOM.SPC"

* Slow Parameters
* .INCLUDE "C:\SPICE\LVT16\HSPICE\LVT16SLO.SPC"

* Fast Parameters
*.INCLUDE "C:\SPICE\LVT16\HSPICE\LVT16FAS.SPC"

* CHOOSE ONE & ONLY ONE PART FOR EACH SIMULATION

* Part Type    In   En   Enb   Out   Vcc   Subcircuit Name
* XL240A        5    7    9     4    100   INV1
* XL240A_1      5    7    9     4    100   INV1_1
XL244B         5    7    9     4    100   NINV1
* XL244B_1      5    7    9     4    100   NINV1_1
* XL245B        5    7    9     4    100   NINV1
* XL245B_1      5    7    9     4    100   NINV1_1
* XL373A        5    7    9     4    100   NINV1
* XL374A        5    7    9     4    100   NINV1
* XL500A        5    7    9     4    100   NINV1
* XL501A        5    7    9     4    100   NINV1
* XL543A        5    7    9     4    100   NINV1
* XL646A        5    7    9     4    100   NINV1
* XL652A        5    7    9     4    100   NINV1
```

```
* EXTERNAL LOAD
R10 4 0 500
C10 4 0 50PF

* POWER
VCC 100 0 3.3

* DRIVE
VIN 5 0 PULSE 0.0 3.3 2N 2.5N 2.5N 10N 25N
VOE 7 0 3.3
VOEB 9 0 0.0

.TRAN   1.000000E-11  2.500000E-08
.TEMP  .2500E+02
.OPTION  ACCT NODE OPTS LIST LIMTIM=50
+         GMIN=1.00E-12 RELTOL=1.00E-03 ABSTOL=1.00E-12
+         VNTOL=1.00E-06 TRTOL=7.00E+00
+         ITL1=1.00E+02 ITL2=1.00E+02 ITL3=4.00E+00 ITL4=2.50E+01
+         ITL5=1.00E+06 LVLTIM=2.00E+00 TNOM=+2.50E+01 LIMPTS=99999
+         CHGTOL=1.00E-14
+         MAXORD= .20E+01
+         METHOD=TRAP
+         DELMAX= 6.00E-10
+         POST
.END
```

LVT16SUB.SPC Subcircuit

```
*****************************************************************************
* LVT16 HSPICE SUBCIRCUIT LIBRARY
* LVT16SUB.SPC
* STANDARD PRODUCT LOGIC GROUP
* PHILIPS SEMICONDUCTORS
* 4/8/1995
*****************************************************************************
.SUBCKT NINV1 D E EB Q VCC
* USE THIS MODEL FOR 74LVT16244  -  245  -  373  -  374  -  500  -  501
*                                -  543  -  646  -  652
L1 111 Q 6N
L2 VCC 99 6N
L3 6 0 6N
L4 D 101 6N
L5 E 109 6N
L6 EB 110 6N
C1 111 0 1.5P
C2 99 0 1.5P
C3 6 0 1.5P
C4 101 0 1.5P
C5 109 0 1.5P
C6 110 0 1.5P
X0 101 99 6 BUSHOLD
X1 102 103 104 105 106 107 99 6 OUTD
X2 108 101 109 102 110 103 104 105 106 99 6 IOCL
X3 108 99 6 BIAS
XESD_15 111 6 ESD
XESD_16 101 6 ESD
R14 106 111 0.001
R13 107 111 0.001
.ENDS NINV1
.SUBCKT NINV1_1 D E EB Q VCC
* USE THIS MODEL FOR 74LVT16244-1  --  245-1
L1 111 Q 6N
L2 VCC 99 6N
L3 6 0 6N
L4 D 101 6N
L5 E 109 6N
L6 EB 110 6N
C1 111 0 1.5P
C2 99 0 1.5P
C3 6 0 1.5P
C4 101 0 1.5P
C5 109 0 1.5P
C6 110 0 1.5P
X0 101 99 6 BUSHOLD
X1 102 103 104 105 106 107 99 6 OUTD
X2 108 101 109 102 110 103 104 105 106 99 6 IOCL
X3 108 99 6 BIAS
XESD_15 111 6 ESD
XESD_16 101 6 ESD
R14 106 111 22.5
R13 107 111 22.5
.ENDS NINV1_1
```

```
.SUBCKT INV1 D E EB Q VCC
* USE THIS MODEL FOR 74LVT16240
L1 111 Q 6N
L2 VCC 99 6N
L3 6 0 6N
L4 D 101 6N
L5 E 109 6N
L6 EB 110 6N
C1 111 0 1.5P
C2 99 0 1.5P
C3 6 0 1.5P
C4 101 0 1.5P
C5 109 0 1.5P
C6 110 0 1.5P
X0 101 99 6 BUSHOLD
X1 102 103 104 105 106 107 99 6 OUTD
X2 108 151 109 102 110 103 104 105 106 99 6 IOCL
X3 108 99 6 BIAS
X4 101 151 99 6 INV20
XESD_15 111 6 ESD
XESD_16 101 6 ESD
R14 106 111 0.0
R13 107 111 0.0
.ENDS INV1

.SUBCKT INV1_1 D E EB Q VCC
* USE THIS MODEL FOR 74LVT16240-1
L1 111 Q 6N
L2 VCC 99 6N
L3 6 0 6N
L4 D 101 6N
L5 E 109 6N
L6 EB 110 6N
C1 111 0 1.5P
C2 99 0 1.5P
C3 6 0 1.5P
C4 101 0 1.5P
C5 109 0 1.5P
C6 110 0 1.5P
X0 101 99 6 BUSHOLD
X1 102 103 104 105 106 107 99 6 OUTD
X2 108 151 109 102 110 103 104 105 106 99 6 IOCL
X3 108 99 6 BIAS
X4 101 151 99 6 INV20
XESD_15 111 6 ESD
XESD_16 101 6 ESD
R14 106 111 22.5
R13 107 111 22.5
.ENDS INV1_1
*

.SUBCKT ESD 112 INTGND
Q10 112 INTGND INTGND INTGND HWESDLGC
.ENDS ESD
.SUBCKT BIAS 108 INTVCC INTGND
XD4 INTVCC 108 INTGND HWDS2X45P2
C4 INTVCC 108 4P
R5 INTVCC 108 4K
R4 108 INTGND 108K
.ENDS BIAS
```

```
.SUBCKT INV20 128 129 INTVCC INTGND
MQN7 129 128 INTGND INTGND HWNMOS  L=(8E-07) W=(6.5E-05) AD=36E-12 AS=36E-12
PD=43.6E-6
+PS=43.6E-6 M=1
MQP8 129 128 INTVCC INTVCC HWPMOS  L=(8E-07) W=(0.00014) AD=36E-12 AS=36E-12
+PD=43.6E-6 PS=43.6E-6 M=1
.ENDS INV20
.SUBCKT INV13 128 129 INTVCC INTGND
MQN7 129 128 INTGND INTGND HWNMOS  L=(8E-07) W=(6.5E-05) AD=36E-12 AS=36E-12
PD=43.6E-6
+PS=43.6E-6 M=1
MQP8 129 128 INTVCC INTVCC HWPMOS  L=(8E-07) W=(0.00014) AD=36E-12 AS=36E-12
+PD=43.6E-6 PS=43.6E-6 M=1
.ENDS INV13
.SUBCKT INV12 128 129 INTVCC INTGND
MQN7 129 128 INTGND INTGND HWNMOS  L=(8E-07) W=(8E-05) AD=36E-12 AS=36E-12
PD=43.6E-6
+PS=43.6E-6 M=1
MQP8 129 128 INTVCC INTVCC HWPMOS  L=(8E-07) W=(5E-05) AD=36E-12 AS=36E-12
+PD=43.6E-6 PS=43.6E-6 M=1
.ENDS INV12
.SUBCKT INV11 128 129 INTVCC INTGND
MQN7 129 128 INTGND INTGND HWNMOS  L=(8E-07) W=(2E-05) AD=36E-12 AS=36E-12
PD=43.6E-6
+PS=43.6E-6 M=1
MQP8 129 128 INTVCC INTVCC HWPMOS  L=(8E-07) W=(3E-05) AD=36E-12 AS=36E-12
+PD=43.6E-6 PS=43.6E-6 M=1
.ENDS INV11
.SUBCKT INV10 128 129 INTVCC INTGND
MQN7 129 128 INTGND INTGND HWNMOS  L=(8E-07) W=(2E-06) AD=36E-12 AS=36E-12
PD=43.6E-6
+PS=43.6E-6 M=1
MQP8 129 128 INTVCC INTVCC HWPMOS  L=(8E-07) W=(4E-06) AD=36E-12 AS=36E-12
+PD=43.6E-6 PS=43.6E-6 M=1
.ENDS INV10
.SUBCKT INV9 128 129 INTVCC INTGND
MQN7 129 128 INTGND INTGND HWNMOS  L=(8E-07) W=(1E-05) AD=36E-12 AS=36E-12
PD=43.6E-6
+PS=43.6E-6 M=1
MQP8 129 128 INTVCC INTVCC HWPMOS  L=(8E-07) W=(2E-05) AD=36E-12 AS=36E-12
+PD=43.6E-6 PS=43.6E-6 M=1
.ENDS INV9
```

```
.SUBCKT IOCL 108 101 109 113 110 114 115 116 117 INTVCC INTGND
R102 117 123 +3.000E+02
R103 117 123 +3.000E+02
XINV_99 122 119 INTVCC INTGND INV9
X10 122 124 INTVCC INTGND INV10
X11 122 118 INTVCC INTGND INV11
X12 122 118 INTVCC INTGND INV12
X13 101 122 INTVCC INTGND INV13
X14 118 110 116 117 INTVCC INTGND OUT3
X15 118 110 116 117 INTVCC INTGND OUT2
X16 113 122 110 121 115 117 INTVCC INTGND OUT1
X17 108 109 120 117 113 121 INTVCC INTGND OVRVLT
X18 122 110 121 114 INTVCC INTGND PMOSDN
X19 119 109 120 113 114 INTVCC INTGND PMOSUP
* MQP44 125 INTGND 126 INTVCC HWPMOS  L=800E-9 W=140E-6 AD=252E-12 AS=252E-12
* +PD=283.6E-6 PS=283.6E-6 M=1  (ORIG.)
MQP44 125 INTGND INTVCC INTVCC HWPMOS  L=800E-9 W=140E-6 AD=252E-12 AS=252E-12
+PD=283.6E-6 PS=283.6E-6 M=1
MQP42 INTGND INTGND 125 INTVCC HWPMOS  L=800E-9 W=65E-6 AD=117E-12 AS=117E-12
PD=133.6E-6
+PS=133.6E-6 M=1
MQN100 119 122 INTGND INTGND HWNMOS  L=800E-9 W=25E-6 AD=45E-12 AS=45E-12 PD=53.6E-6
+PS=53.6E-6 M=1
MQN127 122 124 INTGND INTGND HWNMOS  L=800E-9 W=8E-6 AD=14.4E-12 AS=14.4E-12
PD=19.6E-6
+PS=19.6E-6 M=1
MQN109 118 122 INTGND INTGND HWNMOS  L=800E-9 W=10E-6 AD=18E-12 AS=18E-12 PD=23.6E-6
+PS=23.6E-6 M=1
MQN104 123 122 127 INTGND HWNMOS  L=1E-6 W=50E-6 AD=90E-12 AS=90E-12 PD=103.6E-6
+PS=103.6E-6 M=1
MQN105 127 109 INTGND INTGND HWNMOS  L=1E-6 W=50E-6 AD=90E-12 AS=90E-12 PD=103.6E-6
+PS=103.6E-6 M=1
.ENDS IOCL

.SUBCKT OUTD 113 114 115 116 130 131 INTVCC INTGND
XD48 INTVCC 132 INTGND HWDS2X45P2
XD46 INTVCC 132 INTGND HWDS2X45P2
XD47 INTVCC 132 INTGND HWDS2X45P2
XD49 INTVCC 132 INTGND HWDS2X45P2
XD50 INTVCC 132 INTGND HWDS2X45P2
MQP38 131 114 INTVCC 113 HWPMOS  L=1E-6 W=1E-3 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP39 115 114 INTVCC 113 HWPMOS  L=800E-9 W=100E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
RBNR37 132 133 5.0
R1 116 INTGND +1.000E+04
Q29 130 116 INTGND INTGND HW40SBTCNW
Q27 133 115 131 INTGND HW40SBTCNW
Q28 130 116 INTGND INTGND HW40SBTCNW
Q30 130 116 INTGND INTGND HW40SBTCNW
Q26 133 115 131 INTGND HW40SBTCNW
Q31 130 116 INTGND INTGND HW40SBTCNW
.ENDS OUTD
```

```
.SUBCKT INV21 128 129 INTVCC INTGND
MQN7 129 128 INTGND INTGND HWNMOS  L=(1E-06) W=(2E-06) AD=36E-12 AS=36E-12
PD=43.6E-6
+PS=43.6E-6 M=1
MQP8 129 128 INTVCC INTVCC HWPMOS  L=(1E-06) W=(4E-06) AD=36E-12 AS=36E-12
+PD=43.6E-6 PS=43.6E-6 M=1
.ENDS INV21
.SUBCKT BUSHOLD 134 INTVCC INTGND
XINV_18 134 135 INTVCC INTGND INV21
MQN17 136 135 INTGND INTGND HWNMOS  L=1E-6 W=3E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP16 137 135 INTVCC INTVCC HWPMOS  L=1E-6 W=14E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
XDIO_15 137 104 INTGND HWDS3X8
R0 104 134 +2.000E+03
R1 134 136 +4.000E+03
.ENDS BUSHOLD

.SUBCKT PMOSUP 138 139 140 113 114 INTVCC INTGND
XD50 INTVCC 141 INTGND HWDS3X23
MQP38 114 140 113 113 HWPMOS  L=800E-9 W=50E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP40 114 138 113 113 HWPMOS  L=800E-9 W=20E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP39 114 139 113 113 HWPMOS  L=800E-9 W=20E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN37 142 138 INTGND INTGND HWNMOS  L=800E-9 W=8E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN36 143 139 142 INTGND HWNMOS  L=800E-9 W=8E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN34 144 140 INTGND INTGND HWNMOS  L=800E-9 W=10E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN33 118 139 144 INTGND HWNMOS  L=800E-9 W=10E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN35 114 140 143 INTGND HWNMOS  L=800E-9 W=8E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN32 145 138 118 INTGND HWNMOS  L=800E-9 W=10E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP29 145 138 INTVCC INTVCC HWPMOS  L=800E-9 W=30E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP30 145 139 INTVCC INTVCC HWPMOS  L=800E-9 W=30E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP31 145 140 INTVCC INTVCC HWPMOS  L=800E-9 W=20E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
Q5 141 145 114 INTGND HW8DBTC
.ENDS PMOSUP

.SUBCKT INV8 128 129 INTVCC INTGND
MQN7 129 128 INTGND INTGND HWNMOS  L=(8E-7) W=(2E-05) AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP8 129 128 INTVCC INTVCC HWPMOS  L=(8E-7) W=(8E-06) AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
.ENDS INV8
```

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.SUBCKT PMOSDN 146 147 148 114 INTVCC INTGND
XINV_36 114 149 INTVCC INTGND INV8
XDIO_35 150 114 INTGND HWDS3X8
MQP29 104 148 INTVCC INTVCC HWPMOS  L=800E-9 W=20E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP30 151 149 104 INTVCC HWPMOS  L=800E-9 W=20E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP31 103 147 151 INTVCC HWPMOS  L=800E-9 W=20E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP32 152 146 103 INTVCC HWPMOS  L=800E-9 W=20E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN24 152 146 INTGND INTGND HWNMOS  L=800E-9 W=6E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN23 152 148 INTGND INTGND HWNMOS  L=800E-9 W=6E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN26 152 147 INTGND INTGND HWNMOS  L=800E-9 W=6E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN27 153 147 INTGND INTGND HWNMOS  L=800E-9 W=6E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN25 153 146 INTGND INTGND HWNMOS  L=800E-9 W=6E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN28 153 148 INTGND INTGND HWNMOS  L=800E-9 W=6E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
* Q21 152 152 150 INTGND HW4SBDR (ORIG.)
* Q5 INTVCC 152 153 INTGND HW4SBDR  (ORIG.)
Q21 152 152 150 INTGND HW4X1SBSR
Q5 INTVCC 152 153 INTGND HW4X1SBSR
Q6 114 153 INTGND INTGND HW8DBTC
.ENDS PMOSDN

.SUBCKT INV7 128 129 INTVCC INTGND
MQN7 129 128 INTGND INTGND HWNMOS  L=(8E-7) W=(2E-06) AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP8 129 128 INTVCC INTVCC HWPMOS  L=(8E-7) W=(6E-06) AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
.ENDS INV7

.SUBCKT OVRVLT 108 154 140 155 113 148 INTVCC INTGND
XINV_59 156 158 INTVCC INTGND INV7
R2 149 INTGND +5.000E+03
R3 156 159 +5.000E+02
MQP61 140 156 113 113 HWPMOS  L=800E-9 W=6E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP62 148 140 113 113 HWPMOS  L=800E-9 W=40E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP60 160 156 113 113 HWPMOS  L=800E-9 W=10E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP49 156 108 155 113 HWPMOS  L=1.2E-6 W=160E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP55 156 158 113 113 HWPMOS  L=6E-6 W=2E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
C46 155 157 150E-15
MQP44 161 155 INTVCC INTVCC HWPMOS  L=800E-9 W=8E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN67 148 140 INTGND INTGND HWNMOS  L=800E-9 W=24E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN63 140 156 INTGND INTGND HWNMOS  L=800E-9 W=6E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN65 162 160 INTGND INTGND HWNMOS  L=800E-9 W=2E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
```

```
MQN64 140 156 162 INTGND HWNMOS  L=800E-9 W=6E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN66 160 156 INTGND INTGND HWNMOS  L=800E-9 W=2E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN43 161 155 119 INTGND HWNMOS  L=800E-9 W=2E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN47 157 INTVCC INTGND INTGND HWNMOS  L=5E-6 W=2E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN53 159 154 INTGND INTGND HWNMOS  L=10E-6 W=2.5E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN57 159 161 INTGND INTGND HWNMOS  L=800E-9 W=10E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN56 159 158 INTGND INTGND HWNMOS  L=5E-6 W=2E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
* Q42 119 119 INTGND INTGND HW4SBSR (ORIG)
Q42 119 119 INTGND INTGND HW4X1SBSR
Q50 108 157 149 INTGND HW2SBTC
Q31 140 162 INTGND INTGND HW3SBTC
Q30 113 160 140 INTGND HW3SBTC
.ENDS OVRVLT

.SUBCKT OUT1 113 146 147 148 115 117 INTVCC INTGND
XD51 117 113 INTGND HWDS2X45P2
XD52 INTVCC 113 INTGND HWDS2X45P2
XD53 INTVCC 113 INTGND HWDS2X45P2
MQN40 105 147 INTGND INTGND HWNMOS  L=800E-9 W=10E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN41 105 146 INTGND INTGND HWNMOS  L=800E-9 W=10E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN39 115 146 INTGND INTGND HWNMOS  L=800E-9 W=16E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN38 115 147 INTGND INTGND HWNMOS  L=800E-9 W=16E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP42 113 148 INTVCC 113 HWPMOS  L=1E-6 W=20E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP43 113 INTVCC 117 113 HWPMOS  L=1E-6 W=20E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP34 105 147 163 113 HWPMOS  L=800E-9 W=50E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP32 164 147 INTVCC 113 HWPMOS  L=800E-9 W=70E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP35 105 146 164 113 HWPMOS  L=800E-9 W=50E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP33 163 146 INTVCC 113 HWPMOS  L=800E-9 W=70E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
Q11 INTVCC 105 115 INTGND HW10DBTC
.ENDS OUT1

.SUBCKT INV6 128 129 INTVCC INTGND
MQN7 129 128 INTGND INTGND HWNMOS  L=(8E-7) W=(8E-06) AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP8 129 128 INTVCC INTVCC HWPMOS  L=(8E-7) W=(1.2E-05) AD=36E-12 AS=36E-12
+PD=43.6E-6 PS=43.6E-6 M=1
.ENDS INV6
```

```
.SUBCKT INV5 128 129 INTVCC INTGND
MQN7 129 128 INTGND INTGND HWNMOS  L=(8E-7) W=(1.2E-05) AD=36E-12 AS=36E-12
PD=43.6E-6
+PS=43.6E-6 M=1
MQP8 129 128 INTVCC INTVCC HWPMOS  L=(8E-7) W=(1.2E-05) AD=36E-12 AS=36E-12
+PD=43.6E-6 PS=43.6E-6 M=1
.ENDS INV5

.SUBCKT OUT2 165 147 116 117 INTVCC INTGND
XD37 166 117 INTGND HWDS3X8
R0 INTVCC 106 +1.000E+04
MQN34 149 165 INTGND INTGND HWNMOS  L=800E-9 W=5E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN25 149 147 INTGND INTGND HWNMOS  L=800E-9 W=5E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN32 149 151 INTGND INTGND HWNMOS  L=800E-9 W=5E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP24 167 147 106 INTVCC HWPMOS  L=800E-9 W=35E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP23 152 165 167 INTVCC HWPMOS  L=800E-9 W=35E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP22 149 151 152 INTVCC HWPMOS  L=800E-9 W=35E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
XINV_21 144 151 INTVCC INTGND INV5
XINV_20 117 144 INTVCC INTGND INV6
Q12 149 149 166 INTGND HW6DBTC
Q11 INTVCC 149 116 INTGND HW6DBTC
.ENDS OUT2

.SUBCKT INV4 128 129 INTVCC INTGND
MQN7 129 128 INTGND INTGND HWNMOS  L=(8E-7) W=(5E-06) AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP8 129 128 INTVCC INTVCC HWPMOS  L=(8E-7) W=(3E-06) AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
.ENDS INV4

.SUBCKT NOR1 171 172 173 INTVCC INTGND
MQN1 173 171 INTGND INTGND HWNMOS  L=(8E-7) W=(2.5E-05) AD=36E-12 AS=36E-12
PD=43.6E-6
+PS=43.6E-6 M=1
MQN0 173 172 INTGND INTGND HWNMOS  L=(8E-7) W=(2.5E-05) AD=36E-12 AS=36E-12
PD=43.6E-6
+PS=43.6E-6 M=1
MQP1 173 171 149 INTVCC HWPMOS  L=(8E-7) W=(5E-05) AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP0 149 172 INTVCC INTVCC HWPMOS  L=(8E-7) W=(5E-05) AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
.ENDS NOR1
```

```
.SUBCKT OUT3 165 147 116 117 INTVCC INTGND
XDIO_43 105 117 INTGND HWDS3X8
XNOR_42 147 165 168 INTVCC INTGND NOR1
XINV_41 117 118 INTVCC INTGND INV4
MQN36 116 165 INTGND INTGND HWNMOS  L=800E-9 W=40E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN39 105 165 INTGND INTGND HWNMOS  L=800E-9 W=10E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN40 105 147 INTGND INTGND HWNMOS  L=800E-9 W=10E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN35 116 147 INTGND INTGND HWNMOS  L=800E-9 W=40E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
Q33 INTVCC 105 116 INTGND HW10DBTC
MQP31 105 165 169 INTVCC HWPMOS  L=800E-9 W=50E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP25 164 118 INTVCC INTVCC HWPMOS  L=800E-9 W=5E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP28 170 165 164 INTVCC HWPMOS  L=800E-9 W=70E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP26 164 168 INTVCC INTVCC HWPMOS  L=800E-9 W=120E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP30 105 147 170 INTVCC HWPMOS  L=800E-9 W=50E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP27 169 147 164 INTVCC HWPMOS  L=800E-9 W=70E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
.ENDS OUT3
```

LVT16 Berkeley SPICE Models for PSPICE Simulation

```
*****************************************************************************
LVT16PS.CIR
* Low Voltage BiCMOS Logic
* Standard Logic Product Group
* Philips Semiconductors
* 4/8/95
*****************************************************************************
* To simulate a particular device, locate the device in the section of
* this file titled "LVT16 Circuit Models.  Delete the comment mark, "*",
* in the leading column for that device only.  Make sure that the
* comment "*" is present for all other devices on the list.  To simulate
* with nominal, slow, or fast process parameters, go to the section of
* the file with the particular process corner you want and remove the
* "*".  Insure that the other parameters in the set are remarked out
* with the "*" added.  You may also wish to adjust the values of the
* load and parasitic inductors and capacitors as found in the
* LVT16SUB.SPC files according to the package chosen.  The basic files
* use nominal values.
*****************************************************************************
* Common Models for Nominal, Slow and Fast
* (Do not comment out this INCLUDE line)
.INCLUDE "C:\SPICE\LVT16\PSPICE\LVT16SUB.SPC"

*** LVT16 Circuit Models

* CHOOSE ONE & ONLY ONE DEVICE PARAMETER SET

* Nominal Parameters
.INCLUDE "C:\SPICE\LVT16\PSPICE\LVT16NOM.SPC"

* Slow Parameters
* .INCLUDE "C:\SPICE\LVT16\PSPICE\LVT16SLO.SPC"

* Fast Parameters
* .INCLUDE "C:\SPICE\LVT16\PSPICE\LVT16FAS.SPC"

*CHOOSE ONE & ONLY ONE PART FOR EACH SIMULATION

* Part Type    In  En  Enb  Out  Vcc  Subcircuit Name
* XL240A       5   7   9    4    100  INV1
* XL240A_1     5   7   9    4    100  INV1_1
XL244B       5   7   9    4    100  NINV1
* XL244B_1     5   7   9    4    100  NINV1_1
* XL245B       5   7   9    4    100  NINV1
* XL245B_1     5   7   9    4    100  NINV1_1
* XL373A       5   7   9    4    100  NINV1
* XL374A       5   7   9    4    100  NINV1
* XL500A       5   7   9    4    100  NINV1
* XL501A       5   7   9    4    100  NINV1
* XL543A       5   7   9    4    100  NINV1
* XL646A       5   7   9    4    100  NINV1
* XL652A       5   7   9    4    100  NINV1
```

```
* EXTERNAL LOAD
R10 4 0 500
C10 4 0 50PF

* POWER
VCC 100 0 3.3

* DRIVE
VIN 5 0 PULSE 0.0 3.3 2N 2.5N 2.5N 10N 25N
VOE 7 0 3.3
VOEB 9 0 0.0

.TRAN   1N  25N  ; 0 1P
.OPTIONS ITL4=50
.TEMP  25
.PROBE
.END
```

LVT16SUB.SPC Subcircuit

```
*****************************************************************************
* LVT16 PSPICE SUBCIRCUIT LIBRARY
* LVT16SUB.SPC
* STANDARD PRODUCT LOGIC GROUP
* PHILIPS SEMICONDUCTORS
* 4/8/1995
*****************************************************************************
.SUBCKT NINV1 D E EB Q VCC
* USE THIS MODEL FOR 74LVT16244  -  245  -  373  -  374  -  500  -  501
*                                -  543  -  646  -  652
L1 111 Q 6N
L2 VCC 99 6N
L3 6 0 6N
L4 D 101 6N
L5 E 109 6N
L6 EB 110 6N
C1 111 0 1.5P
C2 99 0 1.5P
C3 6 0 1.5P
C4 101 0 1.5P
C5 109 0 1.5P
C6 110 0 1.5P
X0 101 99 6 BUSHOLD
X1 102 103 104 105 106 107 99 6 OUTD
X2 108 101 109 102 110 103 104 105 106 99 6 IOCL
X3 108 99 6 BIAS
XESD_15 111 6 ESD
XESD_16 101 6 ESD
R14 106 111 0.001
R13 107 111 0.001
.ENDS NINV1

.SUBCKT NINV1_1 D E EB Q VCC
* USE THIS MODEL FOR 74LVT16244-1  --  245-1
L1 111 Q 6N
L2 VCC 99 6N
L3 6 0 6N
L4 D 101 6N
L5 E 109 6N
L6 EB 110 6N
C1 111 0 1.5P
C2 99 0 1.5P
C3 6 0 1.5P
C4 101 0 1.5P
C5 109 0 1.5P
C6 110 0 1.5P
X0 101 99 6 BUSHOLD
X1 102 103 104 105 106 107 99 6 OUTD
X2 108 101 109 102 110 103 104 105 106 99 6 IOCL
X3 108 99 6 BIAS
XESD_15 111 6 ESD
XESD_16 101 6 ESD
R14 106 111 22.5
R13 107 111 22.5
.ENDS NINV1_1
```

```
.SUBCKT INV1 D E EB Q VCC
* USE THIS MODEL FOR 74LVT16240
L1 111 Q 6N
L2 VCC 99 6N
L3 6 0 6N
L4 D 101 6N
L5 E 109 6N
L6 EB 110 6N
C1 111 0 1.5P
C2 99 0 1.5P
C3 6 0 1.5P
C4 101 0 1.5P
C5 109 0 1.5P
C6 110 0 1.5P
X0 101 99 6 BUSHOLD
X1 102 103 104 105 106 107 99 6 OUTD
X2 108 151 109 102 110 103 104 105 106 99 6 IOCL
X3 108 99 6 BIAS
X4 101 151 99 6 INV20
XESD_15 111 6 ESD
XESD_16 101 6 ESD
R14 106 111 0.0
R13 107 111 0.0
.ENDS INV1

.SUBCKT INV1_1 D E EB Q VCC
* USE THIS MODEL FOR 74LVT16240-1
L1 111 Q 6N
L2 VCC 99 6N
L3 6 0 6N
L4 D 101 6N
L5 E 109 6N
L6 EB 110 6N
C1 111 0 1.5P
C2 99 0 1.5P
C3 6 0 1.5P
C4 101 0 1.5P
C5 109 0 1.5P
C6 110 0 1.5P
X0 101 99 6 BUSHOLD
X1 102 103 104 105 106 107 99 6 OUTD
X2 108 151 109 102 110 103 104 105 106 99 6 IOCL
X3 108 99 6 BIAS
X4 101 151 99 6 INV20
XESD_15 111 6 ESD
XESD_16 101 6 ESD
R14 106 111 22.5
R13 107 111 22.5
.ENDS INV1_1
*
.SUBCKT ESD 112 INTGND
Q10 112 INTGND INTGND INTGND HWESDLGC
.ENDS ESD
.SUBCKT BIAS 108 INTVCC INTGND
XD4 INTVCC 108 INTGND HWDS2X45P2
C4 INTVCC 108 4P
R5 INTVCC 108 4K
R4 108 INTGND 108K
.ENDS BIAS
```

```
.SUBCKT INV20 128 129 INTVCC INTGND
MQN7 129 128 INTGND INTGND HWNMOS  L=(8E-07) W=(6.5E-05) AD=36E-12 AS=36E-12
PD=43.6E-6
+PS=43.6E-6 M=1
MQP8 129 128 INTVCC INTVCC HWPMOS  L=(8E-07) W=(0.00014) AD=36E-12 AS=36E-12
+PD=43.6E-6 PS=43.6E-6 M=1
.ENDS INV20

.SUBCKT INV13 128 129 INTVCC INTGND
MQN7 129 128 INTGND INTGND HWNMOS  L=(8E-07) W=(6.5E-05) AD=36E-12 AS=36E-12
PD=43.6E-6
+PS=43.6E-6 M=1
MQP8 129 128 INTVCC INTVCC HWPMOS  L=(8E-07) W=(0.00014) AD=36E-12 AS=36E-12
+PD=43.6E-6 PS=43.6E-6 M=1
.ENDS INV13

.SUBCKT INV12 128 129 INTVCC INTGND
MQN7 129 128 INTGND INTGND HWNMOS  L=(8E-07) W=(8E-05) AD=36E-12 AS=36E-12
PD=43.6E-6
+PS=43.6E-6 M=1
MQP8 129 128 INTVCC INTVCC HWPMOS  L=(8E-07) W=(5E-05) AD=36E-12 AS=36E-12
+PD=43.6E-6 PS=43.6E-6 M=1
.ENDS INV12

.SUBCKT INV11 128 129 INTVCC INTGND
MQN7 129 128 INTGND INTGND HWNMOS  L=(8E-07) W=(2E-05) AD=36E-12 AS=36E-12
PD=43.6E-6
+PS=43.6E-6 M=1
MQP8 129 128 INTVCC INTVCC HWPMOS  L=(8E-07) W=(3E-05) AD=36E-12 AS=36E-12
+PD=43.6E-6 PS=43.6E-6 M=1
.ENDS INV11

.SUBCKT INV10 128 129 INTVCC INTGND
MQN7 129 128 INTGND INTGND HWNMOS  L=(8E-07) W=(2E-06) AD=36E-12 AS=36E-12
PD=43.6E-6
+PS=43.6E-6 M=1
MQP8 129 128 INTVCC INTVCC HWPMOS  L=(8E-07) W=(4E-06) AD=36E-12 AS=36E-12
+PD=43.6E-6 PS=43.6E-6 M=1
.ENDS INV10

.SUBCKT INV9 128 129 INTVCC INTGND
MQN7 129 128 INTGND INTGND HWNMOS  L=(8E-07) W=(1E-05) AD=36E-12 AS=36E-12
PD=43.6E-6
+PS=43.6E-6 M=1
MQP8 129 128 INTVCC INTVCC HWPMOS  L=(8E-07) W=(2E-05) AD=36E-12 AS=36E-12
+PD=43.6E-6 PS=43.6E-6 M=1
.ENDS INV9
```

```
.SUBCKT IOCL 108 101 109 113 110 114 115 116 117 INTVCC INTGND
R102 117 123 +3.000E+02
R103 117 123 +3.000E+02
XINV_99 122 119 INTVCC INTGND INV9
X10 122 124 INTVCC INTGND INV10
X11 122 118 INTVCC INTGND INV11
X12 122 118 INTVCC INTGND INV12
X13 101 122 INTVCC INTGND INV13
X14 118 110 116 117 INTVCC INTGND OUT3
X15 118 110 116 117 INTVCC INTGND OUT2
X16 113 122 110 121 115 117 INTVCC INTGND OUT1
X17 108 109 120 117 113 121 INTVCC INTGND OVRVLT
X18 122 110 121 114 INTVCC INTGND PMOSDN
X19 119 109 120 113 114 INTVCC INTGND PMOSUP
* MQP44 125 INTGND 126 INTVCC HWPMOS  L=800E-9 W=140E-6 AD=252E-12 AS=252E-12
* +PD=283.6E-6 PS=283.6E-6 M=1  (ORIG.)
MQP44 125 INTGND INTVCC INTVCC HWPMOS  L=800E-9 W=140E-6 AD=252E-12 AS=252E-12
+PD=283.6E-6 PS=283.6E-6 M=1
MQP42 INTGND INTGND 125 INTVCC HWPMOS  L=800E-9 W=65E-6 AD=117E-12 AS=117E-12
PD=133.6E-6
+PS=133.6E-6 M=1
MQN100 119 122 INTGND INTGND HWNMOS  L=800E-9 W=25E-6 AD=45E-12 AS=45E-12 PD=53.6E-6
+PS=53.6E-6 M=1
MQN127 122 124 INTGND INTGND HWNMOS  L=800E-9 W=8E-6 AD=14.4E-12 AS=14.4E-12
PD=19.6E-6
+PS=19.6E-6 M=1
MQN109 118 122 INTGND INTGND HWNMOS  L=800E-9 W=10E-6 AD=18E-12 AS=18E-12 PD=23.6E-6
+PS=23.6E-6 M=1
MQN104 123 122 127 INTGND HWNMOS  L=1E-6 W=50E-6 AD=90E-12 AS=90E-12 PD=103.6E-6
+PS=103.6E-6 M=1
MQN105 127 109 INTGND INTGND HWNMOS  L=1E-6 W=50E-6 AD=90E-12 AS=90E-12 PD=103.6E-6
+PS=103.6E-6 M=1
.ENDS IOCL

.SUBCKT OUTD 113 114 115 116 130 131 INTVCC INTGND
XD48 INTVCC 132 INTGND HWDS2X45P2
XD46 INTVCC 132 INTGND HWDS2X45P2
XD47 INTVCC 132 INTGND HWDS2X45P2
XD49 INTVCC 132 INTGND HWDS2X45P2
XD50 INTVCC 132 INTGND HWDS2X45P2
MQP38 131 114 INTVCC 113 HWPMOS  L=1E-6 W=1E-3 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP39 115 114 INTVCC 113 HWPMOS  L=800E-9 W=100E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
RBNR37 132 133 5.0
R1 116 INTGND +1.000E+04
Q29 130 116 INTGND INTGND HW40SBTCNW
Q27 133 115 131 INTGND HW40SBTCNW
Q28 130 116 INTGND INTGND HW40SBTCNW
Q30 130 116 INTGND INTGND HW40SBTCNW
Q26 133 115 131 INTGND HW40SBTCNW
Q31 130 116 INTGND INTGND HW40SBTCNW
.ENDS OUTD
```

```
.SUBCKT INV21 128 129 INTVCC INTGND
MQN7 129 128 INTGND INTGND HWNMOS  L=(1E-06) W=(2E-06) AD=36E-12 AS=36E-12
PD=43.6E-6
+PS=43.6E-6 M=1
MQP8 129 128 INTVCC INTVCC HWPMOS  L=(1E-06) W=(4E-06) AD=36E-12 AS=36E-12
+PD=43.6E-6 PS=43.6E-6 M=1
.ENDS INV21

.SUBCKT BUSHOLD 134 INTVCC INTGND
XINV_18 134 135 INTVCC INTGND INV21
MQN17 136 135 INTGND INTGND HWNMOS  L=1E-6 W=3E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP16 137 135 INTVCC INTVCC HWPMOS  L=1E-6 W=14E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
XDIO_15 137 104 INTGND HWDS3X8
R0 104 134 +2.000E+03
R1 134 136 +4.000E+03
.ENDS BUSHOLD

.SUBCKT PMOSUP 138 139 140 113 114 INTVCC INTGND
XD50 INTVCC 141 INTGND HWDS3X23
MQP38 114 140 113 113 HWPMOS  L=800E-9 W=50E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP40 114 138 113 113 HWPMOS  L=800E-9 W=20E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP39 114 139 113 113 HWPMOS  L=800E-9 W=20E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN37 142 138 INTGND INTGND HWNMOS  L=800E-9 W=8E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN36 143 139 142 INTGND HWNMOS  L=800E-9 W=8E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN34 144 140 INTGND INTGND HWNMOS  L=800E-9 W=10E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN33 118 139 144 INTGND HWNMOS  L=800E-9 W=10E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN35 114 140 143 INTGND HWNMOS  L=800E-9 W=8E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN32 145 138 118 INTGND HWNMOS  L=800E-9 W=10E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP29 145 138 INTVCC INTVCC HWPMOS  L=800E-9 W=30E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP30 145 139 INTVCC INTVCC HWPMOS  L=800E-9 W=30E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP31 145 140 INTVCC INTVCC HWPMOS  L=800E-9 W=20E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
Q5 141 145 114 INTGND HW8DBTC
.ENDS PMOSUP

.SUBCKT INV8 128 129 INTVCC INTGND
MQN7 129 128 INTGND INTGND HWNMOS  L=(8E-7) W=(2E-05) AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP8 129 128 INTVCC INTVCC HWPMOS  L=(8E-7) W=(8E-06) AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
.ENDS INV8
```

```
.SUBCKT PMOSDN 146 147 148 114 INTVCC INTGND
XINV_36 114 149 INTVCC INTGND INV8
XDIO_35 150 114 INTGND HWDS3X8
MQP29 104 148 INTVCC INTVCC HWPMOS  L=800E-9 W=20E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP30 151 149 104 INTVCC HWPMOS  L=800E-9 W=20E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP31 103 147 151 INTVCC HWPMOS  L=800E-9 W=20E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP32 152 146 103 INTVCC HWPMOS  L=800E-9 W=20E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN24 152 146 INTGND INTGND HWNMOS  L=800E-9 W=6E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN23 152 148 INTGND INTGND HWNMOS  L=800E-9 W=6E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN26 152 147 INTGND INTGND HWNMOS  L=800E-9 W=6E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN27 153 147 INTGND INTGND HWNMOS  L=800E-9 W=6E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN25 153 146 INTGND INTGND HWNMOS  L=800E-9 W=6E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN28 153 148 INTGND INTGND HWNMOS  L=800E-9 W=6E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
* Q21 152 152 150 INTGND HW4SBDR (ORIG.)
* Q5 INTVCC 152 153 INTGND HW4SBDR  (ORIG.)
Q21 152 152 150 INTGND HW4X1SBSR
Q5 INTVCC 152 153 INTGND HW4X1SBSR
Q6 114 153 INTGND INTGND HW8DBTC
.ENDS PMOSDN

.SUBCKT INV7 128 129 INTVCC INTGND
MQN7 129 128 INTGND INTGND HWNMOS  L=(8E-7) W=(2E-06) AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP8 129 128 INTVCC INTVCC HWPMOS  L=(8E-7) W=(6E-06) AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
.ENDS INV7

.SUBCKT OVRVLT 108 154 140 155 113 148 INTVCC INTGND
XINV_59 156 158 INTVCC INTGND INV7
R2 149 INTGND +5.000E+03
R3 156 159 +5.000E+02
MQP61 140 156 113 113 HWPMOS  L=800E-9 W=6E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP62 148 140 113 113 HWPMOS  L=800E-9 W=40E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP60 160 156 113 113 HWPMOS  L=800E-9 W=10E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP49 156 108 155 113 HWPMOS  L=1.2E-6 W=160E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP55 156 158 113 113 HWPMOS  L=6E-6 W=2E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
C46 155 157 150E-15
MQP44 161 155 INTVCC INTVCC HWPMOS  L=800E-9 W=8E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN67 148 140 INTGND INTGND HWNMOS  L=800E-9 W=24E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN63 140 156 INTGND INTGND HWNMOS  L=800E-9 W=6E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
```

```
MQN65 162 160 INTGND INTGND HWNMOS  L=800E-9 W=2E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN64 140 156 162 INTGND HWNMOS  L=800E-9 W=6E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN66 160 156 INTGND INTGND HWNMOS  L=800E-9 W=2E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN43 161 155 119 INTGND HWNMOS  L=800E-9 W=2E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN47 157 INTVCC INTGND INTGND HWNMOS  L=5E-6 W=2E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN53 159 154 INTGND INTGND HWNMOS  L=10E-6 W=2.5E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN57 159 161 INTGND INTGND HWNMOS  L=800E-9 W=10E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN56 159 158 INTGND INTGND HWNMOS  L=5E-6 W=2E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
* Q42 119 119 INTGND INTGND HW4SBSR (ORIG)
Q42 119 119 INTGND INTGND HW4X1SBSR
Q50 108 157 149 INTGND HW2SBTC
Q31 140 162 INTGND INTGND HW3SBTC
Q30 113 160 140 INTGND HW3SBTC
.ENDS OVRVLT

.SUBCKT OUT1 113 146 147 148 115 117 INTVCC INTGND
XD51 117 113 INTGND HWDS2X45P2
XD52 INTVCC 113 INTGND HWDS2X45P2
XD53 INTVCC 113 INTGND HWDS2X45P2
MQN40 105 147 INTGND INTGND HWNMOS  L=800E-9 W=10E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN41 105 146 INTGND INTGND HWNMOS  L=800E-9 W=10E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN39 115 146 INTGND INTGND HWNMOS  L=800E-9 W=16E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN38 115 147 INTGND INTGND HWNMOS  L=800E-9 W=16E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
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+PS=43.6E-6 M=1
MQP43 113 INTVCC 117 113 HWPMOS  L=1E-6 W=20E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP34 105 147 163 113 HWPMOS  L=800E-9 W=50E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP32 164 147 INTVCC 113 HWPMOS  L=800E-9 W=70E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP35 105 146 164 113 HWPMOS  L=800E-9 W=50E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP33 163 146 INTVCC 113 HWPMOS  L=800E-9 W=70E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
Q11 INTVCC 105 115 INTGND HW10DBTC
.ENDS OUT1

.SUBCKT INV6 128 129 INTVCC INTGND
MQN7 129 128 INTGND INTGND HWNMOS  L=(8E-7) W=(8E-06) AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP8 129 128 INTVCC INTVCC HWPMOS  L=(8E-7) W=(1.2E-05) AD=36E-12 AS=36E-12
+PD=43.6E-6 PS=43.6E-6 M=1
.ENDS INV6
```

```
.SUBCKT INV5 128 129 INTVCC INTGND
MQN7 129 128 INTGND INTGND HWNMOS  L=(8E-7) W=(1.2E-05) AD=36E-12 AS=36E-12
PD=43.6E-6
+PS=43.6E-6 M=1
MQP8 129 128 INTVCC INTVCC HWPMOS  L=(8E-7) W=(1.2E-05) AD=36E-12 AS=36E-12
+PD=43.6E-6 PS=43.6E-6 M=1
.ENDS INV5

.SUBCKT OUT2 165 147 116 117 INTVCC INTGND
XD37 166 117 INTGND HWDS3X8
R0 INTVCC 106 +1.000E+04
MQN34 149 165 INTGND INTGND HWNMOS  L=800E-9 W=5E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN25 149 147 INTGND INTGND HWNMOS  L=800E-9 W=5E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN32 149 151 INTGND INTGND HWNMOS  L=800E-9 W=5E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP24 167 147 106 INTVCC HWPMOS  L=800E-9 W=35E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP23 152 165 167 INTVCC HWPMOS  L=800E-9 W=35E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP22 149 151 152 INTVCC HWPMOS  L=800E-9 W=35E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
XINV_21 144 151 INTVCC INTGND INV5
XINV_20 117 144 INTVCC INTGND INV6
Q12 149 149 166 INTGND HW6DBTC
Q11 INTVCC 149 116 INTGND HW6DBTC
.ENDS OUT2

.SUBCKT INV4 128 129 INTVCC INTGND
MQN7 129 128 INTGND INTGND HWNMOS  L=(8E-7) W=(5E-06) AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP8 129 128 INTVCC INTVCC HWPMOS  L=(8E-7) W=(3E-06) AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
.ENDS INV4

.SUBCKT NOR1 171 172 173 INTVCC INTGND
MQN1 173 171 INTGND INTGND HWNMOS  L=(8E-7) W=(2.5E-05) AD=36E-12 AS=36E-12
PD=43.6E-6
+PS=43.6E-6 M=1
MQN0 173 172 INTGND INTGND HWNMOS  L=(8E-7) W=(2.5E-05) AD=36E-12 AS=36E-12
PD=43.6E-6
+PS=43.6E-6 M=1
MQP1 173 171 149 INTVCC HWPMOS  L=(8E-7) W=(5E-05) AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP0 149 172 INTVCC INTVCC HWPMOS  L=(8E-7) W=(5E-05) AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
.ENDS NOR1
```

```
.SUBCKT OUT3 165 147 116 117 INTVCC INTGND
XDIO_43 105 117 INTGND HWDS3X8
XNOR_42 147 165 168 INTVCC INTGND NOR1
XINV_41 117 118 INTVCC INTGND INV4
MQN36 116 165 INTGND INTGND HWNMOS  L=800E-9 W=40E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN39 105 165 INTGND INTGND HWNMOS  L=800E-9 W=10E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN40 105 147 INTGND INTGND HWNMOS  L=800E-9 W=10E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQN35 116 147 INTGND INTGND HWNMOS  L=800E-9 W=40E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
Q33 INTVCC 105 116 INTGND HW10DBTC
MQP31 105 165 169 INTVCC HWPMOS  L=800E-9 W=50E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP25 164 118 INTVCC INTVCC HWPMOS  L=800E-9 W=5E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP28 170 165 164 INTVCC HWPMOS  L=800E-9 W=70E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP26 164 168 INTVCC INTVCC HWPMOS  L=800E-9 W=120E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP30 105 147 170 INTVCC HWPMOS  L=800E-9 W=50E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
MQP27 169 147 164 INTVCC HWPMOS  L=800E-9 W=70E-6 AD=36E-12 AS=36E-12 PD=43.6E-6
+PS=43.6E-6 M=1
.ENDS OUT3
```

Section 6
LVC

SPICE

CONTENTS

Each LVC device requires some combination of one or two input stages, an output stage, possibly one or two inverting stages, possibly a NAND stage, and some package parasitics. Table 6-1 shows LVC model combinations that correlate input, inverting, AND, NAND, and output structures for each part type. Dashes indicate that a particular stage is not needed.

Table 6-1. LVC Model Combinations

LVC	Input Circuit	Inverter Circuit	NAND Circuit	Output Circuit	Inverting Output	Subcircuit Name
00	LVCINPA	LVCINVA	–	LVCOUT2	Yes	INVERT
02	LVCINPA	LVCINVA	–	LVCOUT2	Yes	INVERT
04	LVCINPA	LVCINVA	–	LVCOUT2	Yes	INVERT
08	LVCINPA	LVCINVA/INV1	–	LVCOUT2	No	INVERTN
32	LVCINPA	LVCINVA/INV1	–	LVCOUT2	No	INVERTN
38	LVCINPA	LVCINVA/INV1	–	LVCOUTB	Yes	INVERT4
74	LVCINPA	LVCINVA/INV1	–	LVCOUT2	No	INVERTN
86	LVCINPA	LVCINVA/INV1	–	LVCOUT2	No	INVERTN
109	LVCINPA	LVCINVA	–	LVCOUT2	Yes	INVERT
125	LVCINPA	LVCINVA	–	LVCOUTA	No	INVERT3N
137	2–LVCINPA	–	LVCNAND	LVCOUT2	Yes	NANDINVN
138	2–LVCINPA	–	LVCNAND	LVCOUT2	Yes	NANDINVN
139	2–LVCINPA	–	LVCNAND	LVCOUT2	Yes	NANDINVN
157	2–LVCINPA	LVCINVA/INV1	LVCAND	LVCOUT2	No	ANDINVN
240	LVCINPA	LVCINVA/INV1	–	LVCOUTA	Yes	INVERT3
241	LVCINPA	LVCINVA	–	LVCOUTA	No	INVERT3N
244	LVCINPA	LVCINVA	–	LVCOUTA	No	INVERT3N
245	LVCINPA	LVCINVA	–	LVCOUTA	No	INVERT3N
373	LVCINPA	LVCINVA	–	LVCOUTA	No	INVERT3N
374	LVCINPA	LVCINVA	–	LVCOUTA	No	INVERT3N
543	LVCINPA	LVCINVA	–	LVCOUTA	No	INVERT3N
544	LVCINPA	LVCINVA/INV1	–	LVCOUTA	Yes	INVERT3
573	LVCINPA	LVCINVA	–	LVCOUTA	No	INVERT3N
574	LVCINPA	LVCINVA	–	LVCOUTA	No	INVERT3N
623	LVCINPA	LVCINVA	–	LVCOUTA	No	INVERT3N
646	LVCINPA	LVCINVA	–	LVCOUTA	No	INVERT3N
652	LVCINPA	LVCINVA	–	LVCOUTA	No	INVERT3N
821	LVCINPA	LVCINVA	–	LVCOUTA	No	INVERT3N
823	LVCINPA	LVCINVA	–	LVCOUTA	No	INVERT3N
827	LVCINPA	LVCINVA	–	LVCOUTA	No	INVERT3N
841	LVCINPA	LVCINVA	–	LVCOUTA	No	INVERT3N
2952	LVCINPA	LVCINVA	–	LVCOUTA	No	INVERT3N
4245	LVCINPA	LVCINVA	–	LVCOUTA	No	INVERT3N

The data sheet section provides information on each LVC part type. Each data sheet contains a part description, part features, quick reference data, ordering information, pin configuration, logic symbol, and function table.

To do simulations on a particular part type, refer to the LVC Netlists section of the book. That section contains a file called "LVC.CIR" that contains simulation test circuits for individual device types. The file is also in the LVC directory in the attached diskette, and it is written in the Berkeley SPICE format only. Figures 6-1 through 6-5 show examples of how the test circuits are assembled.

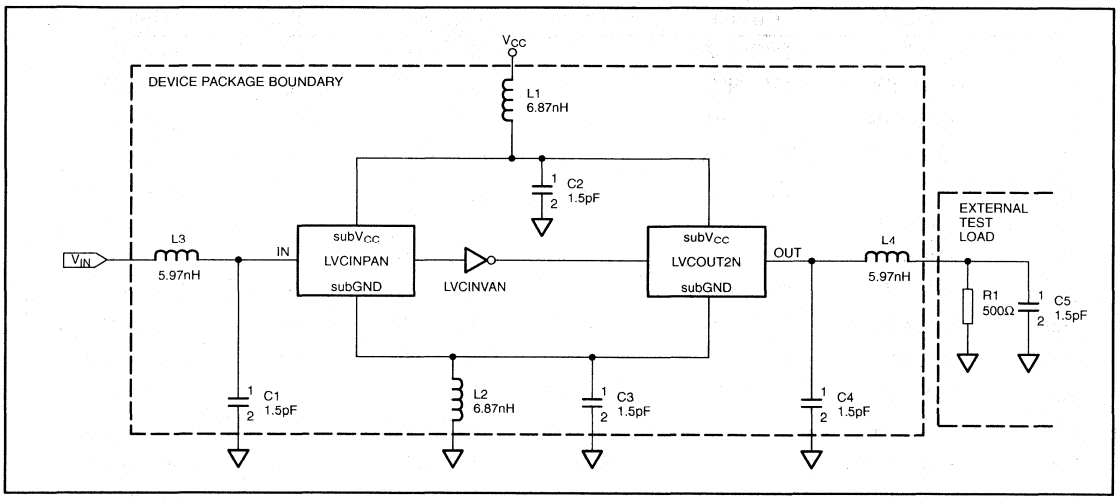


Figure 6-1. 74LVC00 Test Circuit

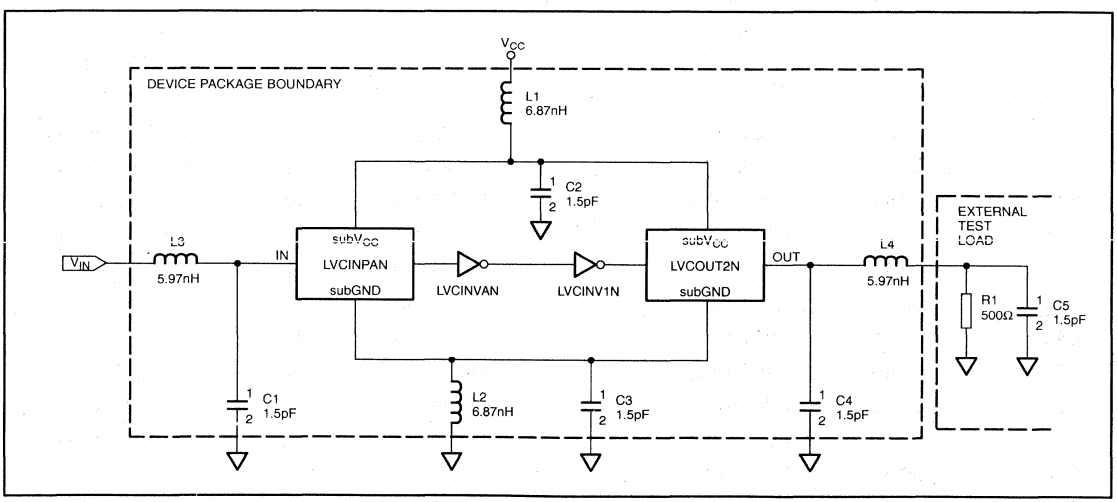


Figure 6-2. 74LVC08 Test Circuit

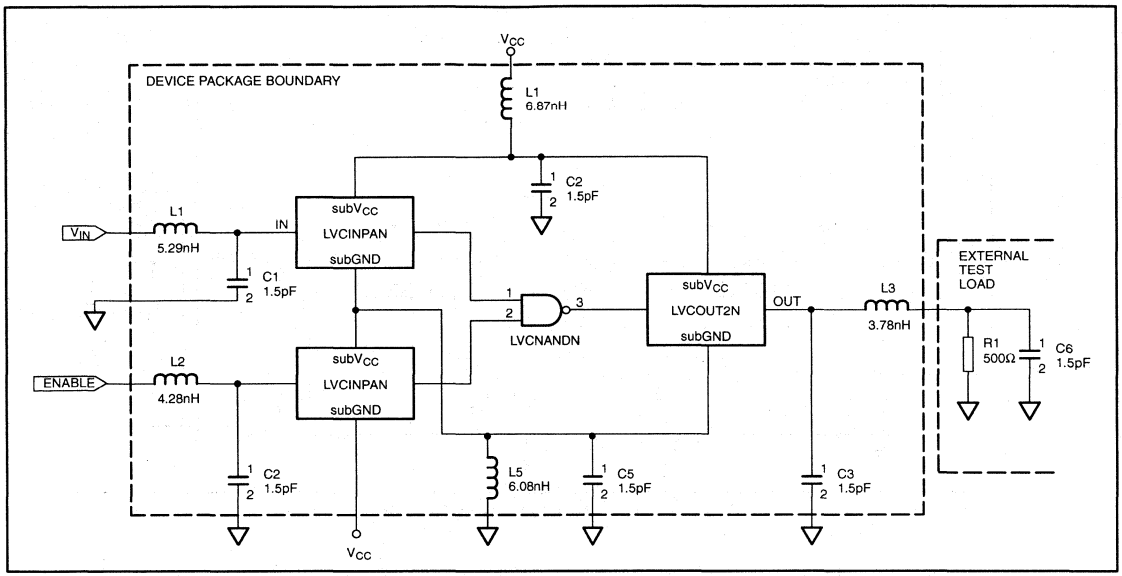


Figure 6-3. 74LVC138 Test Circuit

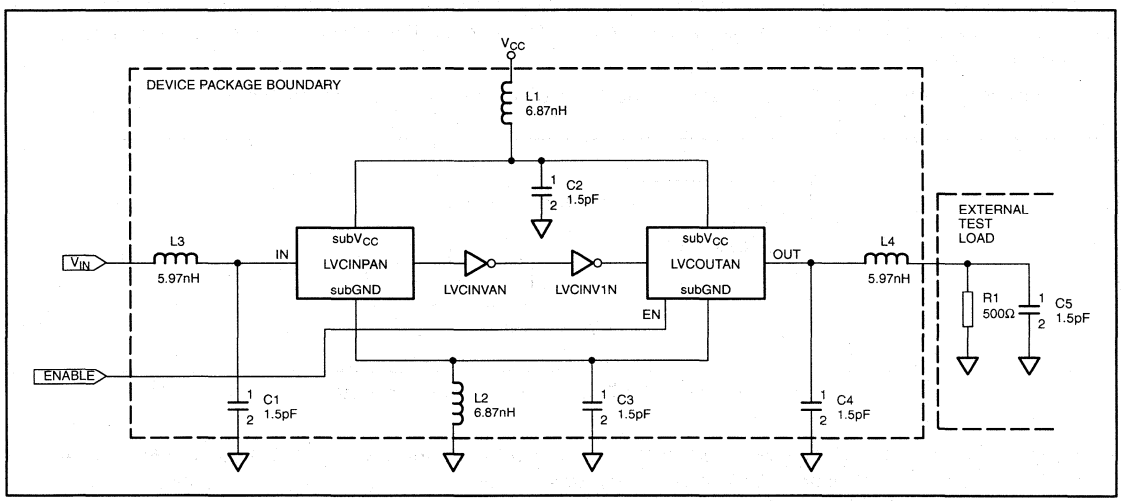


Figure 6-4. 74LVC240 Test Circuit

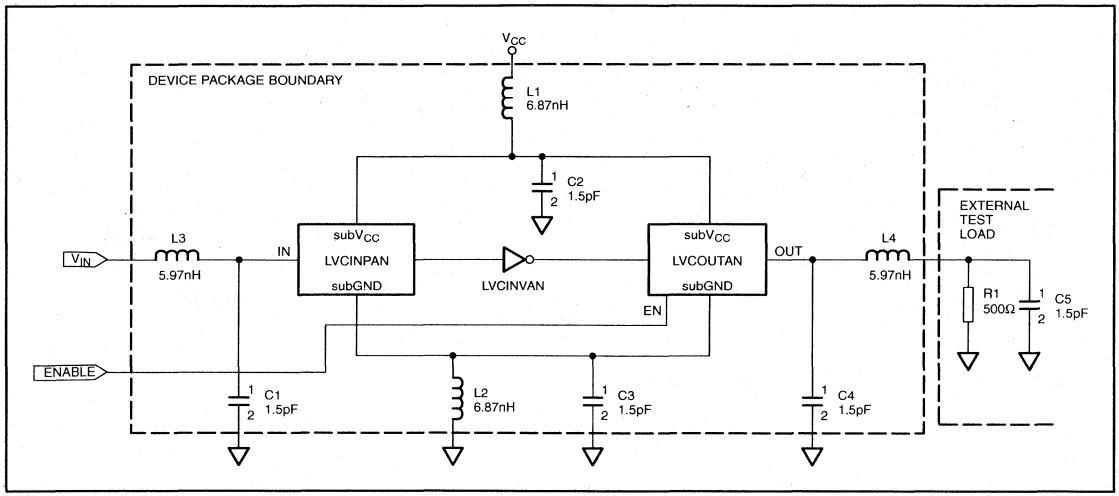


Figure 6-5. 74LVC241 Test Circuit

Also in the LVC Netlists section of the book and in the LVC directory of the diskette are files for subcircuits and primitive elements, such as transistors, diodes, and resistors. These files are called LVCXXXX.CIR, the "XXXX" standing for NOMI, FAST, and SLOW, representing the nominal, fast, and slow process corners. The files contain the subcircuits for input, output, and inverter circuits, and they also have package parasitics connected to simulate a device in a package. Package parasitic values can be changed to suit the application. See the Packaging section of the book for values.

For clarification, the following illustration shows how the two programs interact with each other:

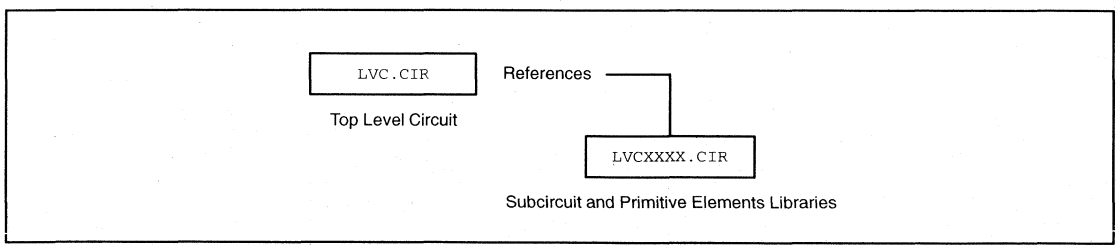


Figure 6-6. LVC SPICE Program Hierarchy

The top level program, LVC.CIR, uses an AC test set-up with a 3V square wave input, 5ns delay, 2.5ns rise and fall times, 40ns pulse width, 70ns period, 3V V_{CC}, 3V applied to the output enable, and a 500Ω, 50pF load. These conditions may be modified to suit the application. Also, the ".INC" command that specifies the path to reference the other program should be modified to reflect your disk directory structure.

LVC Short-form Datasheets

Quad 2-input NAND gate | 74LVC00

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels

DESCRIPTION

The 74LVC00 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC00 provides the 2-input NAND function.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL} t_{PLH}	Propagation delay nA, nB to nY	C_L = 50pF; V_{CC} = 3.3V	3.3	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1, 2	50	pF

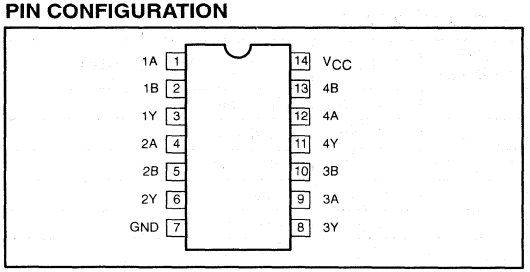
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC00D	14	SO	Plastic	SO14/SOT108A
74LVC00DB	14	SSOP	Plastic	SSOP14/SOT337
74LVC00PW	14	TSSOP	Plastic	TSSOP14/SOT402

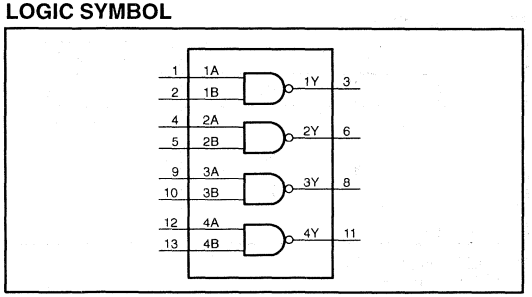
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A – 4A	Data inputs
2, 5, 10, 13	1B – 4B	Data inputs
3, 6, 8, 11	1Y – 4Y	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

Quad 2-input NOR gate | 74LVC02

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels

DESCRIPTION

The 74LVC02 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC02 provides the 2-input NOR function.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL} t_{PLH}	Propagation delay nA, nB to nY	C_L = 50pF; V_{CC} = 3.3V	3.3	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1, 2	60	pF

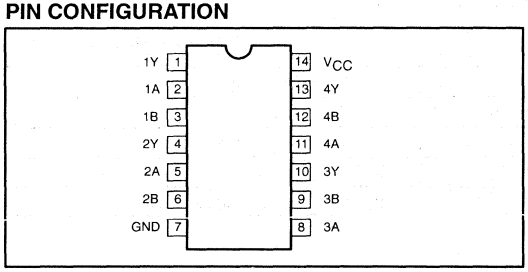
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC02D	14	SO	Plastic	SO14/SOT108A
74LVC02DB	14	SSOP	Plastic	SSOP14/SOT337
74LVC02PW	14	TSSOP	Plastic	TSSOP14/SOT402

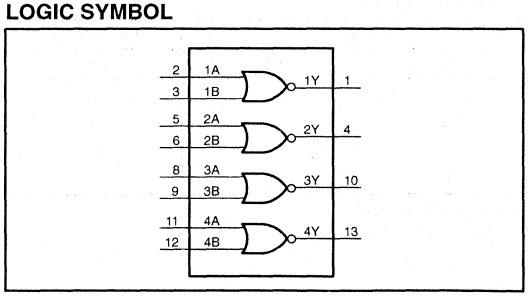
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 5, 8, 11	1A – 4A	Data inputs
3, 6, 9, 12	1B – 4B	Data inputs
1, 4, 10, 13	1Y – 4Y	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	L

H = High voltage level
L = Low voltage level

Hex inverter | 74LVC04

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels

DESCRIPTION

The 74LVC04 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC04 provides six inverting buffers.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL} t_{PLH}	Propagation delay nA, nB to nY	C_L = 50pF; V_{CC} = 3.3V	3.3	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1, 2	45	pF

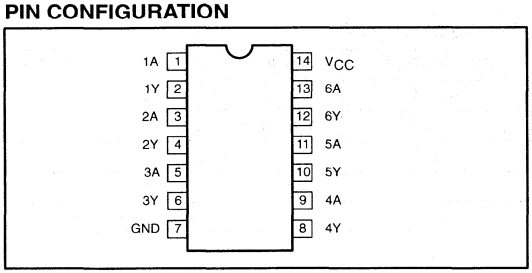
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC04D	14	SO	Plastic	SO14/SOT108A
74LVC04DB	14	SSOP	Plastic	SSOP14/SOT337
74LVC04PW	14	TSSOP	Plastic	TSSOP14/SOT402

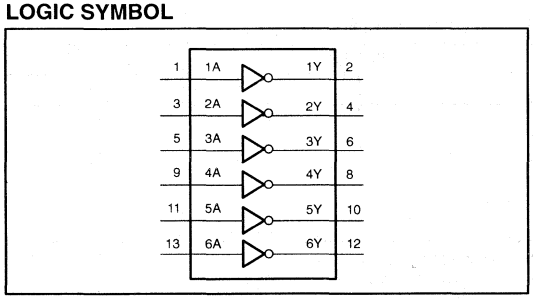
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A – 6A	Data inputs
2, 4, 6, 8, 10, 12	1Y – 6Y	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUTS	OUTPUTS
nA	nY
L	H
H	L

H = High voltage level
L = Low voltage level

Hex inverter | 74LVC08

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels

DESCRIPTION

The 74LVC08 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC08 provides the 2-input AND function

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL} t_{PLH}	Propagation delay nA, nB to nY	C_L = 50pF; V_{CC} = 3.3V	3.3	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1, 2	50	pF

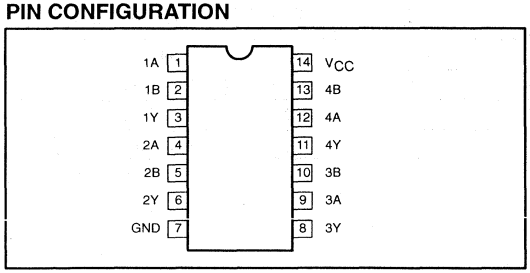
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC08D	14	SO	Plastic	SO14/SOT108A
74LVC08DB	14	SSOP	Plastic	SSOP14/SOT337
74LVC08PW	14	TSSOP	Plastic	TSSOP14/SOT402

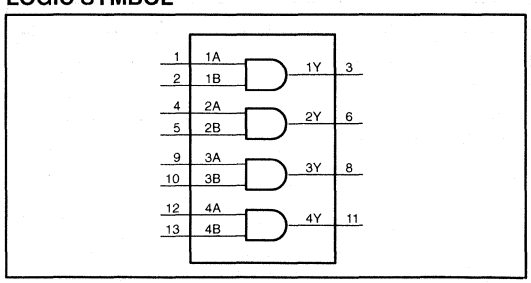
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A – 4A	Data inputs
2, 5, 10, 13	1B – 4B	Data inputs
3, 6, 8, 11	1Y – 4Y	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

H = High voltage level
L = Low voltage level

Quad 2-input OR gate 74LVC32

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels

DESCRIPTION

The 74LVC32 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC32 provides the 2-input OR function.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL} t_{PLH}	Propagation delay nA, nB to nY	C_L = 50pF; V_{CC} = 3.3V	3.3	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1, 2	50	pF

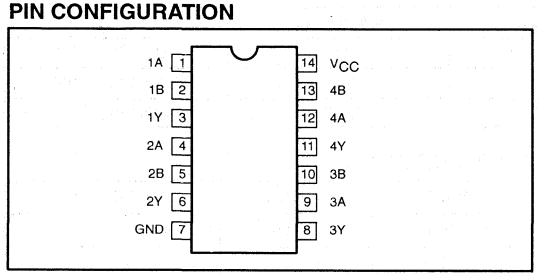
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC32D	14	SO	Plastic	SO14/SOT108A
74LVC32DB	14	SSOP	Plastic	SSOP14/SOT337
74LVC32PW	14	TSSOP	Plastic	TSSOP14/SOT402

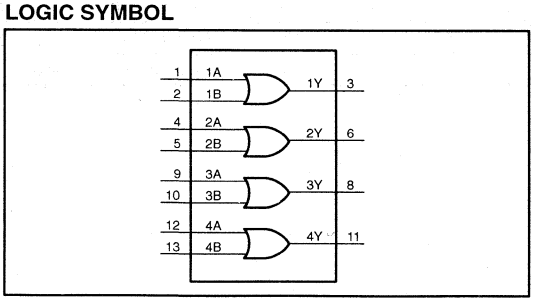
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A – 4A	Data inputs
2, 5, 10, 13	1B – 4B	Data inputs
3, 6, 8, 11	1Y – 4Y	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

H = High voltage level
L = Low voltage level

Quad 2-input NAND buffer (open drain) 74LVC38

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard 8-1A
- Inputs accept voltages up to 5.5V
- Open drain outputs
- CMOS low power consumption
- Direct interface with TTL levels

DESCRIPTION

The 74LVC38 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC38 provides the 2-input NAND function

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZL}	Propagation delay nA, nB to nY	C_L = 50pF V_{CC} = 3.3V	2.7	ns
t_{PLZ}	Propagation delay nA, nB to nY	C_L = 50pF V_{CC} = 3.3V	5.0	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1, 2	20	pF

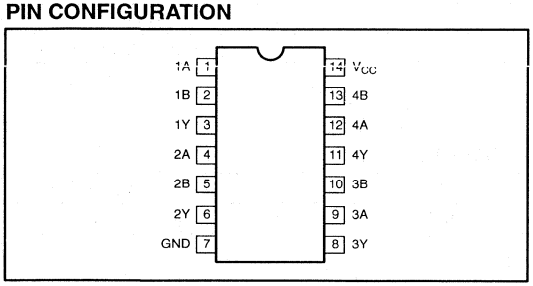
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) +$
   $\sum (V_O^2 / R_L) \times$ duty factor LOW, where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   V_O = output voltage in V; R_L = pull-up resistor in MΩ;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.
3. The given value of C_{PD} is obtained with: C_L = 0pF and $R_L = \infty$

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC38D	14	SO	Plastic	SO14/SOT108A
74LVC38DB	14	SSOP	Plastic	SSOP14/SOT337
74LVC38PW	14	TSSOP	Plastic	TSSOP14/SOT402

PIN CONFIGURATION

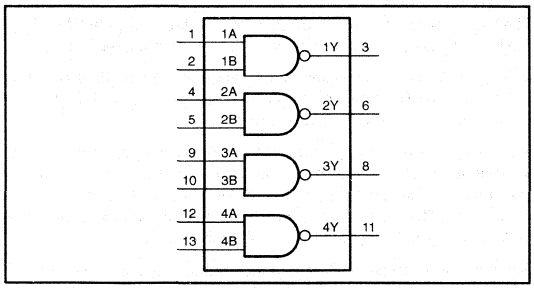


PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 4, 9, 12	1A–4A	Data inputs
2, 5, 10, 13	1B–4B	Data inputs
3, 6, 8, 11	1Y–4Y	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

Quad 2-input NAND buffer (open drain) 74LVC38

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	Z
L	H	Z
H	L	Z
H	H	L

H = HIGH voltage level
L = LOW voltage level
Z = High impedance OFF-state

Dual D-type flip-flop with set and reset; positive edge trigger

74LVC74

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74LVC74 is a high-performance, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible families.

The 74LVC74 is a dual positive edge triggered, D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set ($\overline{S}_D$) and ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

Schmitt-trigger action in all data inputs makes the circuit highly tolerant of slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nCP to nQ, n$\overline{Q}$ n$\overline{S}_D$ to nQ, n$\overline{Q}$ n$\overline{R}_D$ to nQ, n$\overline{Q}$	C_L = 50pF V_{CC} = 3.3V	3.8 4.4 4.4	ns
f_{max}	Maximum clock frequency		250	MHz
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1, 2	24	pF

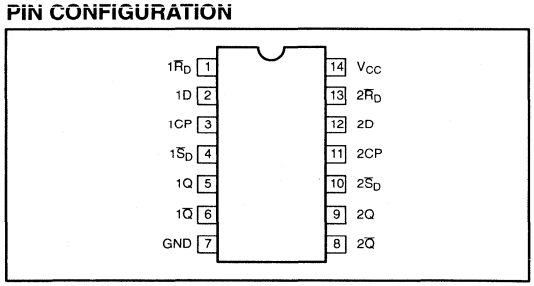
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC74D	14	SO	PLASTIC	SO14/SOT108A
74LVC74DB	14	SSOP	PLASTIC	SSOP14/SOT337
74LVC74PW	14	TSSOP	PLASTIC	TSSOP14/SOT402

PIN CONFIGURATION

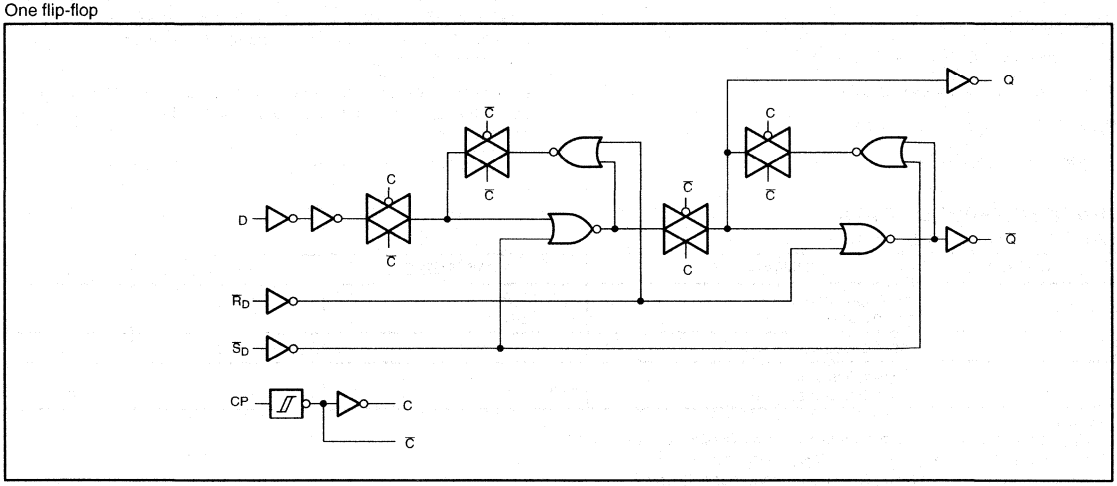


PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 13	1$\overline{R}_D$, 2$\overline{R}_D$	Asynchronous reset-direct input (active LOW)
2, 12	1D, 2D	Data inputs
3, 11	1CP, 2CP	Clock input (LOW-to-HIGH, edge-triggered)
4, 10	1$\overline{S}_D$, 2$\overline{S}_D$	Asynchronous set-direct input (active LOW)
5, 9	1Q, 2Q	True flip-flop outputs
6, 8	1$\overline{Q}$, 2$\overline{Q}$	Complement flip-flop outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC DIAGRAM

One flip-flop



FUNCTION TABLES

INPUTS				OUTPUTS	
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

INPUTS				OUTPUTS	
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH CP transition
Q_{n+1} = State after the next LOW-to-HIGH CP transition

Quad 2-input EXCLUSIVE-OR gate | 74LVC86

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels

DESCRIPTION

The 74LVC86 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC86 provides the 2-input EXCLUSIVE-OR function.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA, nB to nY	C_L = 15pF V_{CC} = 3.3V	3.7	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1, 2	55	pF

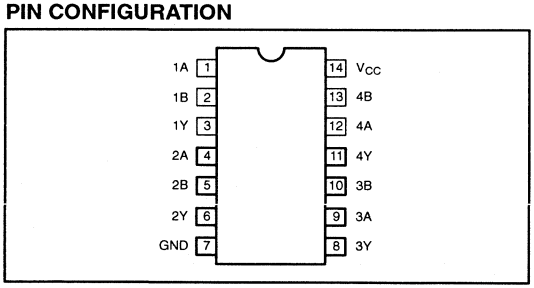
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

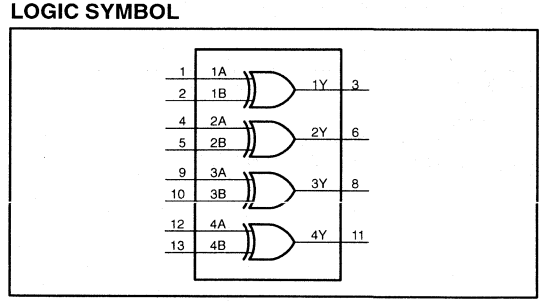
ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC86D	14	SO	PLASTIC	SO14/SOT108A
74LVC86DB	14	SSOP	PLASTIC	SSOP14/SOT337
74LVC86PW	14	TSSOP	PLASTIC	TSSOP14/SOT402

PIN CONFIGURATION



LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 4, 9, 12	1A–4A	Data inputs
2, 5, 10, 13	1B–4B	Data inputs
3, 6, 8, 11	1Y–4Y	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

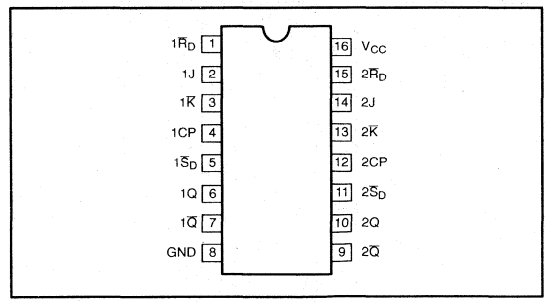
H = HIGH voltage level
L = LOW voltage level

Dual $J\overline{K}$ flip-flop with set and reset; positive-edge trigger 74LVC109

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- Output capability: standard
- I_{CC} category: flip-flops

PIN CONFIGURATION



DESCRIPTION

The 74LVC109 is a low-voltage, Si-gate CMOS device and is pin and function compatible with 74HC/HCT109.

The 74LVC109 is a dual positive-edge triggered JK type flip-flop featuring individual J, $\overline{K}$ inputs, clock (CP) inputs, set ($\overline{S}_D$) and reset ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input.

The J and $\overline{K}$ inputs control the state changes of the flip-flops as described in the mode select function table.

The J and $\overline{K}$ inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

The $J\overline{K}$ design allows operation as a D-type flip-flop by tying the J and $\overline{K}$ inputs together.

Schmitt-trigger action in the clock input makes the circuit highly tolerant of slower clock rise and fall times.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 15	1$\overline{R}_D$, 2$\overline{R}_D$	Asynchronous reset-direct input (active LOW)
2, 14, 3, 13	1J, 2J, 1$\overline{K}$, 2$\overline{K}$	Synchronous inputs; flip-flops 1 and 2
4, 12	1CP, 2CP	Clock input (LOW-to-HIGH, edge-triggered)
5, 11	1$\overline{S}_D$, 2$\overline{S}_D$	Asynchronous set inputs (active LOW)
6, 10	1Q, 2Q	True flip-flop outputs
7, 9	1$\overline{Q}$, 2$\overline{Q}$	Complement flip-flop outputs
8	GND	Ground (0V)
16	V_{CC}	Positive supply voltage

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nCP to nQ, n$\overline{Q}$ n$\overline{S}_D$ to nQ, n$\overline{Q}$ n$\overline{R}_D$ to nQ, n$\overline{Q}$	C_L = 50pF V_{CC} = 3.3V	 4.0 4.5 4.5	ns
f_{max}	Maximum clock frequency		250	MHz
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1, 2	15	pF

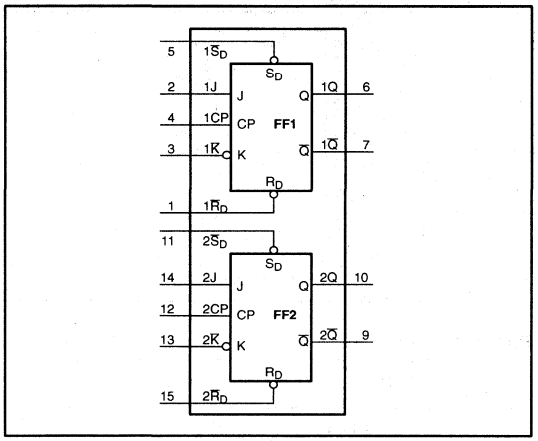
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

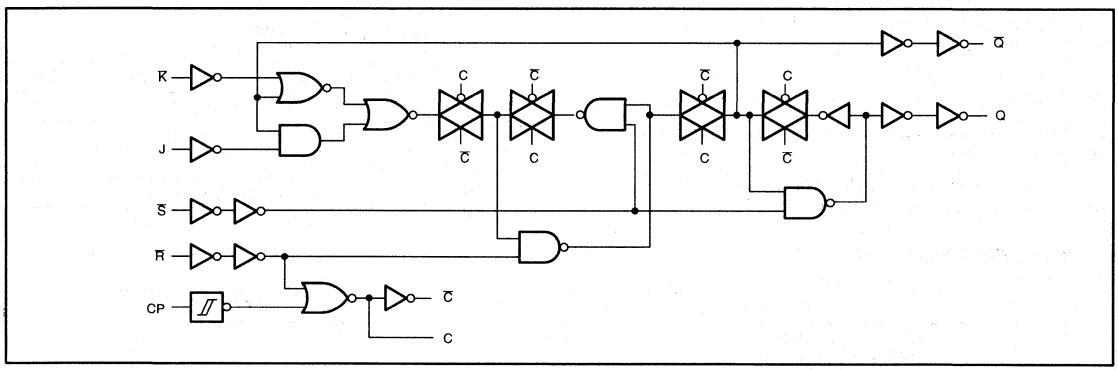
ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC109D	16	SO	PLASTIC	SO16/SOT109A
74LVC109DB	16	SSOP	PLASTIC	SSOP16/SOT338
74LVC109PW	16	TSSOP	PLASTIC	TSSOP16/SOT403

FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS					OUTPUTS	
	$n\overline{S}_D$	$n\overline{R}_D$	nCP	nJ	$n\overline{K}$	nQ	$n\overline{Q}$
Asynchronous set	l	H	X	X	X	H	L
Asynchronous reset	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	↑	h	l	$\overline{q}$	q
Load "0" (reset)	H	H	↑	l	l	L	H
Load "1" (set)	H	H	↑	h	h	H	L
Hold "no change"	H	H	↑	l	h	q	$\overline{q}$

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = Lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
X = Don't care
↑ = LOW-to-HIGH CP transition

Quad buffer/line driver; 3-State 74LVC125

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74LVC125 is a high-performance, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC125 consists of four non-inverting buffers/line drivers with 3-State outputs. The 3-State outputs (nY) are controlled by the output enable input ($n\overline{OE}$). A HIGH at $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA to nY	C_L = 50pF V_{CC} = 3.3V	3.5	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_{CC} = 3.3V Notes 1, 2	22	pF

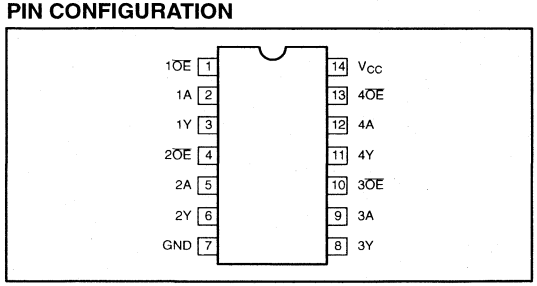
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC125D	14	SO	PLASTIC	SO14/SOT108A
74LVC125DB	14	SSOP	PLASTIC	SSOP14/SOT337
74LVC125PW	14	TSSOP	PLASTIC	TSSOP14/SOT402

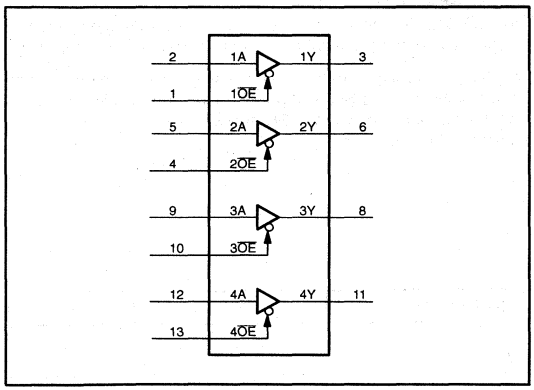
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 4, 10, 13	$1\overline{OE}$ to $4\overline{OE}$	Output enable inputs (active LOW)
2, 5, 9, 12	1A to 4A	Data inputs
3, 6, 8, 11	1Y to 4Y	Data outputs
7	GND	Groubd (0V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA	nY
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF-state

3-to-8 line decoder/demultiplexer; inverting | 74LVC138

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- Output drive capability 50 Ω transmission lines at 85°C

DESCRIPTION

The 74LVC138 is a low-voltage, low-power, high-performance Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC138 accepts three binary weighted address inputs (A_0, A_1, A_2) and when enabled, provide 8 mutually exclusive active LOW outputs ($\overline{Y}_0$ to $\overline{Y}_7$).

The 74LVC138 features three enable inputs: two active LOW ($\overline{E}_1$ and $\overline{E}_2$ and one active HIGH (E_3). Every output will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH.

This multiple enable function allows easy parallel expansion of the 74LVC138 to a 1-of-32 (5 lines to 32 lines) decoder with just four 74LVC138 ICs and one inverter. The 74LVC138 can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL} t_{PLH}	Propagation delay An to $\overline{Y}n$; E3 to $\overline{Y}n$, $\overline{E}n$ to $\overline{Y}n$	C_L = 15pF; V_{CC} = 3.3V	4.0 4.4	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per package	V_{CC} = 3.3V Notes 1, 2	22	pF

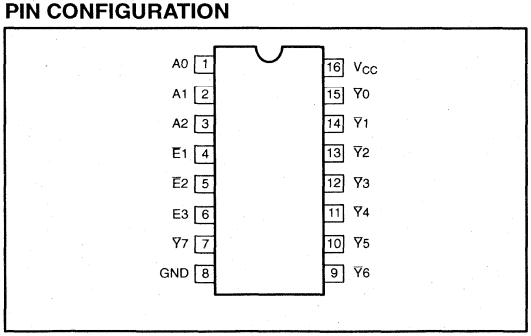
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC138D	14	SO	Plastic	SO14/SOT108A
74LVC138DB	14	SSOP	Plastic	SSOP14/SOT337
74LVC138PW	14	TSSOP	Plastic	TSSOP14/SOT402

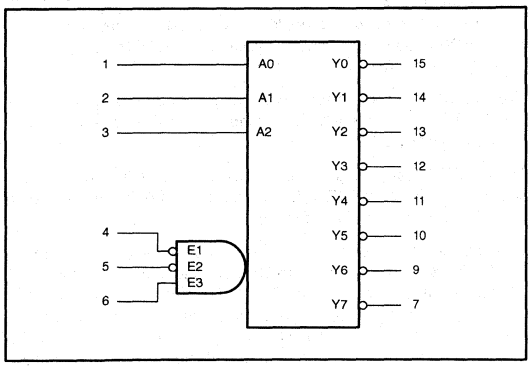
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 3	A0 – A2	Address inputs
4, 5	$\overline{E}1$ – $\overline{E}2$	Enable inputs (active LOW)
6	E3	Enable inputs (active HIGH)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y}0$ – $\overline{Y}7$	Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive power supply

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	Y_6	$\overline{Y}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

Dual 2-to-4 line decoder/demultiplexer 74LVC139

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- Demultiplexing capability
- Two independent 2-to-4 decoders
- Multifunction capability
- Active LOW mutually exclusive outputs
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74LVC139 is a high-performance, low-voltage, low power, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC139 is a dual 2-to-4 line decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (nA_0 and nA_1) and providing four mutually exclusive active LOW outputs ($n\overline{Y}_0$ to $n\overline{Y}_3$). Each decoder has an active LOW enable input ($n\overline{E}$). When $n\overline{E}$ is HIGH, every output is forced HIGH. The enable can be used as the data input for a 1-to-4 demultiplexer application.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA_n to $n\overline{Y}_n$, $n\overline{E}$ to $n\overline{Y}_n$	C_L = 50pF V_{CC} = 3.3V	3.0 2.9	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per multiplexer	V_{CC} = 3.3V Notes 1, 2	29	pF

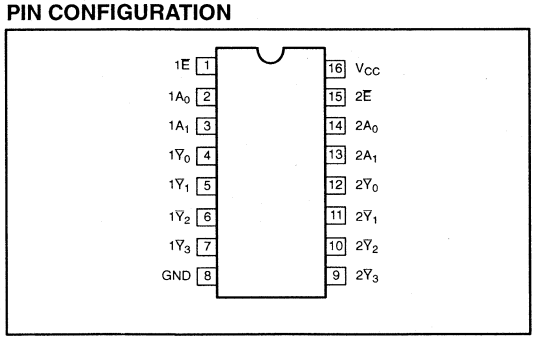
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC139D	16	SO	Plastic	SO16/SOT109A
74LVC139DB	16	SSOP	Plastic	SSOP16/SOT338
74LVC139PW	16	TSSOP	Plastic	TSSOP16/SOT403

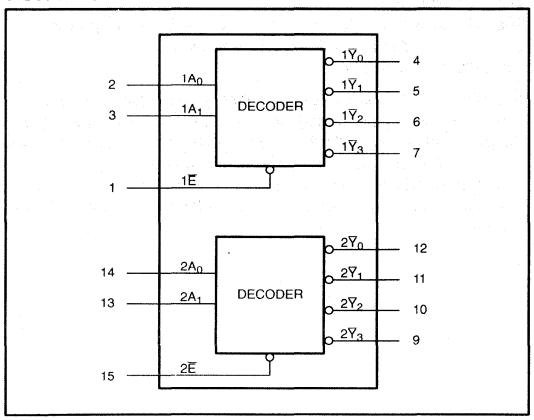
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 15	$1\overline{E}$, $2\overline{E}$	Enable inputs (active LOW)
2, 3	$1A_0$, $1A_1$	Address inputs
4, 5, 6, 7	$1\overline{Y}_0$ to $1\overline{Y}_3$	Outputs (active LOW)
8	GND	Ground (0V)
12, 11, 10, 9	$2\overline{Y}_0$ to $2\overline{Y}_3$	Outputs (active LOW)
14, 13	$2A_0$, $2A_1$	Address inputs
16	V_{CC}	Positive Supply voltage

FUNCTIONAL DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS			
$n\overline{E}$	nA_0	nA_1	$n\overline{Y}_0$	$n\overline{Y}_1$	$n\overline{Y}_2$	$n\overline{Y}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

Quad 2-input multiplexer 74LVC157

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- Output drive capability 50Ω transmission lines @ 85°C
- Non-inverting data path

DESCRIPTION

The 74LVC157 is a high-performance, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible families.

The 74LVC157 is a quad 2-input multiplexer which selects 4 bits of data from two sources under the control of a common data select input(S). The four outputs present the selected data in the true (non-inverted) form. The enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (1Y to 4Y) are forced LOW regardless of all other input conditions. Moving the data from two groups of registers to four common output buses is a common use of the "157". The state of the common data select input (S) determines the particular register from which the data comes. It can also be used as a function generator.

The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The "157" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The "157" is identical to the "158" but has non-inverting (true) outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nI_0, nI_1 to nY $\overline{E}$ to nY S to nY	C_L = 50pF V_{CC} = 3.3V	4.2 3.8 4.7	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1, 2	30	pF

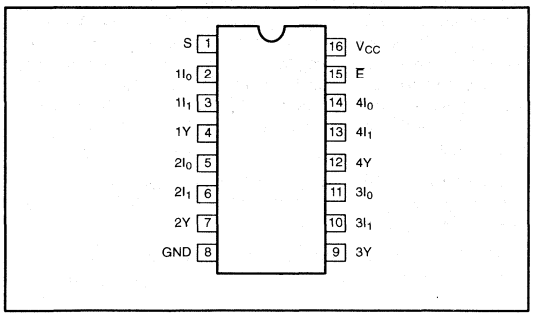
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC157D	16	SO	Plastic	SO16/SOT109A
74LVC157DB	16	SSOP	Plastic	SSOP16/SOT338M
74LVC157PW	16	TSSOP	Plastic	TSSOP16/SOT403

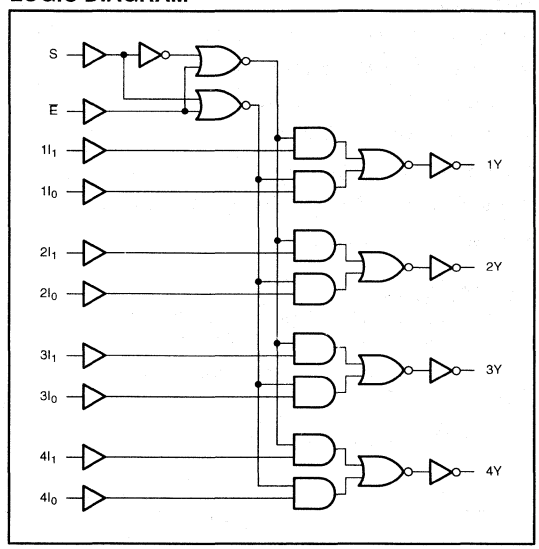
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	S	Common data select input
2, 5, 11, 14	$1I_0$–$4I_0$	Data inputs from source 0
3, 6, 10, 13	$1I_1$–$4I_1$	Data inputs from source 1
4, 7, 9, 12	1Y–4Y	Multiplexer outputs
8	GND	Ground (0V)
15	$\overline{E}$	Enable input (active LOW)
16	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUT
$\overline{E}$	S	nI_0	nI_1	nY
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

Octal buffer/line driver; 3-State; inverting — 74LVC240

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- Output drive capacity 50Ω transmission lines at 85°C

DESCRIPTION

The 74LVC240 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC240 is an octal inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-State. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times. The 74LVC240 is identical to the 74LVC244 but has inverting outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL} t_{PLH}	Propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 50pF; V_{CC} = 3.3V	4.6	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per beffer	notes [1, 2]	30	pF

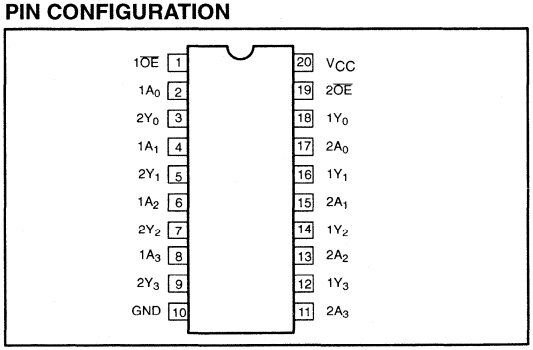
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC240D	20	SO	Plastic	SO20/SOT163A
74LVC240DB	20	SSOP	Plastic	SSOP20/SOT339
74LVC240PW	20	TSSOP	Plastic	TSSOP20/SOT360

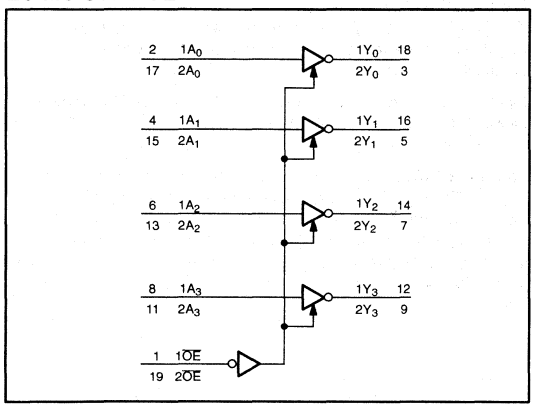
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 4, 6, 8	$1A_0 - 1A_3$	Data inputs
3, 5, 7, 9	$2Y_0 - 2Y_3$	Bus outputs
10	GND	Ground (0V)
17, 15, 13, 11	$2A_0 - 2A_3$	Data inputs
18, 16, 14, 12	$1Y_0 - 1Y_3$	Bus outputs
19	$2\overline{OE}$	Output enable input (active LOW)
20	V_{CC}	Positive power supply

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS
$n\overline{OE}$	nA_n	nY_n
L	L	H
L	H	L
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance OFF-state

Octal buffer/line driver; 3-State | 74LVC241

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- Output drive capacity 50Ω transmission line at 85°C

DESCRIPTION

The 74LVC241 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC241 is an octal non-inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs $1\overline{OE}$ and 2OE. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL} t_{PLH}	Propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 50pF; V_{CC} = 3.3V	4.8	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1, 2	30	pF

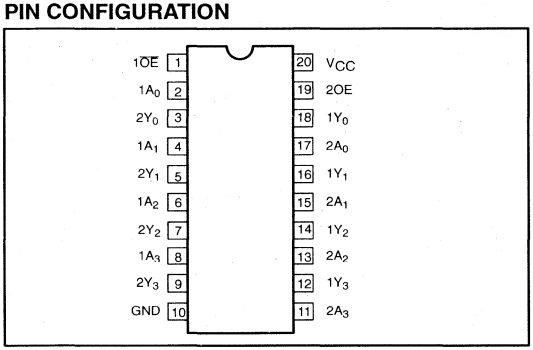
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC241D	20	SO	Plastic	SO20/SOT163A
74LVC241DB	20	SSOP	Plastic	SSOP20/SOT339
74LVC241PW	20	TSSOP	Plastic	TSSOP20/SOT360

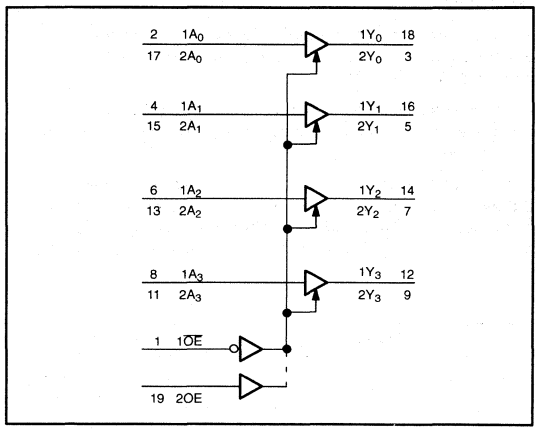
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 4, 6, 8	$1A_0 - 1A_3$	Data inputs
3, 5, 7, 9	$2Y_0 - 2Y_3$	Bus outputs
10	GND	Ground (0V)
17, 15, 13, 11	$2A_0 - 2A_3$	Data inputs
18, 16, 14, 12	$1Y_0 - 1Y_3$	Bus outputs
19	2OE	Output enable input (active LOW)
20	V_{CC}	Positive power supply

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS
$1\overline{OE}$	$1A_n$	$1Y_n$
L	L	L
L	H	H
H	X	Z

INPUTS		OUTPUTS
2OE	$2A_n$	$2Y_n$
H	L	L
H	H	H
L	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance OFF-state

Octal buffer/line driver; 3-State | 74LVC244

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- Output drive capacity 50Ω transmission lines at 85°C

DESCRIPTION

The 74LVC244 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC244 is an octal non-inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-State. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times. The 74LVC244 is identical to the 74LVC240 but has non-inverting outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL} t_{PLH}	Propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 50pF; V_{CC} = 3.3V	4.9	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1, 2	30	pF

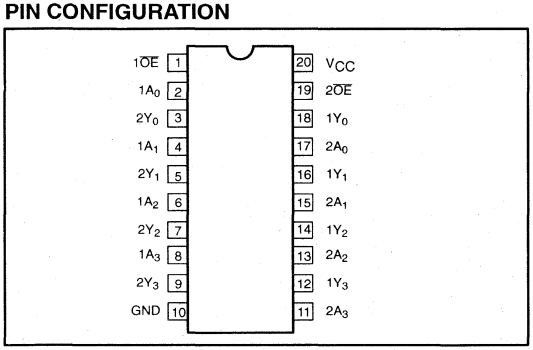
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC244D	20	SO	Plastic	SO20/SOT163A
74LVC244DB	20	SSOP	Plastic	SSOP20/SOT339
74LVC244PW	20	TSSOP	Plastic	TSSOP20/SOT360

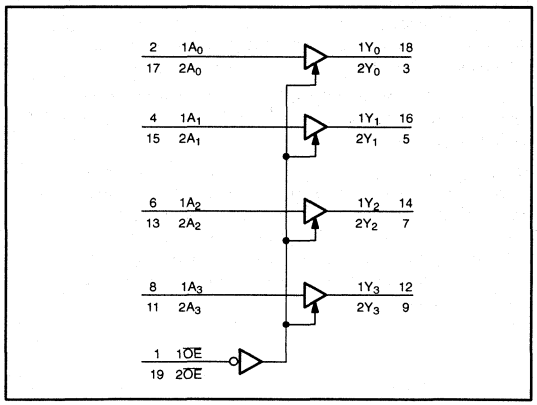
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 4, 6, 8	$1A_0 - 1A_3$	Data inputs
3, 5, 7, 9	$2Y_0 - 2Y_3$	Bus outputs
10	GND	Ground (0V)
17, 15, 13, 11	$2A_0 - 2A_3$	Data inputs
18, 16, 14, 12	$1Y_0 - 1Y_3$	Bus outputs
19	$2\overline{OE}$	Output enable input (active LOW)
20	V_{CC}	Positive power supply

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	L
L	H	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance OFF-state

Octal bus transceiver with direction pin; 3-State — 74LVC245

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- Direct interface with TTL levels
- CMOS low power consumption
- Output drive capacity 50Ω transmission lines at 85°C

DESCRIPTION

The 74LVC245 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC245 is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The 74LVC245 features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) input for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated. The 74LVC245 is identical to the 74LVC640 but has true (non-inverting) outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL} t_{PLH}	Propagation delay A_n to B_n; B_n to A_n	C_L = 50pF; V_{CC} = 3.3V	4.1	ns
C_I	Input capacitance		5.0	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1, 2	40	pF

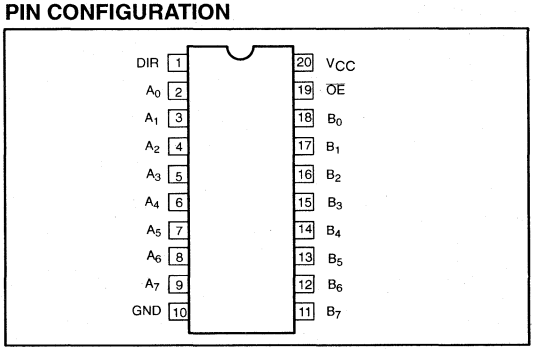
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC245D	20	SO	Plastic	SO20/SOT163A
74LVC245DB	20	SSOP	Plastic	SSOP20/SOT339
74LVC245PW	20	TSSOP	Plastic	TSSOP20/SOT360

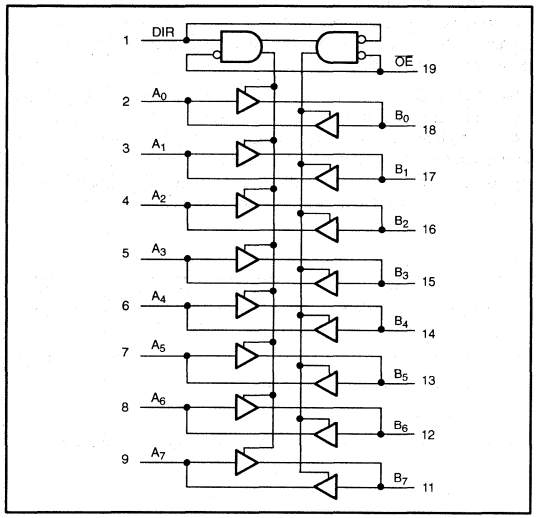
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	DIR	Direction control
2, 3, 4, 5, 6, 7, 8, 9	$A_0 - A_7$	Data inputs/outputs
10	GND	Ground (0V)
18, 17, 16, 15, 14, 13, 12, 11	$B_0 - B_7$	Data inputs/outputs
19	$\overline{OE}$	Output enable input (active LOW)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		INPUTS/OUTPUT	
$\overline{OE}$	DIR	A_n	B_n
L	L	A=B	inputs
L	H	Inputs	B=A
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance OFF-state

Quad 2-input multiplexer; 3-State | 74LVC257

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- Output drive capacity 50Ω transmission lines at 85°C
- Non-inverting data path

DESCRIPTION

The 74LVC257 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC257 is a quad 2-input multiplexer with 3-State outputs, which select 4 bits of data from two sources under the control of a common data select input (S). The data inputs from source 0 ($1I_0$ to $4I_0$) are selected when input S is LOW and the data inputs from source 1 ($1I_1$ to $4I_1$) are selected when S is HIGH. Data appears at the outputs (1Y to 4Y) in true (non-inverting) form from the selected inputs. The 74LVC257 is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The outputs are forced to a high impedance OFF-state when $\overline{OE}$ is HIGH.

The logic equations for the outputs are:
$1Y = \overline{OE}\ (1I_1 \bullet S + 1I_0 \bullet S)$
$2Y = \overline{OE}\ (2I_1 \bullet S + 2I_0 \bullet S)$
$3Y = \overline{OE}\ (3I_1 \bullet S + 3I_0 \bullet S)$
$4Y = \overline{OE}\ (4I_1 \bullet S + 4I_0 \bullet S)$

The 74LVC257 is identical to the 74LVC258 but has non-inverting (true) outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL} t_{PLH}	Propagation delay nI_0, nI_1 to nY S to nY	C_L = 50pF; V_{CC} = 3.3V	4.0 4.5	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per gate	notes [1, 2]	30	pF

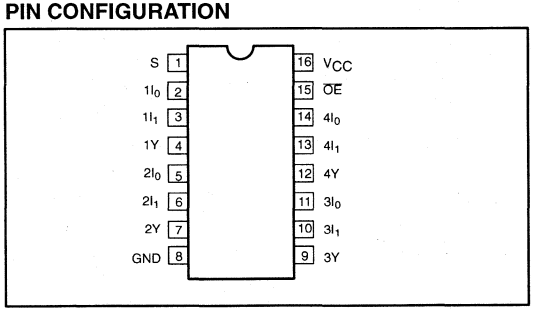
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC257D	16	SO	Plastic	SO16/SOT109A
74LVC257DB	16	SSOP	Plastic	SSOP16/SOT338M
74LVC257PW	16	TSSOP	Plastic	TSSOP16/SOT403

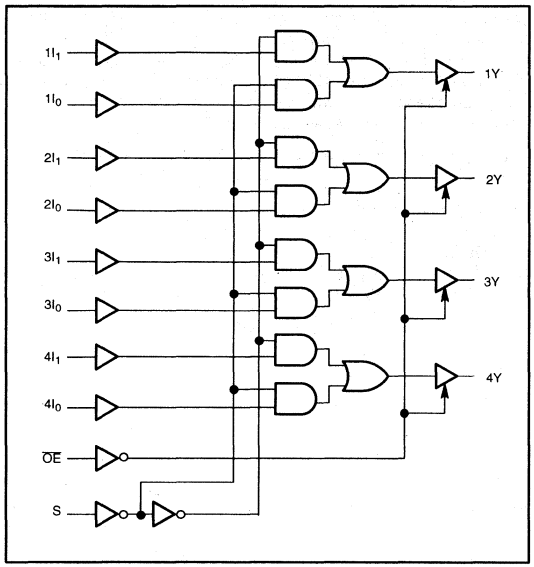
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	S	Common data select input
2, 5, 11, 14	$1I_0 - 4I_0$	Data inputs from source 0
3, 6, 10, 13	$1I_1 - 4I_1$	Data inputs from source 1
4, 7, 9, 12	1Y to 4Y	3-State multiplexer outputs
8	GND	Ground (0V)
15	$\overline{OE}$	3-State output enable input (active LOW)
16	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	nI_0	nI_1	nY
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance OFF-state

Octal D-type transparent latch; 3-State | 74LVC373

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- Common 3-State output enable input
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74LVC373 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC373 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all internal latches.

The 74LVC373 consists of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches. The 74LVC373 is functionally identical to the 74LVC573, but the 74LVC573 has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay D_n to Q_n LE to Q_n	C_L = 50pF V_{CC} = 3.3V	 4.3 4.6	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	23	pF

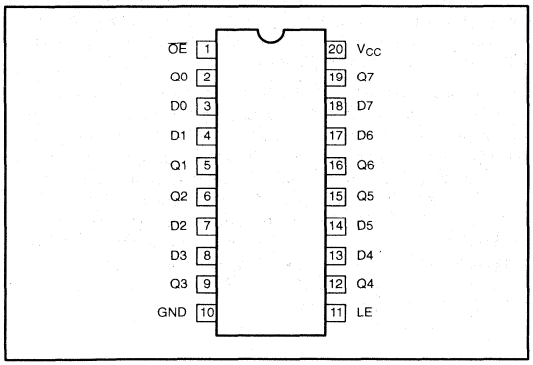
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC373D	20	SO	Plastic	SO20/SOT163A
74LVC373DB	20	SSOP	Plastic	SSOP20/SOT339
74LVC373PW	20	TSSOP	Plastic	TSSOP20/SOT360

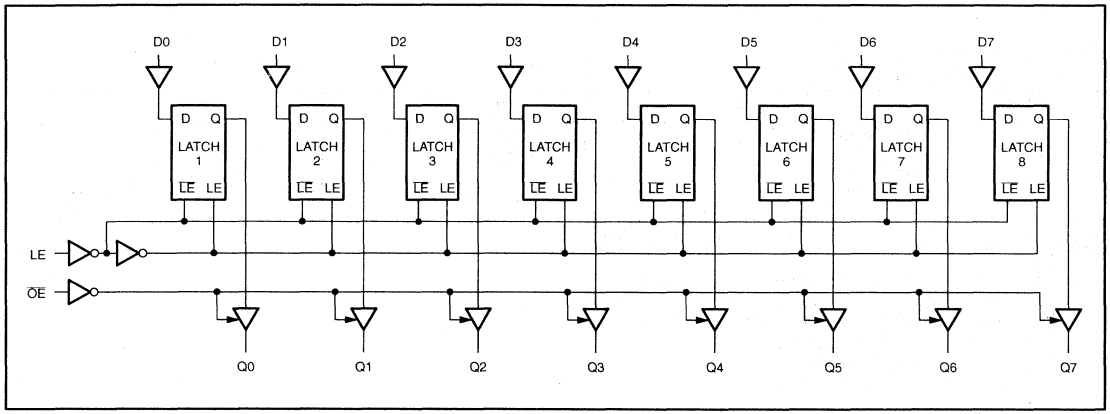
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enabled input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0–Q7	3-State latch outputs
3, 4, 7, 8, 13, 14, 17, 18	D0–D7	Data inputs
10	GND	Ground (0V)
11	LE	Latch enable input (active HIGH)
20	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	Dn		Q0 to Q7
Enable and read register (transparent mode)	L L	H H	L H	L H	L H
Latch and read register	L L	L L	l h	L H	L H
Latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW transition
X = Don't care
Z = High impedance OFF-state

Octal D-type flip-flop; positive edge-trigger; 3-State 74LVC374

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- 8-bit positive edge-triggered register
- Independent register and 3-State buffer operation
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74LVC374 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC374 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-State outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The eight flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the eight flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. The 74LVC374 is functionally identical to the 74LVC574, but the 74LVC574 has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Qn	C_L = 50pF V_{CC}= 3.3V	4.8	ns
f_{max}	Maximum clock frequency		150	MHz
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes [1, 2]	28	pF

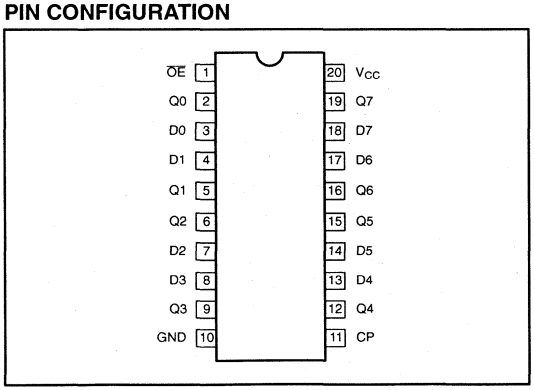
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC374D	20	SO	Plastic	SO20/SOT163A
74LVC374DB	20	SSOP	Plastic	SSOP20/SOT339
74LVC374PW	20	TSSOP	Plastic	TSSOP20/SOT360

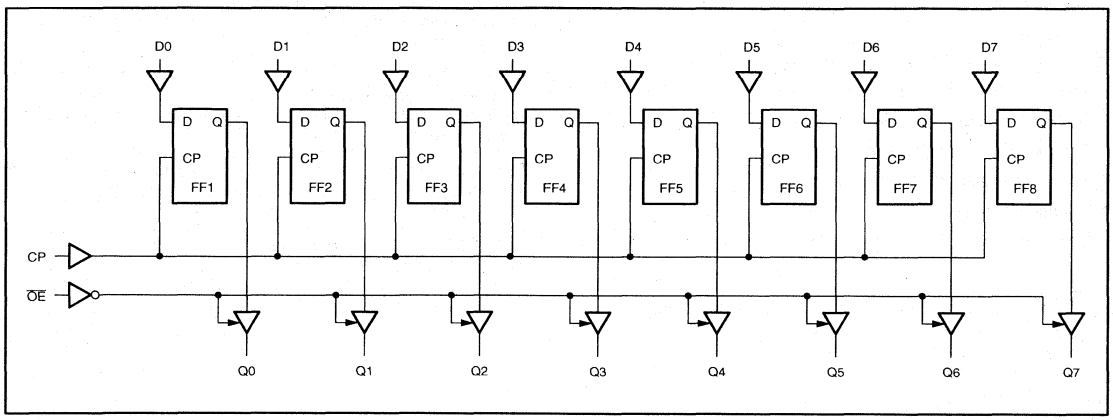
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0–Q7	3-State flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D0–D7	Data inputs
10	GND	Ground (0V)
11	CP	Clock input (LOW-to-HIGH, edge-triggered
20	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	Dn		Q0–Q7
Load and read register	L L	↑ ↑	l h	L H	L H
Load register and disable outputs	H H	↑ ↑	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH transition
Z = High impedance OFF-state
↑ = LOW-to-HIGH clock transition

Octal D-type registered transceiver; 3-State 74LVC543

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- Combines 74LVC245 and 74LVC373 type functions in one chip
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- 3-State non-inverting outputs for bus oriented applications

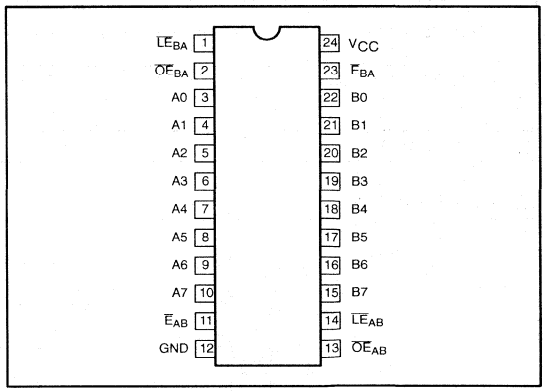
DESCRIPTION

The 74LVC543 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC543 is an octal registered transceiver containing two sets of D-type latches for temporary storage of the data flow in either direction. Separate latch enable ($\overline{LE}_{AB}$, $\overline{LE}_{BA}$) and output enable ($\overline{OE}_{AB}$, $\overline{OE}_{BA}$) inputs are provided for each register to permit independent control of inputting in either direction of the data flow.

The 74LVC543 contains eight D-type latches, with separate inputs and controls for each set. For data flow from A to B, for example, the A-to-B enable ($\overline{E}_{AB}$) input must be LOW in order to enter data from A0–A7 or take data from B0–B7, as indicated in the function table. With $\overline{E}_{AB}$ LOW, a LOW signal on the A-to-B latch enable ($\overline{LE}_{AB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LE}_{AB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{E}_{AB}$ and $\overline{OE}_{AB}$ both LOW, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{LE}_{BA}$	B to A latch enable input (active LOW)
2	$\overline{OE}_{BA}$	B to A output enable input (active LOW)
3, 4, 5, 6, 7, 8, 9, 10	A0–A7	A data inputs/outputs
11	$\overline{E}_{AB}$	B to A enable input (active LOW)
12	GND	Ground (0V)
22, 21, 20, 19, 18, 17, 16, 15	B0–B7	B data inputs/outputs
13	$\overline{OE}_{AB}$	A to B output enable input (active LOW)
14	$\overline{LE}_{AB}$	A to B latch enable input (active LOW)
23	$\overline{E}_{BA}$	A to B enable input (active LOW)
24	V_{CC}	Positive supply voltage

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An–Bn	C_L = 50pF V_{CC} = 3.3V	5.4	ns
C_I	Input capacitance		5.0	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	33	pF

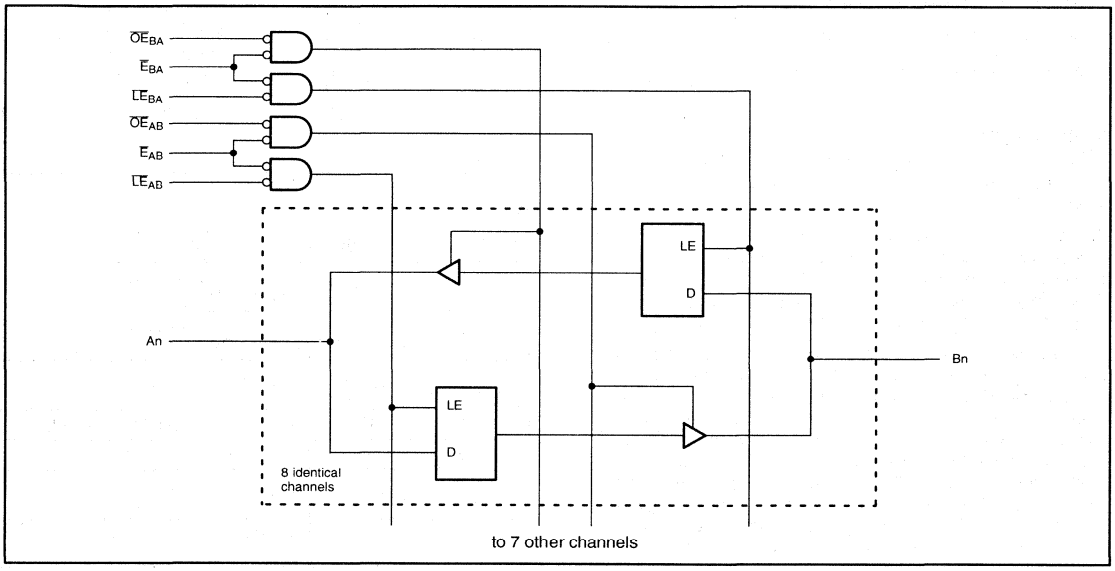
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC543D	24	SO	Plastic	SO24/SOT137
74LVC543DB	24	SSOP	Plastic	SSOP24/SOT340
74LVC543PW	24	TSSOP	Plastic	TSSOP24/SOT355

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OE}_{XX}$	$\overline{E}_{XX}$	$\overline{LE}_{XX}$	DATA		
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	H L	Latch + Display
L L	L L	L L	H L	H L	Transparent
L	L	H	X	NC	Hold

XX = AB for A-to-B direction, BA for B-to-A direction
H = HIGH voltage level
L = LOW voltage level
h = HIGH state must be present one setup time before the LOW-to-HIGH transition of $\overline{LE}_{AB}$, $\overline{LE}_{BA}$, $\overline{E}_{AB}$, $\overline{E}_{BA}$
l = LOW state must be present one setup time before the LOW-to-HIGH transition of $\overline{LE}_{AB}$, $\overline{LE}_{BA}$, $\overline{E}_{AB}$, $\overline{E}_{BA}$
X = Don't care
↑ = LOW-to-HIGH level transition
NC= No change
Z = High impedance OFF state

Octal registered transceiver; 3-State; inverting 74LVC544

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- Combines 74LVC640 and 74LVC533 type functions in one chip
- Octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- 3-State inverting outputs for bus oriented applications

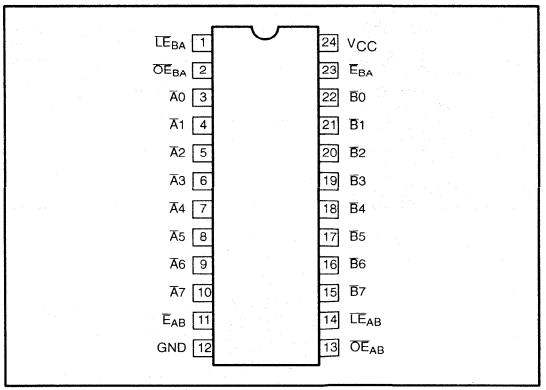
DESCRIPTION

The 74LVC544 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC544 is an octal registered inverting transceiver containing two sets of D-type latches for temporary storage of the data flow in either direction. Separate latch enable ($\overline{LE}_{AB}$, $\overline{LE}_{BA}$) and output enable ($\overline{OE}_{AB}$, $\overline{OE}_{BA}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of the data flow.

The 74LVC544 contains eight D-type latches, with separate inputs and controls for each set. For data flow from A to B, for example, the A-to-B enable ($\overline{E}_{AB}$) input must be LOW in order to enter data from $\overline{A0}$–$\overline{A7}$ or take data from $\overline{B0}$–$\overline{B7}$, as indicated in the function table. With $\overline{E}_{AB}$ LOW, a LOW signal on the A-to-B latch enable ($\overline{LE}_{AB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LE}_{AB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{E}_{AB}$ and $\overline{OE}_{AB}$ both LOW, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{LE}_{BA}$	B to A latch enable input (active LOW)
2	$\overline{OE}_{BA}$	B to A output enable input (active LOW)
3, 4, 5, 6, 7, 8, 9, 10	$\overline{A0}$–$\overline{A7}$	A data inputs/outputs
11	$\overline{E}_{AB}$	A to B enable input (active LOW)
12	GND	Ground (0V)
22, 21, 20, 19, 18, 17, 16, 15	$\overline{B0}$–$\overline{B7}$	B data inputs/outputs
13	$\overline{OE}_{AB}$	A to B output enable input (active LOW)
14	$\overline{LE}_{AB}$	A to B latch enable input (active LOW)
23	$\overline{E}_{BA}$	B to A enable input (active LOW)
24	V_{CC}	Positive supply voltage

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay $\overline{An}$–$\overline{Bn}$	C_L = 50pF V_{CC} = 3.3V	5.1	ns
C_I	Input capacitance		5.0	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	34	pF

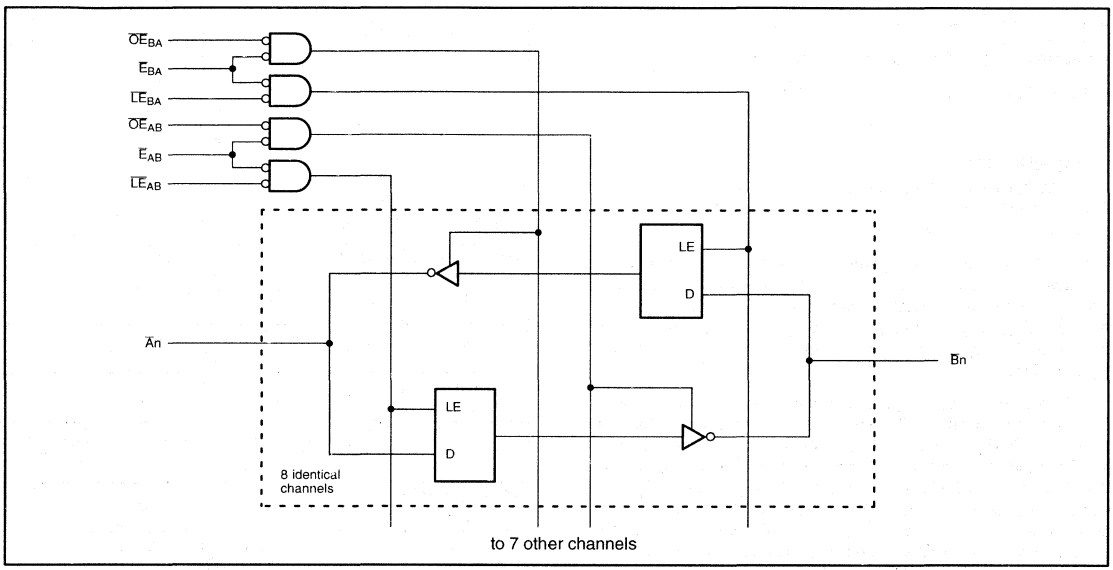
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC544D	24	SO	Plastic	SO24/SOT137A
74LVC544DB	24	SSOP	Plastic	SSOP24/SOT340
74LVC544PW	24	TSSOP	Plastic	TSSOP24/SOT355

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OE}_{XX}$	$\overline{E}_{XX}$	$\overline{LE}_{XX}$	DATA		
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	L H	Latch + Display
L L	L L	L L	H L	L H	Transparent
L	L	H	X	NC	Hold

XX = AB for A-to-B direction, BA for B-to-A direction
H = HIGH voltage level
L = LOW voltage level
h = HIGH state must be present one setup time before the LOW-to-HIGH transition of $\overline{LE}_{AB}$, $\overline{LE}_{BA}$, $\overline{E}_{AB}$, $\overline{E}_{BA}$
l = LOW state must be present one setup time before the LOW-to-HIGH transition of $\overline{LE}_{AB}$, $\overline{LE}_{BA}$, $\overline{E}_{AB}$, $\overline{E}_{BA}$
X = Don't care
↑ = LOW-to-HIGH level transition
NC = No change
Z = High impedance OFF state

Octal D-type transparent latch; 3-State 74LVC573

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- Flow-through pin-out architecture
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74LVC573 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC573 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all internal latches.

The 74LVC573 consists of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the D_n inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches. The 74LVC573 is functionally identical to the 74LVC373, but the 74LVC573 has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay D_n to Q_n LE to Q_n	C_L = 50pF V_{CC} = 3.3V	 4.3 4.6	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	23	pF

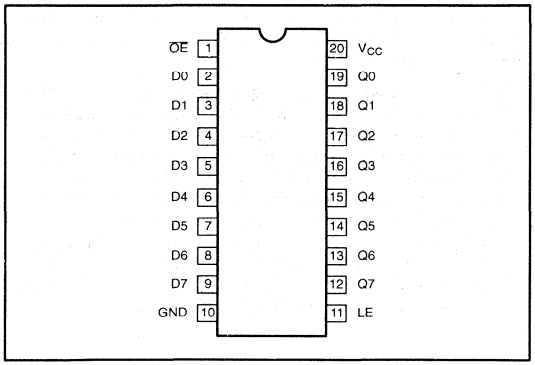
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC573D	20	SO	Plastic	SO20/SOT163A
74LVC573DB	20	SSOP	Plastic	SSOP20/SOT339
74LVC573PW	20	TSSOP	Plastic	TSSOP20/SOT360

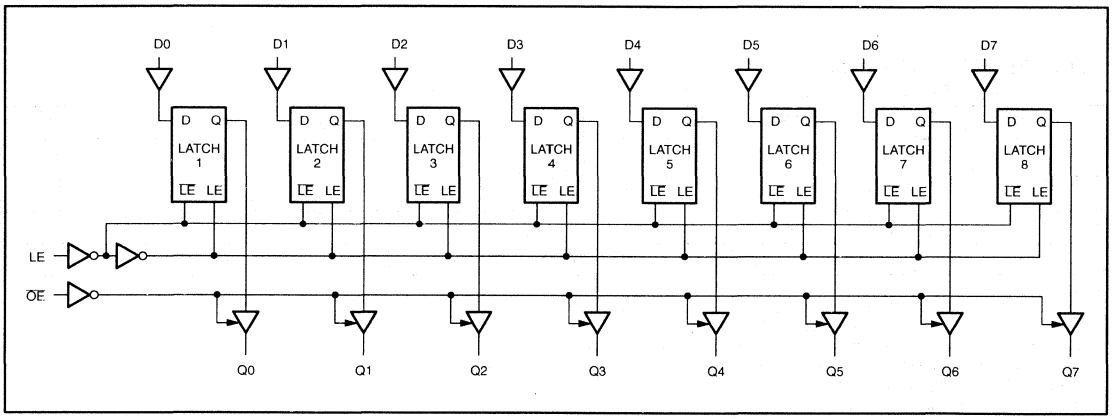
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enabled input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0–D7	Data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0–Q7	3-State latch outputs
10	GND	Ground (0V)
11	LE	Latch enable input (active HIGH)
20	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	Dn		Q0 to Q7
Enable and read register (transparent mode)	L L	H H	L H	L H	L H
Latch and read register	L L	L L	l h	L H	L H
Latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW transition
X = Don't care
Z = High impedance OFF-state

Octal D-type flip-flop; positive-edge trigger; 3-State 74LVC574

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- 8-bit positive edge-triggered register
- Independent register and 3-State buffer operation
- Flow-through pin-out architecture
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74LVC574 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC574 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-State outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The eight flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH CP transition. When $\overline{OE}$ is LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. The 74LVC574 is functionally identical to the 74LVC374, but the 74LVC374 has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Qn	C_L = 50pF V_{CC}= 3.3V	4.8	ns
f_{max}	Maximum clock frequency		150	MHz
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1, 2	28	pF

NOTES:

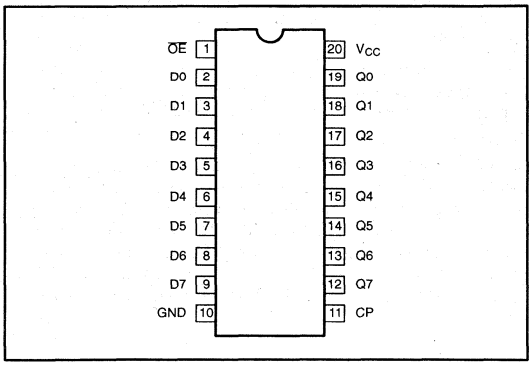
1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC574D	20	SO	Plastic	SO20/SOT163A
74LVC574DB	20	SSOP	Plastic	SSOP20/SOT339
74LVC574PW	20	TSSOP	Plastic	TSSOP20/SOT360

Octal D-type flip-flop; positive-edge trigger; 3-State 74LVC574

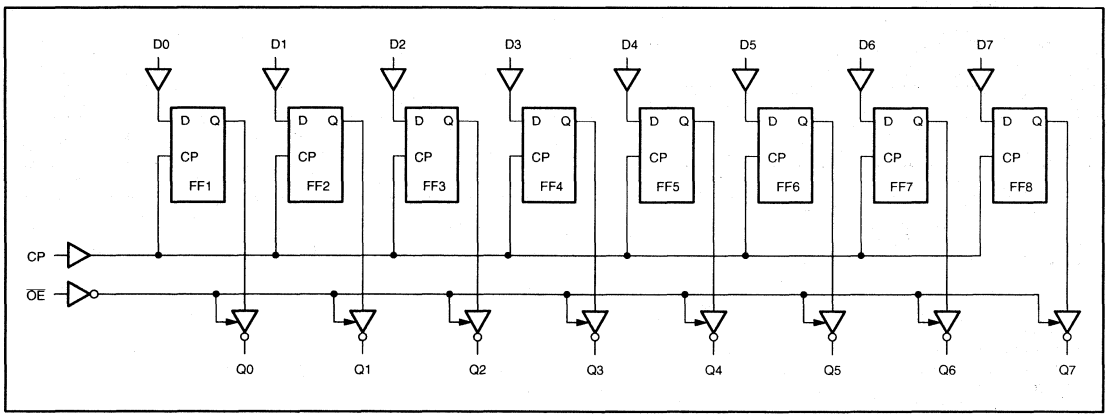
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enabled input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0–D7	Data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0–Q7	3-State flip-flop outputs
10	GND	Ground (0V)
11	CP	Clock input (LOW-to-HIGH, edge-triggered
20	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	Dn		Q0–Q7
Load and read register	L L	↑ ↑	l h	L H	L H
Load register and disable outputs	H H	↑ ↑	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = High impedance OFF-state
↑ = LOW-to-HIGH clock transition

Octal transceiver with dual enable; 3-State 74LVC623

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Flow-through pin-out architecture
- CMOS low power consumption
- Inputs accept voltages up to 5.5V
- Direct interface with TTL levels
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74LVC574 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC623 is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. This octal bus transceiver is designed for asynchronous two-way communication between data buses. The control function implementation allows maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the enable inputs (OE_{AB}, $\overline{OE}_{BA}$). The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual enable function configuration gives this transceiver the capability to store data by simultaneous enabling of OE_{AB} and $\overline{OE}_{BA}$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance OFF-State, both sets of bus lines will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical.

The 74LVC623 is identical to the 74LVC620 but has true (non-inverting) outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Bn; Bn to An	C_L = 50pF V_{CC} = 3.3V	3.8	ns
C_I	Input capacitance		5.0	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1, 2	40	pF

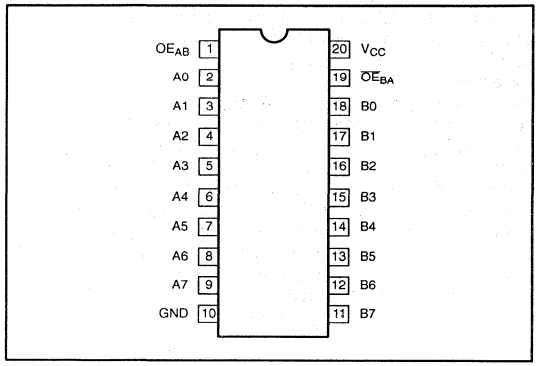
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC623D	20	SO	Plastic	SO20/SOT163A
74LVC623DB	20	SSOP	Plastic	SSOP20/SOT339
74LVC623PW	20	TSSOP	Plastic	TSSOP20/SOT360

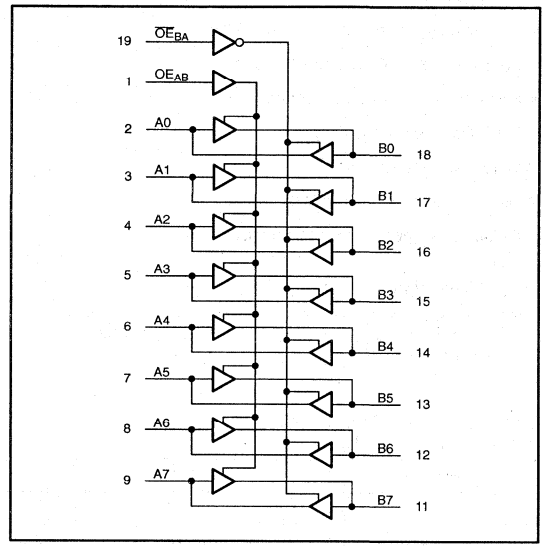
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	OE_{AB}	Output enable input (active HIGH)
2, 3, 4, 5, 6, 7, 8, 9	A0–A7	Data inputs/outputs
10	GND	Ground (0V)
18, 17, 16, 15, 14, 13, 12, 11	B0–B7	Data inputs/outputs
19	$\overline{OE}_{BA}$	Output enable input (active LOW)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
OE_{AB}	$\overline{OE}_{BA}$	An	Bn
L	L	A = B	Inputs
H	H	Inputs	B = A
L	H	Z	Z
H	L	A = B Inputs	Inputs B = A

H = HIGH voltage level
L = LOW voltage level
Z = High impedance OFF-state

Octal bus transceiver/register; 3-State 74LVC646

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- Flow-through pin-out architecture

DESCRIPTION

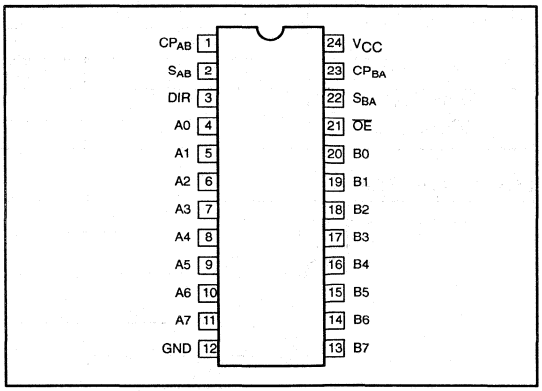
The 74LVC646 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC646 consists of 8 non-inverting bus transceiver circuits with 3-State outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the A or B bus will be clocked in the internal registers, as the appropriate clock (CP_{AB} or CP_{BA}) goes to a HIGH logic level. Output enable ($\overline{OE}$) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register, or in both. The select source inputs (S_{AB} and S_{Ba}) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when $\overline{OE}$ is active (LOW). In the isolation mode ($\overline{OE}$ = HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time.

The 74LVC646 is functionally identical to the 74LVC648, but has non-inverting data paths.

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	CP_{AB}	A to B clock input (LOW-to-HIGH, edge triggered)
2	S_{AB}	Select A to B source input
3	DIR	Direction control input
4, 5, 6, 7, 8, 9, 10, 11	A0 to A7	A data inputs/outputs
12	GND	Ground (0V)
20, 19, 18, 17, 16, 15, 14, 13	B0 to B7	B data inputs/outputs
21	$\overline{OE}$	Output enable input (active LOW)
22	S_{BA}	Select B to A source input
23	CP_{BA}	B to A clock input (LOW-to-HIGH, edge-triggered)
24	V_{CC}	Positive supply voltage

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An, Bn to Bn, An	C_L = 50pF; V_{CC} = 3.3V	4.7	ns
f_{max}	Maximum clock frequency		150	MHz
C_I	Input capacitance		5.0	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	35	pF

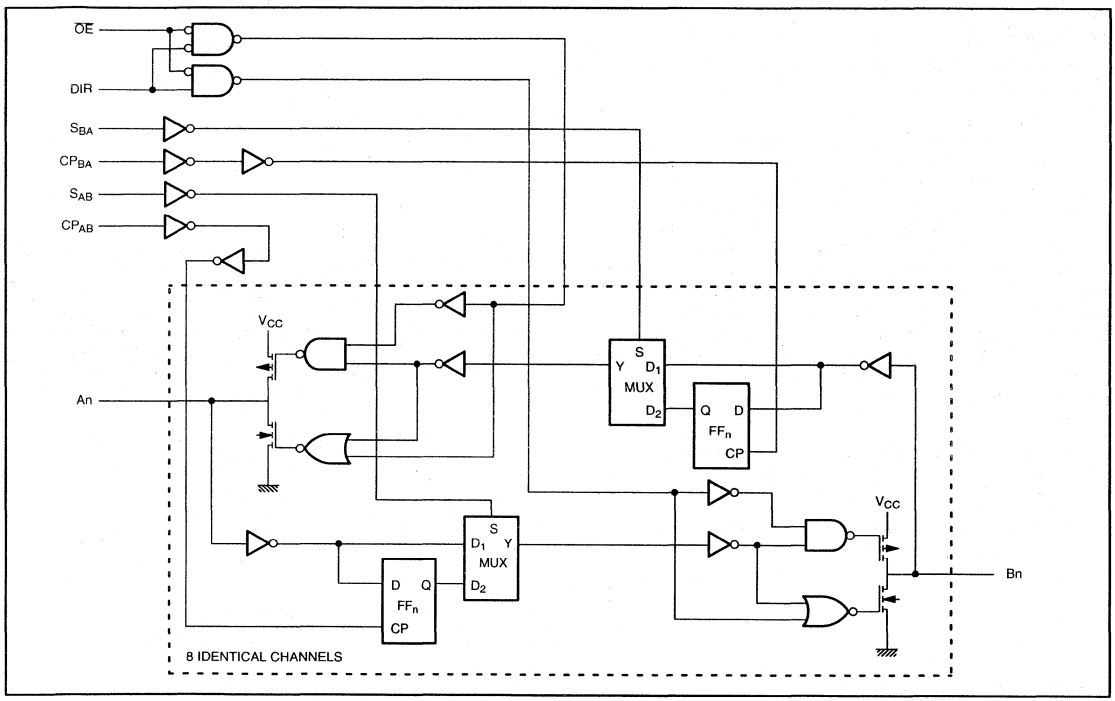
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC646D	24	SO	Plastic	SO24/SOT137A
74LVC646DB	24	SSOP	Plastic	SSOP24/SOT340
74LVC646PW	24	TSSOP	Plastic	TSSOP24/SOT355

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O *		OUTPUTS
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A0–A7	B0–B7	
X X	X X	↑ X	X ↑	X X	X X	Input un*	un* Input	Store A, B unspecified* Store B, A unspecified*
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data, isolation hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real-time B data to A bus Stored B data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real-time data to B bus Stored A data to B bus

* The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = Unspecified
H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH level transition

Octal transceiver/register with dual enable; 3-State 74LVC652

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- In accordance with JEDEC standard no. 8-1A
- Flow-through pin-out architecture
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels

DESCRIPTION

The 74LVC652 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC652 consists of 8 non-inverting bus transceiver circuits with 3-State outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the "A" or "B" or both buses, will be stored in the internal registers, at the appropriate clock inputs (CP_{AB} or CP_{BA}) regardless of the select inputs (S_{AB} and S_{BA}) or output enable (OE_{AB} and $\overline{OE}_{BA}$) control inputs. Depending on the select inputs S_{AB} and S_{BA} data can directly go from input to output (real time mode) or data can be controlled by the clock (storage mode), this is when the OE_n inputs this operating mode permits. The output enable inputs OE_{AB} and $\overline{OE}_{BA}$ determine the operation mode of the transceiver. When OE_{AB} is LOW, no data transmission from A_n to B_n is possible and when $\overline{OE}_{BA}$ is HIGH, there is no data transmission from B_n to A_n possible. When S_{AB} and S_{BA} are in the real time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OE_{AB} and $\overline{OE}_{BA}$. In this configuration each output reinforces its input. The 74LVC652 is functionally identical to the 74LVC651, but has non-inverting data paths.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An, Bn to Bn, An	C_L = 50pF; V_{CC} = 3.3V	5.0	ns
f_{max}	Maximum clock frequency		150	MHz
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	45	pF

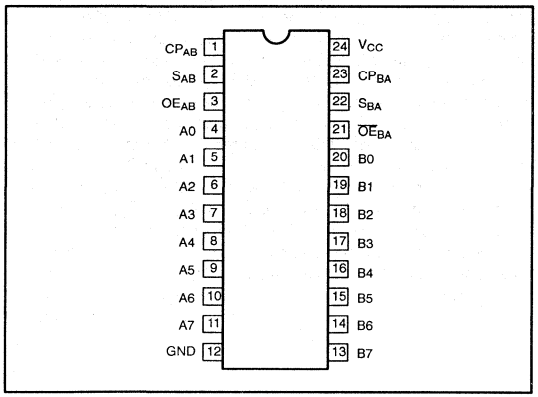
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC652D	24	SO	Plastic	SO24/SOT137A
74LVC652DB	24	SSOP	Plastic	SSOP14/SOT340
74LVC652PW	24	TSSOP	Plastic	TSSOP14/SOT355

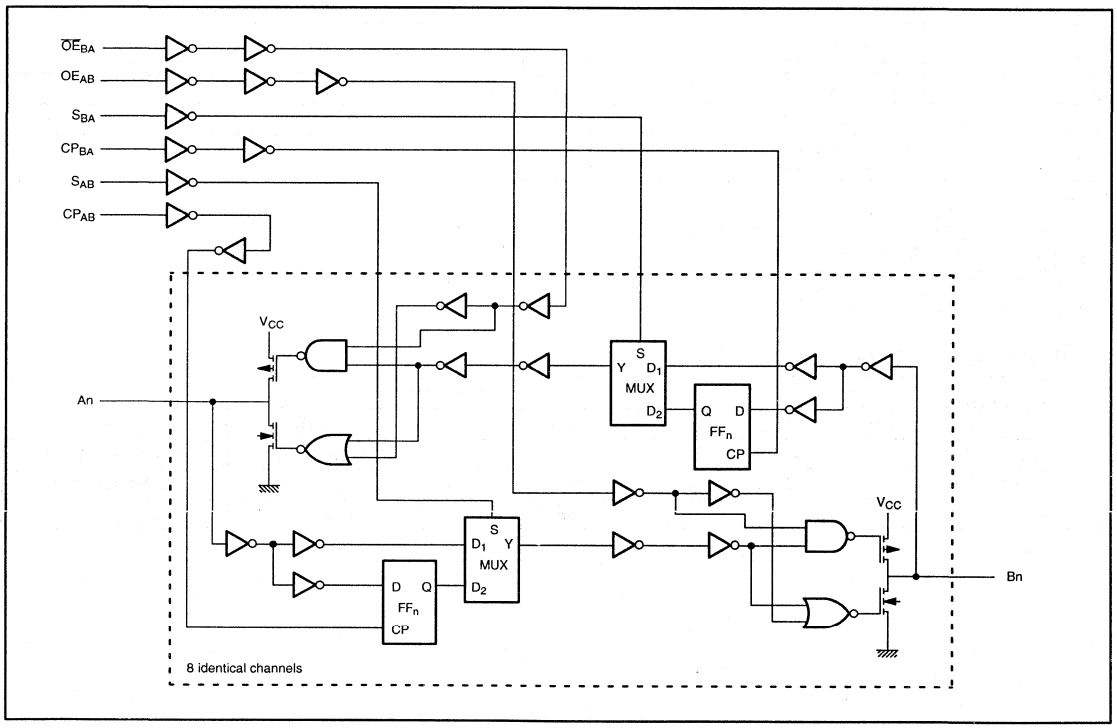
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	CP_{AB}	A to B clock input (LOW-to-HIGH edge triggered)
2	S_{AB}	Select A to B source input
3	OE_{AB}	Output enable B to A input (active LOW)
4, 5, 6, 7, 8, 9, 10, 11	A0 – A7	A data inputs/outputs
12	GND	Ground (0V)
20, 19, 18, 17, 16, 15, 14, 13	B0 – B7	B data inputs/outputs
21	$\overline{OE}_{AB}$	Output enable A to B input
22	S_{BA}	Select B to A source input
23	CP_{BA}	B to A clock input (LOW-to-HIGH, edge-triggered)
24	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A_0 to A_7	B_0 to B_7	
L	H	H or L	H or L	X	X	input	input	isolation
L	H	↑	↑	X	X			store A and B data
X	H	↑	H or L	X	X	input	un*	store A, hold B
H	H	↑	↑	L	X	input	output	store A in both registers
L	X	H or L	↑	X	X	un*	input	hold A, store B
L	L	↑	↑	X	L	output	input	store B in both registers
L	L	X	X	X	L	output	input	real time B data to A bus
L	L	X	H or L	X	H			stored B data to A bus
H	H	X	X	L	X	input	output	real-time A data to B bus
H	H	H or L	X	H	X			stored A data to B bus
H	L	H or L	H or L	H	H	output	output	stored A data to B bus and stored B data to A bus

* The data output functions may be enabled or disabled by various signals at the OE_{AB} and $\overline{OE}_{BA}$ inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

10-bit D-type flip-flop; positive-edge trigger; 3-State 74LVC821

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages upto 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- 8-bit positive edge-triggered register
- Independent register and 3-State buffer operation
- Flow-through pin-out architecture
- Output drive capability 50Ω transmission lines at 85°C

DESCRIPTION

The 74LVC821 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC821 is a 10-bit D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-State outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The ten flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the ten flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-State. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Qn	C_L = 50pF V_{CC} = 3.3V	4.8	ns
f_{max}	maximum clock frequency		150	MHz
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1, 2	28	pF

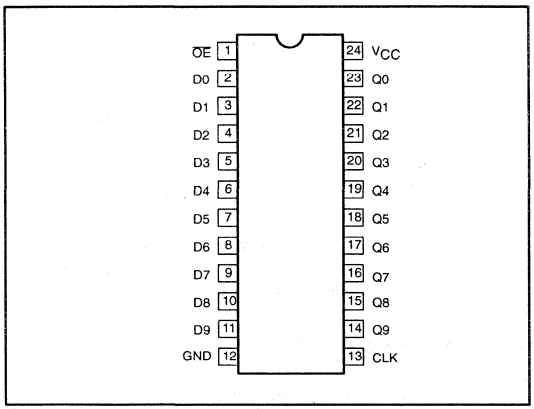
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC821D	24	SO	Plastic	SO14/SOT137
74LVC821DB	24	SSOP	Plastic	SSOP14/SOT340
74LVC821PW	24	TSSOP	Plastic	TSSOP14/SOT355

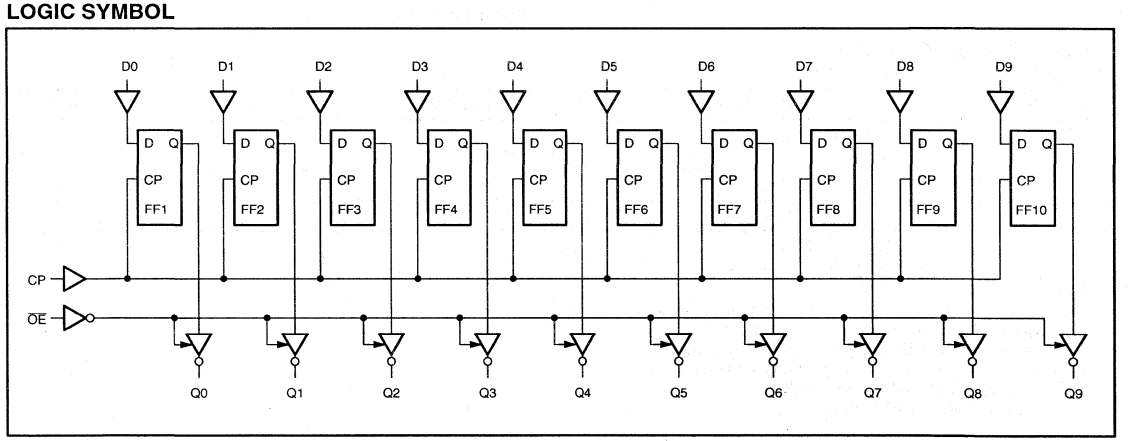
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	D0 – D9	Data inputs
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	Q0 – Q9	3-State flip-flop outputs
12	GND	Ground (0V)
13	CP	clock input (LOW-to-HIGH, edge-triggered)
24	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0 to Q_9
Load and read register	L L	↑ ↑	l h	L H	L H
Load register and disable outputs	H H	↑ ↑	l h	L H	Z Z
Hold	L	H or L	X	NC	NC

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH clock transition
NC = no change

9-bit D-type flip-flop; positive-edge trigger; 3-State 74LVC823

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages upto 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- 8-bit positive edge-triggered register
- Independent register and 3-State buffer operation
- Flow-through pin-out architecture
- Output drive capability 50 Ω transmission lines at 85°C

DESCRIPTION

The 74LVC823 is a low-power, low-voltage, high-performance, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC823 is a 9-bit D-type flip-flop with common clock (CP), Clock Enable ($\overline{CE}$), Master Reset ($\overline{MR}$) and 3-State outputs for bus oriented applications.

The nine flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition, provided $\overline{CE}$ is LOW. When $\overline{CE}$ is HIGH the flip-flops hold their data.

A low on $\overline{MR}$ resets all flip-flops.

When $\overline{OE}$ is LOW, the contents of the nine flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Qn	C_L = 50pF V_{CC} = 3.3V	4.8	ns
f_{max}	Maximum clock frequency		150	MHz
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1, 2	28	pF

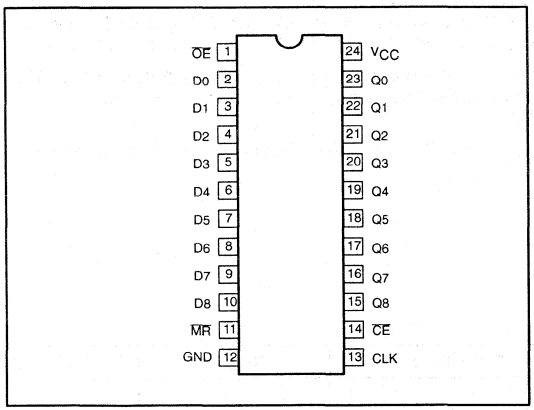
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC823D	24	SO	Plastic	SO14/SOT137
74LVC823DB	24	SSOP	Plastic	SSOP14/SOT340
74LVC823PW	24	TSSOP	Plastic	TSSOP14/SOT355

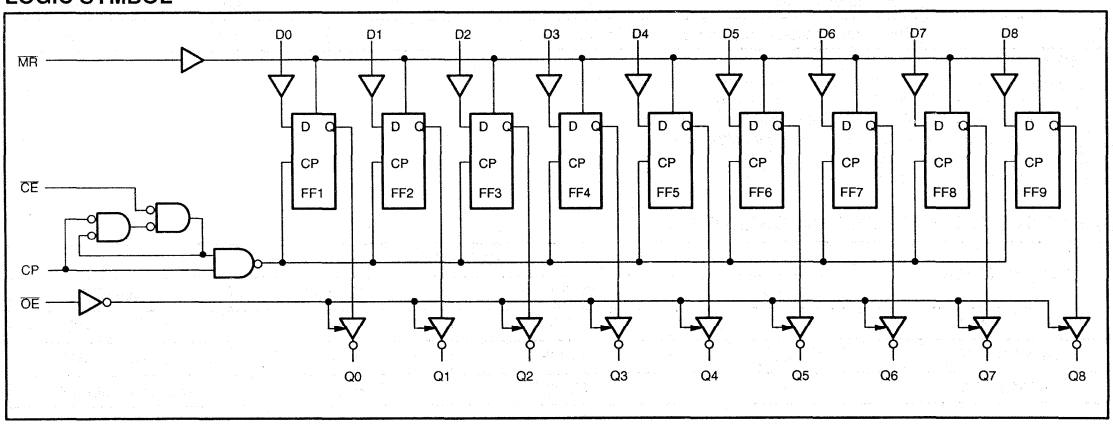
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9, 10	D0 – D8	Data inputs
11	$\overline{MR}$	Mater Reset (active LOW)
12	GND	Ground (0V)
13	CP	Clock Pulse (active rising)
14	$\overline{CE}$	Clock Enable (active LOW)
23, 22, 21, 20, 19, 18, 17, 16, 15	Q0 – Q8	3-State flip-flop outputs
24	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

OPERATING MODES	INPUTS					INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	$\overline{MR}$	$\overline{CE}$	CP	D_n		Q_0 to Q_8
Clear	L	L	X	X	X	L	L
Load and read register	L L	H H	L L	↑ ↑	l h	L H	L H
Load register and disable outputs	H H	H H	L L	X X	l h	L H	Z Z
Hold	L	H	H	NC	X	NC	NC

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH clock transition
NC= no change

10-bit buffer/line driver; 3-State | 74LVC827

FEATURES

- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC} = 3.3V, T_{amb} = 25°C.
- Typical V_{OHV} (output V_{OH} undershoot) > 2V at V_{CC} = 3.3V, T_{amb} = 25°C.
- Non-inverting outputs
- Output capability: bus driver
- I_{CC} category: MSI

DESCRIPTION

The 74LVC827 is a low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC827 is a 10-bit buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs $\overline{OE}1$ and $\overline{OE}2$.

A HIGH on $\overline{OE}n$ causes the outputs to assume a high impedance OFF-state.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Yn	C_L = 15pF V_{CC} = 3.3V	10	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1, 2	37	pF

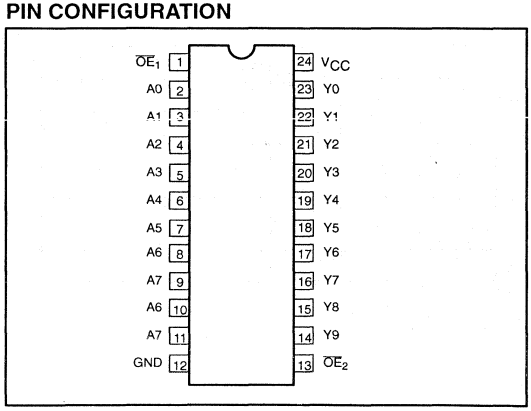
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC827D	24	SO	Plastic	SO24/SOT137
74LVC827DB	24	SSOP	Plastic	SOP24/SOT340
74LVC827PW	24	TSSOP	Plastic	TSSOP24/SOT355

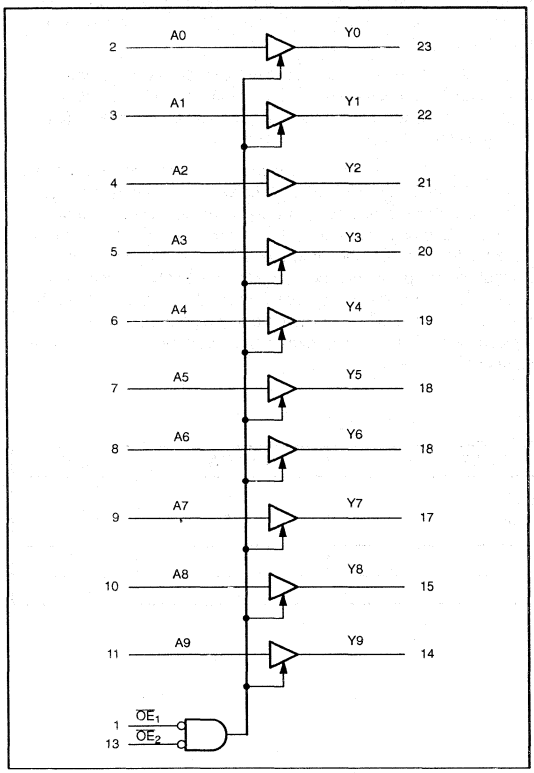
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 13	$\overline{OE}1$, $\overline{OE}2$	Output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	A0 – A9	Data inputs
10	GND	Ground (0V)
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	Y0 – Y9	Bus outputs
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{OE}_1$	$\overline{OE}_2$	nA	nY
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF-state

10-bit transparent latch; 3-State 74LVC841

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC Standard No. 8-1A.
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- Flow-through pin-out architecture
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74LVC841 is a low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC841 is a 10-bit transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all internal latches.

The 74LVC841 consists of ten transparent latches with 3-State true outputs. When LE is HIGH, data at the Dn inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the ten latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

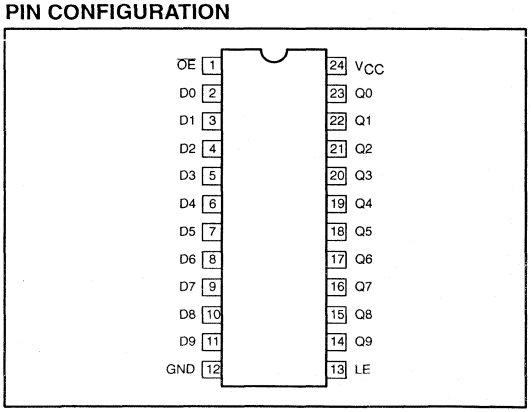
SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay Dn to Qn; LE to Qn	C_L = 50pF V_{CC} = 3.3V	4.3 4.6	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	23	pF

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC841D	24	SO	Plastic	SO24/SOT137
74LVC841DB	24	SSOP	Plastic	SOP24/SOT340
74LVC841PW	24	TSSOP	Plastic	TSSOP24/SOT355

PIN CONFIGURATION



PIN DESCRIPTION

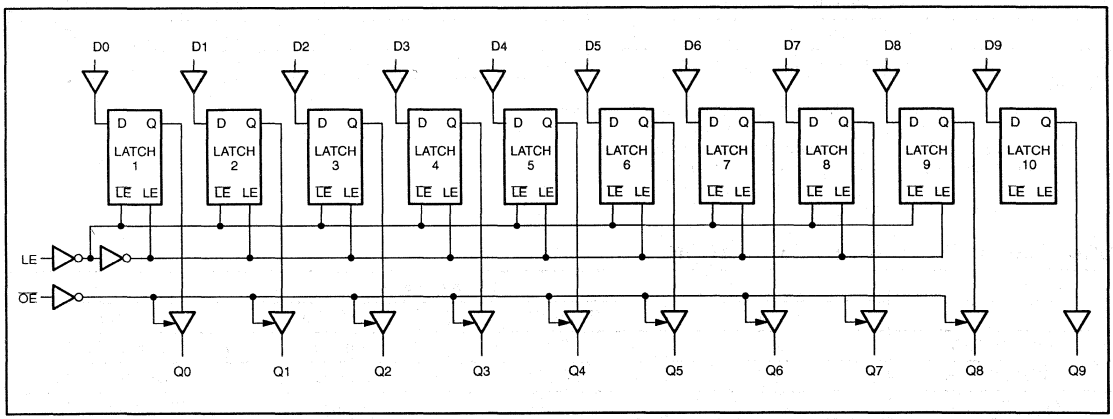
PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	D0 to D9	Data inputs
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	Q0 to Q9	3-State latch inputs
12	GND	Ground (0V)
13	LE	Latch enable input (active HIGH)
14	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	Dn		Q0 to Q8
Enable and read register (transparent mode)	L L	H H	L H	L H	L H
Latch and read register	L L	↓ ↓	l h	L H	L H
Latch register and disable outputs	H H	X X	l h	L H	Z Z
Hold	L	L	X	NC	NC

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
↓ = HIGH-to-LOW LE transition
X = Don't care
Z = High impedance OFF-state
NC = No change

LOGIC DIAGRAM



Octal registered transceiver; 3-State | 74LVC2952

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC Standard No. 8-1A
- CMOS low power consumption
- Inputs accept voltages up to 5.5V
- Flow-through pin-out architecture
- 3-State outputs
- Direct interface with TTL levels
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74LVC2952 is a low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC2952 is an octal non-inverting registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bi-directional buses. Data applied to the inputs is entered and stored on the rising edge of the clock (CP_{nn}) provided that the clock enable ($\overline{CE}_{nn}$) is LOW. The data is then present at the 3-State output buffers, but is only accessible when the output enable input ($\overline{OE}_{nn}$) is LOW. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

The 74LVC2952 is identical to the 74LVC2953 but has non-inverting outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP_{nn} to An, Bn	C_L = 50pF; V_{CC} = 3.3V	3.2	ns
f_{max}	Maximum clock frequency		350	MHz
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1, 2	35	pF

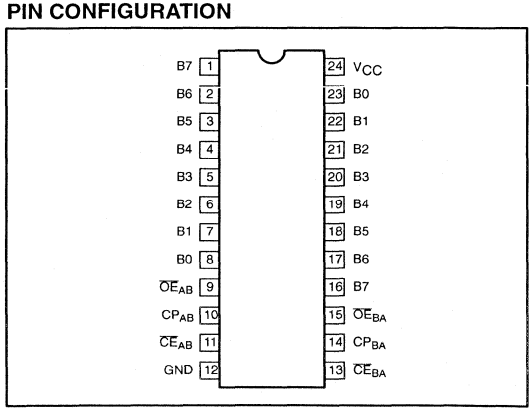
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC2952D	24	SO	Plastic	SO24/SOT137A
74LVC2952DB	24	SSOP	Plastic	SOP24/SOT340
74LVC2952PW	24	TSSOP	Plastic	TSSOP24/SOT355

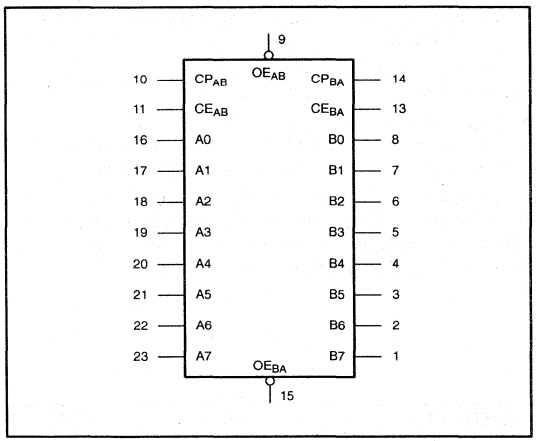
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
8, 7, 6, 5, 4, 3, 2, 1	B0 to B7	B data inputs/outputs
6, 7, 8, 9	GND	Ground (0V)
9, 15	$\overline{OE}_{AB}$, $\overline{OE}_{BA}$	Output enable inputs (active LOW)
10, 14	CP_{AB}, CP_{BA}	Clock inputs
11, 13	$\overline{CE}_{AB}$, $\overline{CE}_{BA}$	Clock enable inputs
16, 17, 18, 19, 20, 21, 22, 23	A0 to A7	A data inputs/outputs
24	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE for register An or Bn

INPUTS			INTERNAL Q	OPERATING MODE
An or Bn	CP_{nn}	$\overline{CE}_{nn}$		
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	Load data

FUNCTION TABLE for output enable

INPUTS	INTERNAL Q	An or Bn OUTPUTS	OPERATING MODE
$\overline{OE}_{nn}$			
H	X	Z	Disable outputs
L	L	L	Enable outputs
L	H	H	Enable outputs

H = HIGH voltage level
L = LOW voltage level
↑ = Low-to-High transition
NC = No change
X = Don't care
Z = High impedance OFF-state

Octal dual supply translating transceiver; 3-State 74LVC4245

FEATURES

- Wide supply voltage range
  3 Volt port: 1.2 to 3.6V
  5 Volt port: 1.2 to 5.5V
- Complies with JEDEC Standard No. 8-1A
- Control Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels

DESCRIPTION

The 74LVC4245 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC4245 is an octal dual supply translating transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions.

It is designed to interface between a 3V bus and a 5V bus in a mixed 3V/5V supply environment.

The 74LVC4245 features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) input for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.

In suspend mode, when V_{CCA} is zero, there will be no current flow from one supply to the other supply. The A-outputs must be set 3-State and the voltage on the A bus must be smaller than V_{diode} (typ. 0.7V). $V_{CCA} \geq V_{CCB}$ (except in suspend mode).

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA to nB nB to nA	C_L = 50pF V_{CCA} = 5.0V V_{CCB} = 3.3V	 4.3 4.3	ns
C_I	Input capacitance		5.0	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1, 2	t.b.f.	pF

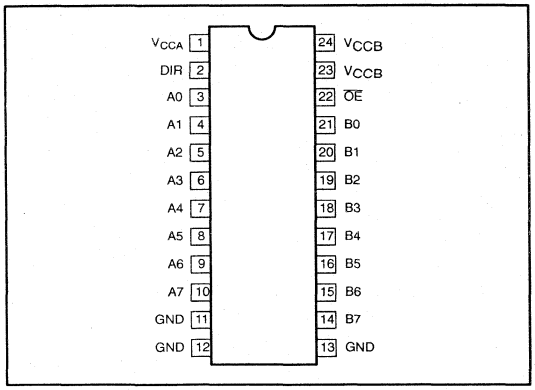
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC4245D	24	SO	Plastic	SO24/SOT137A
74LVC4245DB	24	SSOP	Plastic	SOP24/SOT340
74LVC4245PW	24	TSSOP	Plastic	TSSOP24/SOT355

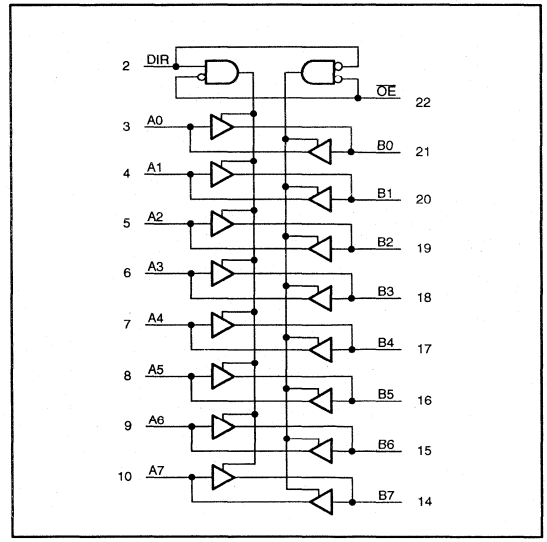
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	V_{CCA}	Positive supply voltage (5V bus)
2	DIR	Direction control
3, 4, 5, 6, 7, 8, 9, 10	A0 to A7	Data inputs
11, 12, 13	GND	Ground (0V)
14, 15, 16, 17, 18, 19, 20, 21	B7 to B0	Data inputs
22	$\overline{OE}$	Output enable input (active LOW)
23, 24	V_{CCB}	Positive supply voltage (3V bus)

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS	
$\overline{OE}$	DIR	An	Bn
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF-state

LVC Netlists

LVC SPICE MODELS

```
* LVC.CIR
* STANDARD LOGIC PRODUCT GROUP
* PHILIPS SEMICONDUCTORS
* 4/6/95
*-------------------------------------------------------------*
* SIMULATION MODULES OF CMOS LOGIC PARTS OF PHILIPS LVC FAMILY *
*                    BERKELEY SPICE FORMAT                    *
*-------------------------------------------------------------*
* IN ORDER TO SIMULATE A SPECIFIC LVC DEVICE, GO TO THE END OF *
* FILE UNDER HEADING 'START RUNNING CIRCUIT MODEL' AND REMOVE  *
* THE COMMENT STATEMENT '*' BEFORE THE REQUIRED DEVICE.        *
* ALL OTHER DEVICES MUST HAVE AN '*' COMMENT STATEMENT.        *
* YOU MAY ONLY SIMULATE ONE DEVICE AT THE TIME.                *
* IF YOU LIKE TO SIMULATE WITH FAST OR SLOW PARAMETERS MODULES:*
* YOU HAVE TO CHANGE THE LAST LETTER OF THE NAMES OF THE SUB-  *
* CIRCUITS STARTING WITH LVC....N, UNDER HEADING 'START OF LVC *
* CIRCUITS DESCRIPTIONS MODELS' INTO IN A 'F' FOR FAST OR A    *
* 'S' FOR SLOW PARAMETERS.                                     *
* THE LOADCIRCUIT AND SIMULATION TIMING SHOULD NORMALLY BE     *
* ADAPTED TO YOUR SPECIFIC SITUATION.                          *
*-------------------------------------------------------------*

*****************************************************************
*                                                               *
* These LVC models represent only one data input and one output  *
* buffer of the device. Devices with a 3-state output buffer,    *
* have also an Output Enable (OE) input. The devices 137/138/139 *
* 157 have also an Input Enable (EN) input. Other control inputs *
* such as DIR or CLK inputs are not modeled. Circuitry between   *
* the input and output buffers are also omitted, such as gates,  *
* registers, latches, mux's and intermediate buffers. One result *
* of this is that LVC models does not show the exact function of *
* the device. Another result of this is that propagation delays  *
* in SPICE will not necessarily match with the published AC      *
* timing specifications in the device datasheet.                 *
*                                                               *
*****************************************************************

.OPTIONS  ACCT   LIST  OPTS  ITL5=25000  NOMOD

**************  PROCESS MODELS ***************

* Nominal parameters
.INC c:\spice\lvc\lvcnomi.cir

* Fast parameters
*.INC c:\spice\lvc\lvcfast.cir

* Slow parameters
*.INC c:\spice\lvc\lvcslow.cir

******* START RUNNING CIRCUIT MODEL ********

*XLVC00   2  4     1  0       INVERT
*XLVC02   2  4     1  0       INVERT
*XLVC04   2  4     1  0       INVERT
*XLVC08   2  4     1  0       INVERTN
*XLVC32   2  4     1  0       INVERTN
```

```
*XLVC38   5  2  4  1  0       INVERT4
* OPEN DRAIN OUTPUT, INP5 = HIGH

*XLVC74   2  4     1  0       INVERTN
* D TO Q IS NON-INV, CLK = SWITCHING

*XLVC86   2  4     1  0       INVERTN

*XLVC109  2  4     1  0       INVERT
* D TO Q IS INV, CLK = SWITCHING

*XLVC125  5  2  4  1  0       INVERT3N
* INP5 = HIGH

*XLVC137  5  2  4  1  0       NANDINVN
* INV TYPE, INP5 = LOW

*XLVC138  5  2  4  1  0       NANDINVN
* INV TYPE, INP5 = LOW

*XLVC139  5  2  4  1  0       NANDINVN
* INV TYPE, INP5 = LOW

*XLVC157  5  2  4  1  0       ANDINVN
* I0 TO Y IS NON-INV, INP5 = LOW

*XLVC240  5  2  4  1  0       INVERT3
* INP5 = HIGH

*XLVC241  5  2  4  1  0       INVERT3N
* INP5 = HIGH

XLVC244   5  2  4  1  0       INVERT3N
* INP5 = HIGH

*XLVC245  5  2  4  1  0       INVERT3N
* INP5 = HIGH

*XLVC373  5  2  4  1  0       INVERT3N
* INP5 = HIGH

*XLVC374  5  2  4  1  0       INVERT3N
* INP5 = HIGH

*XLVC543  5  2  4  1  0       INVERT3N
* INP5 = HIGH

*XLVC544  5  2  4  1  0       INVERT3
* INP5 = HIGH

*XLVC573  5  2  4  1  0       INVERT3N
* INP5 = HIGH

*XLVC574  5  2  4  1  0       INVERT3N
* INP5 = HIGH

*XLVC623  5  2  4  1  0       INVERT3N
* INP5 = HIGH

*XLVC646  5  2  4  1  0       INVERT3N
* INP5 = HIGH
```

```
*XLVC652  5  2  4  1  0        INVERT3N
* INP5 = HIGH

*XLVC821  5  2  4  1  0        INVERT3N
* INP5 = HIGH

*XLVC823  5  2  4  1  0        INVERT3N
* INP5 = HIGH

*XLVC827  5  2  4  1  0        INVERT3N
* INP5 = HIGH

*XLVC841  5  2  4  1  0        INVERT3N
* INP5 = HIGH

*XLVC2952 5  2  4  1  0        INVERT3N
* INP5 = HIGH

*XLVC4245 5  2  4  1  0        INVERT3N
* INP5 = HIGH

************ EXTERNAL TEST LOAD ************
R1    4   0   250
* Use this resistor only with a 3-state output

R2    4   1   250
* Use this resistor only with a 3-State output

C2     4   0   50P

*R1    4   0   500
* Use this resistor only with a totem pole output

*R1    4   1   1000
* Use this resistor only with the 74LVC38 (open drain output)

*******************************************

VDD    1   0   DC  3.0
VIN1   2   0   PULSE  0  3.0  5N  2.5N  2.5N  40N  70N

*VEN    5   0   DC    0
*USE THIS WHEN INP5 = LOW

VEN    5   0   DC  3.0
*USE THIS WHEN INP5 = HIGH

.TRAN  1.000n   70.000n
.PROBE V(4)     V(2)
.PRINT TRAN   V(2)     V(4)
.END
```

LVCNOMI.CIR Subcircuit

```
* LVC SUBCIRCUIT AND PRIMITIVE ELEMENTS LIBRARY
* LVCNOMI.CIR
* NOMINAL PROCESS CORNER
* STANDARD LOGIC PRODUCT GROUP
* PHILIPS SEMICONDUCTORS
* 4/6/95
************************************************
*          NOMINAL N-CHANNEL TRANSISTOR         *
*             UCB-3 PARAMETER SET               *
*                 24-JUNE-1993                  *
************************************************
.MODEL MNEN NMOS
+LEVEL = 3
+KP    = 114E-6
+VTO   = 0.57
+TOX   = 15E-9
+NSUB  = 7.8E16
+GAMMA = 0.70
+PHI   = 0.65
+VMAX  = 187E3
+RS    = 20
+RD    = 20
+XJ    = 0.26E-6
+LD    = 0.11E-6
+DELTA = 1.89
+THETA = 0.072
+ETA   = 0.043
+KAPPA = 0.0
+WD    = 0.0
* USE PARAMETER WD ONLY IN SPICE MODEL 3
* OTHERWISE MAKE FROM THAT LINE A COMMENT
************************************************
*         NOMINAL P-CHANNEL TRANSISTOR          *
*            UCB-3 PARAMETER SET                *
*                24-JUNE-1993                   *
************************************************
.MODEL MPEN PMOS
+LEVEL = 3
+KP    = 43.7E-6
+VTO   = -0.67
+TOX   = 15.0E-9
+NSUB  = 6.0E16
+GAMMA = 0.84
+PHI   = 0.65
+VMAX  = 1.0E6
+RS    = 17.5
+RD    = 17.5
+XJ    = 0.30E-6
+LD    = 0.04E-6
+DELTA = 2.88
+THETA = 0.189
+ETA   = 0.091
+KAPPA = 0.0
+WD    = -0.03E-6
* USE PARAMETER WD ONLY IN SPICE MODEL 3
* OTHERWISE MAKE FROM THAT LINE A COMMENT
```

```
*********************************************
*       START OF SUBCIRCUIT DESCRIPTION     *
*                 SEPT. 1994                *
*********************************************

.SUBCKT LVCINPAN   2   3   50   60
* NOMINAL CASE PARAMETERS
* STANDARD LVC INPUT P-CH 150/0.8 N-CH 70/0.8 INCL. ESD STRUCTURE
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MN1 2 60 60 60 MNEN W=400U L=1.0U AD=7390P AS=208P PD=688U PS=420U
R1  4  2  100
MN2 4 60 60 60 MNEN W= 43U L=1.0U AD=176P AS=208P PD= 58U PS= 58U
MP1 3  4 50 50 MPEN W=150U L=0.8U AD=220P AS=400P PD=175U PS=175U
MN3 3  4 60 60 MNEN W= 70U L=0.8U AD= 80P AS=170P PD= 80U PS= 80U
MP2 5  3 50 50 MPEN W= 10U L=0.8U AD= 22P AS= 22P PD= 25U PS= 25U
MN4 5  3 60 60 MNEN W=  4U L=0.8U AD=  9P AS=  9P PD= 12U PS= 12U
MN5 3  5 60 60 MNEN W= 22U L=1.6U AD= 40P AS= 40P PD= 40U PS= 40U
.ENDS


.SUBCKT LVCINVAN   2   3   50   60
* NOMINAL CASE PARAMETERS
* INTERNAL INVERTER P-CH 30/0.8  N-CH 12/0.8
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 3  2 50 50 MPEN W= 30U L=0.8U AD=35P AS=35P PD=35U PS=30U
MN1 3  2 60 60 MNEN W= 12U L=0.8U AD=30P AS=30P PD=20U PS=15U
.ENDS

.SUBCKT LVCINV1N   2   3   50   60
* NOMINAL CASE PARAMETERS
* INTERNAL INVERTER P-CH 22/0.8  N-CH 16/0.8
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 3  2 50 50 MPEN W= 22U L=0.8U AD=50P AS=50P PD=50U PS=50U
MN1 3  2 60 60 MNEN W= 16U L=0.8U AD=25P AS=25P PD=25U PS=25U
.ENDS

.SUBCKT LVCINV2N   2   3   50   60
* FAST CASE PARAMETERS
* INTERNAL INVERTER P-CH 10/0.8  N-CH 4/0.8
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 3  2 50 50 MPEN W= 10U L=0.8U AD=15P AS=15P PD=15U PS=15U
MN1 3  2 60 60 MNEN W=  4U L=0.8U AD=10P AS=10P PD=10U PS=15U
.ENDS

.SUBCKT LVCNANDN  2   3   4   50   60
* NOMINAL CASE PARAMETERS
* INTERNAL NAND 2-INPUT P-CH 150/0.8  N-CH  180/0.8
* IN1 = 2,  IN2 = 3, OUT = 4,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 4  2  50 50 MPEN W=150U L=0.8U AD=200P AS=400P PD=100U PS=200U
MP2 4  3  50 50 MPEN W=150U L=0.8U AD=200P AS=400P PD=100U PS=200U
MN1 4  2   5 60 MNEN W=180U L=0.8U AD=400P AS=400P PD=400U PS=400U
MN2 5  3  60 60 MNEN W=180U L=0.8U AD=400P AS=400P PD=400U PS=400U
.ENDS
```

```
.SUBCKT LVCANDN  2   3   4   50   60
* NOMINAL CASE PARAMETERS
* INTERNAL NAND 2-INPUT WITH NON-INV INP P-CH 150/0.8  N-CH  180/0.8
* IN1 = 2,  IN2 = 3, OUT = 4,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 4  6  50 50 MPEN W=150U L=0.8U AD=200P AS=400P PD=100U PS=200U
MP2 4  3  50 50 MPEN W=150U L=0.8U AD=200P AS=400P PD=100U PS=200U
MN1 4  6   5 60 MNEN W=180U L=0.8U AD=400P AS=400P PD=400U PS=400U
MN2 5  3  60 60 MNEN W=180U L=0.8U AD=400P AS=400P PD=400U PS=400U
MP3 6  2  50 50 MPEN W= 75U L=0.8U AD=100P AS=200P PD= 50U PS=100U
MN4 6  2  60 60 MNEN W= 30U L=0.8U AD= 60P AS=120P PD= 40U PS= 40U
.ENDS


.SUBCKT LVCOUTAN    2   3   4   50   60
* NOMINAL CASE PARAMETERS
* 3-STATE OUTPUT MODULE
* OE = 2, IN = 3,  OUT = 4,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 5  2 50 50 MPEN W=100U L=0.8U AD=200P AS=400P PD=200U PS=200U
MP2 5  3 50 50 MPEN W=175U L=0.8U AD=225P AS=450P PD=225U PS=225U
MN1 5  3  6 60 MNEN W=100U L=0.8U AD=130P AS=130P PD=150U PS=130U
MN2 6  2 60 60 MNEN W=125U L=0.8U AD=175P AS=250P PD=175U PS=175U
MP3 15 2 50 50 MPEN W= 50U L=0.8U AD= 80P AS= 80P PD= 80U PS= 80U
MN3 15 2 60 60 MNEN W= 20U L=0.8U AD= 40P AS= 40P PD= 45U PS= 45U
MP4 7 15  8 50 MPEN W= 80U L=0.8U AD=250P AS=250P PD=250U PS=250U
MP5 8  3 50 50 MPEN W=100U L=0.8U AD=400P AS=400P PD=350U PS=350U
MN4 7 15 60 60 MNEN W= 75U L=0.8U AD=120P AS=160P PD=120U PS=120U
MN5 7  3 60 60 MNEN W= 60U L=0.8U AD= 80P AS=160P PD= 80U PS= 80U
R1  5 16 25
MP6 4 16 50 50 MPEN W=100U L=0.8U AD=125P AS=125P PD=125U PS=100U
R2 16  9 25
MP7 4  9 50 50 MPEN W=250U L=0.8U AD=250P AS=250P PD=275U PS=275U
R3  9 10 10
MP8 4 10 50 50 MPEN W=245U L=0.8U AD=250P AS=250P PD=275U PS=275U
R4 10 11 10
MP9 4 11 50 50 MPEN W=245U L=0.8U AD=250P AS=250P PD=275U PS=275U
R5  7 17 25
MN6 4 17 60 60 MNEN W= 65U L=0.8U AD= 75P AS= 75P PD=100U PS=100U
R6 17 12 10
MN7 4 12 60 60 MNEN W= 65U L=0.8U AD= 75P AS= 75P PD=100U PS=100U
R7 12 13 10
MN8 4 13 60 60 MNEN W= 50U L=0.8U AD= 50P AS= 50P PD=100U PS= 50U
R8 13 14 10
MN9 4 14 60 60 MNEN W= 50U L=0.8U AD= 50P AS= 50P PD=100U PS= 50U
.ENDS
```

```
.SUBCKT LVCOUTBN    2   3   4   50   60
* NOMINAL CASE PARAMETERS
* 3-STATE OUTPUT MODULE (ONLY N-CHANNEL)
* OE = 2, IN = 3,  OUT = 4,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 5  2 50 50 MPEN W=100U L=0.8U AD=200P AS=400P PD=200U PS=200U
MP2 5  3 50 50 MPEN W=175U L=0.8U AD=225P AS=450P PD=225U PS=225U
MN1 5  3  6 60 MNEN W=100U L=0.8U AD=130P AS=130P PD=150U PS=130U
MN2 6  2 60 60 MNEN W=125U L=0.8U AD=175P AS=250P PD=175U PS=175U
MP3 15 2 50 50 MPEN W= 50U L=0.8U AD= 80P AS= 80P PD= 80U PS= 80U
MN3 15 2 60 60 MNEN W= 20U L=0.8U AD= 40P AS= 40P PD= 45U PS= 45U
MP4 7 15  8 50 MPEN W= 80U L=0.8U AD=250P AS=250P PD=250U PS=250U
MP5 8  3 50 50 MPEN W=100U L=0.8U AD=400P AS=400P PD=350U PS=350U
MN4 7 15 60 60 MNEN W= 75U L=0.8U AD=120P AS=160P PD=120U PS=120U
MN5 7  3 60 60 MNEN W= 60U L=0.8U AD= 80P AS=160P PD= 80U PS= 80U
R5  7 17 25
MN6 4 17 60 60 MNEN W= 65U L=0.8U AD= 75P AS= 75P PD=100U PS=100U
R6 17 12 10
MN7 4 12 60 60 MNEN W= 65U L=0.8U AD= 75P AS= 75P PD=100U PS=100U
R7 12 13 10
MN8 4 13 60 60 MNEN W= 50U L=0.8U AD= 50P AS= 50P PD=100U PS= 50U
R8 13 14 10
MN9 4 14 60 60 MNEN W= 50U L=0.8U AD= 50P AS= 50P PD=100U PS= 50U
.ENDS

.SUBCKT LVCOUT2N    5   4   50   60
* NOMINAL CASE PARAMETERS
* OUTPUT MODULE
* IN1 = 5, OUT = 4,  VCC = 50,  GND = 60
* 21-SEPTEMBER-1993
R1  5 16 25
MP6 4 16 50 50 MPEN W=250U L=0.8U AD=500P AS=500P PD=400U PS=250U
R2 16  9 25
MP7 4  9 50 50 MPEN W=375U L=0.8U AD=750P AS=750P PD=600U PS=375U
R3  9 10 10
MP8 4 10 50 50 MPEN W=375U L=0.8U AD=750P AS=750P PD=600U PS=375U
R4 10 11 10
MP9 4 11 50 50 MPEN W=375U L=0.8U AD=750P AS=750P PD=600U PS=375U
R5  5 17 25
MN6 4 17 60 60 MNEN W=175U L=0.8U AD=175P AS=175P PD=200U PS=175U
R6 17 12 10
MN7 4 12 60 60 MNEN W=175U L=0.8U AD=175P AS=175P PD=200U PS=175U
R7 12 13 10
MN8 4 13 60 60 MNEN W=450U L=0.8U AD=450P AS=450P PD=500U PS=450U
R8 13 14 10
MN9 4 14 60 60 MNEN W=450U L=0.8U AD=450P AS=450P PD=500U PS=450U
.ENDS
```

```
*******************************************************
*      START OF LVC CIRCUITS DESCRIPTION MODELS       *
*                    SEPT. 1994                       *
*******************************************************

.SUBCKT INVERT3  5  2  4  1  90
* INVERTING BUFFER TYPE; 3-STATE
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
* USE THIS MODEL FOR 74LVC240 - 544
* OE = 5, IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1   20  30  50  60      LVCINPAN
XINV1  30  35  50  60      LVCINVAN
XINV2  35  36  50  60      LVCINV1N
XOUT    5  36  40  50  60  LVCOUTAN
L4     4   40   5.97NH
C4    40  90   1.5P
L3     2  20   5.97NH
C1    20  90   1.5P
L1     1  50   6.87NH
R1     1  50   0.1
L2    90  60   6.87NH
C2    50  90   1.5P
C3    60  90   1.5P
.ENDS

.SUBCKT INVERT4  5  2  4  1  90
* INVERTING BUFFER TYPE; OPEN DRAIN
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
* USE THIS MODEL FOR 74LVC 38
* OE = 5, IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1   20  30  50  60      LVCINPAN
XINV1  30  35  50  60      LVCINVAN
XINV2  35  36  50  60      LVCINV1N
XOUT    5  36  40  50  60  LVCOUTBN
L4     4   40   5.97NH
C4    40  90   1.5P
L3     2  20   5.97NH
C1    20  90   1.5P
L1     1  50   6.87NH
R1     1  50   0.1
L2    90  60   6.87NH
C2    50  90   1.5P
C3    60  90   1.5P
.ENDS
```

```
.SUBCKT INVERT3N  5  2  4  1  90
* NON-INVERTING BUFFER TYPE; 3-STATE
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
* USE THIS MODEL FOR 74LVC125/241/244/245/373/374/543/573
* /574/623/646/652/821/823/827/841/2952/4245
* OE = 5, IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1    20  30  50  60       LVCINPAN
XINV    30  35  50  60       LVCINVAN
XOUT     5  35  40  50  60   LVCOUTAN
L4       4  40   5.97NH
C4      40  90   1.5P
L3       2  20   5.97NH
C1      20  90   1.5P
L1       1  50   6.87NH
R1       1  50   0.1
L2      90  60   6.87NH
C2      50  90   1.5P
C3      60  90   1.5P
.ENDS

.SUBCKT INVERTN  2  4  1  90
* NON-INVERTING BUFFER TYPE;
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
* USE THIS MODEL FOR 74LVC 08/32/74/86
* IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1    20  30  50  60       LVCINPAN
XINV1   30  35  50  60       LVCINVAN
XINV2   35  36  50  60       LVCINV1N
XOUT    36  40  50  60       LVCOUT2N
L4       4   40   5.97NH
C4      40  90   1.5P
L3       2  20   5.97NH
C1      20  90   1.5P
L1       1  50   6.87NH
R1       1  50   0.1
L2      90  60   6.87NH
C2      50  90   1.5P
C3      60  90   1.5P
.ENDS

.SUBCKT INVERT  2  4  1  90
*.SUBCKT INVERTN  2  4  1  90
* INVERTING BUFFER TYPE;
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
* USE THIS MODEL FOR 74LVC 00/02/04/109
* IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1    20  30  50  60       LVCINPAN
XINV    30  35  50  60       LVCINVAN
XOUT    35  40  50  60       LVCOUT2N
L4       4  40   5.97NH
C4      40  90   1.5P
L3       2  20   5.97NH
C1      20  90   1.5P
L1       1  50   6.87NH
R1       1  50   0.1
L2      90  60   6.87NH
C2      50  90   1.5P
C3      60  90   1.5P
.ENDS
```

```
.SUBCKT NANDINVN  3  2  4  1  90
* INVERTING 2-NAND BUFFER TYPE
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
* USE THIS MODEL FOR THE 74LVC 137/138/139
* EN = 3, IN =2, OUT = 4, VCC = 1, GND = 90
* OCTOBER-1994
XIN1    20  25       50  60    LVCINPAN
XIN2    30  35       50  60    LVCINPAN
XNAND1 25   35  36   50  60    LVCNANDN
XOUT1   36  40       50  60    LVCOUT2N
L1       2  20    5.29NH
L2       3  30    4.28NH
L3      40   4    3.78NH
L4       1  50    6.08NH
R1       1  50    0.1
L5      60  90    6.08NH
R2      60  90    0.1
C1      20  90    1.5P
C2      30  90    1.5P
C3      40  90    1.5P
C4      50  90    1.5P
C5      60  90    1.5P
.ENDS

.SUBCKT ANDINVN  3  2  4  1  90
* NON-INVERTING 2-NAND BUFFER TYPE
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
* USE THIS MODEL FOR THE 74LVC 157
* EN = 3, IN =2, OUT = 4, VCC = 1, GND = 90
* OCTOBER-1994
XIN1    20  25       50  60    LVCINPAN
XIN2    30  35       50  60    LVCINPAN
XAND1   25  35  36   50  60    LVCANDN
XOUT1   36  40       50  60    LVCOUT2N
L1       2  20    5.29NH
L2       3  30    4.28NH
L3      40   4    3.78NH
L4       1  50    6.08NH
R1       1  50    0.1
L5      60  90    6.08NH
R2      60  90    0.1
C1      20  90    1.5P
C2      30  90    1.5P
C3      40  90    1.5P
C4      50  90    1.5P
C5      60  90    1.5P
.ENDS
```

LVCFAST.CIR Subcircuit

```
* LVC SUBCIRCUIT AND PRIMITIVE ELEMENTS LIBRARY
* LVCFAST.CIR
* FAST PROCESS CORNER
* STANDARD LOGIC PRODUCT GROUP
* PHILIPS SEMICONDUCTORS
* 4/6/95
************************************************
*          FAST N-CHANNEL TRANSISTOR           *
*            UCB-3 PARAMETER SET               *
*                24-JUNE-1993                  *
************************************************
.MODEL MNEF NMOS
+LEVEL = 3
+KP    = 134E-6
+VTO   = 0.46
+TOX   = 13.5E-9
+NSUB  = 8.9E16
+GAMMA = 0.54
+PHI   = 0.65
+VMAX  = 160E3
+RS    = 10
+RD    = 10
+XJ    = 0.31E-6
+LD    = 0.18E-6
+DELTA = 1.46
+THETA = 0.070
+ETA   = 0.025
+KAPPA = 0.0
+WD    = -0.05E-6
* USE PARAMETER WD ONLY IN SPICE MODEL 3
* OTHERWISE MAKE FROM THAT LINE A COMMENT
************************************************
*         FAST P-CHANNEL TRANSISTOR            *
*            UCB-3 PARAMETER SET               *
*                24-JUNE-1993                  *
************************************************
.MODEL MPEF PMOS
+LEVEL = 3
+KP    = 47.3E-6
+VTO   = -0.55
+TOX   = 13.5E-9
+NSUB  = 7.9E16
+GAMMA = 0.65
+PHI   = 0.65
+VMAX  = 1.0E6
+RS    = 10
+RD    = 10
+XJ    = 0.28E-6
+LD    = 0.11E-6
+DELTA = 4.80
+THETA = 0.189
+ETA   = 0.055
+KAPPA = 0.0
+WD    = -0.12E-6
* USE PARAMETER WD ONLY IN SPICE MODEL 3
* OTHERWISE MAKE FROM THAT LINE A COMMENT
```

```
*********************************************
*       START OF SUBCIRCUIT DESCRIPTION     *
*                 SEPT. 1994                *
*********************************************

.SUBCKT LVCINPAF   2   3   50   60
* FAST CASE PARAMETERS
* STANDARD LVC INPUT P-CH 150/0.8 N-CH 70/0.8 INCL. ESD STRUCTURE
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MN1 2 60 60 60 MNEF W=400U L=1.0U AD=7390P AS=208P PD=688U PS=420U
R1  4  2  100
MN2 4 60 60 60 MNEF W= 43U L=1.0U AD=176P AS=208P PD= 58U PS= 58U
MP1 3  4 50 50 MPEF W=150U L=0.8U AD=220P AS=400P PD=175U PS=175U
MN3 3  4 60 60 MNEF W= 70U L=0.8U AD= 80P AS=170P PD= 80U PS= 80U
MP2 5  3 50 50 MPEF W= 10U L=0.8U AD= 22P AS= 22P PD= 25U PS= 25U
MN4 5  3 60 60 MNEF W=  4U L=0.8U AD=  9P AS=  9P PD= 12U PS= 12U
MN5 3  5 60 60 MNEF W= 22U L=1.6U AD= 40P AS= 40P PD= 40U PS= 40U
.ENDS


.SUBCKT LVCINVAF   2   3   50   60
* FAST CASE PARAMETERS
* INTERNAL INVERTER P-CH 30/0.8  N-CH 12/0.8
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 3  2 50 50 MPEF W= 30U L=0.8U AD=35P AS=35P PD=35U PS=30U
MN1 3  2 60 60 MNEF W= 12U L=0.8U AD=30P AS=30P PD=20U PS=15U
.ENDS

.SUBCKT LVCINV1F   2   3   50   60
* FAST CASE PARAMETERS
* INTERNAL INVERTER P-CH 22/0.8  N-CH 16/0.8
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 3  2 50 50 MPEF W= 22U L=0.8U AD=50P AS=50P PD=50U PS=50U
MN1 3  2 60 60 MNEF W= 16U L=0.8U AD=25P AS=25P PD=25U PS=25U
.ENDS

.SUBCKT LVCINV2F   2   3   50   60
* FAST CASE PARAMETERS
* INTERNAL INVERTER P-CH 10/0.8  N-CH 4/0.8
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 3  2 50 50 MPEF W= 10U L=0.8U AD=15P AS=15P PD=15U PS=15U
MN1 3  2 60 60 MNEF W=  4U L=0.8U AD=10P AS=10P PD=10U PS=15U
.ENDS

.SUBCKT LVCNANDF  2   3   4   50   60
* FAST CASE PARAMETERS
* INTERNAL NAND 2-INPUT P-CH 150/0.8  N-CH  180/0.8
* IN1 = 2,  IN2 = 3, OUT = 4,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 4  2  50 50 MPEF W=150U L=0.8U AD=200P AS=400P PD=100U PS=200U
MP2 4  3  50 50 MPEF W=150U L=0.8U AD=200P AS=400P PD=100U PS=200U
MN1 4  2   5 60 MNEF W=180U L=0.8U AD=400P AS=400P PD=400U PS=400U
MN2 5  3  60 60 MNEF W=180U L=0.8U AD=400P AS=400P PD=400U PS=400U
.ENDS
```

```
.SUBCKT LVCANDF  2   3   4   50   60
* FAST CASE PARAMETERS
* INTERNAL NAND 2-INPUT WITH NON-INV INP P-CH 150/0.8  N-CH  180/0.8
* IN1 = 2,  IN2 = 3, OUT = 4,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 4  6  50 50 MPEF W=150U L=0.8U AD=200P AS=400P PD=100U PS=200U
MP2 4  3  50 50 MPEF W=150U L=0.8U AD=200P AS=400P PD=100U PS=200U
MN1 4  6   5 60 MNEF W=180U L=0.8U AD=400P AS=400P PD=400U PS=400U
MN2 5  3  60 60 MNEF W=180U L=0.8U AD=400P AS=400P PD=400U PS=400U
MP3 6  2  50 50 MPEF W= 75U L=0.8U AD=100P AS=200P PD= 50U PS=100U
MN4 6  2  60 60 MNEF W= 30U L=0.8U AD= 60P AS=120P PD= 40U PS= 40U
.ENDS


.SUBCKT LVCOUTAF    2   3   4   50   60
* FAST CASE PARAMETERS
* 3-STATE OUTPUT MODULE
* OE = 2, IN = 3,  OUT = 4,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 5  2 50 50 MPEF W=100U L=0.8U AD=200P AS=400P PD=200U PS=200U
MP2 5  3 50 50 MPEF W=175U L=0.8U AD=225P AS=450P PD=225U PS=225U
MN1 5  3  6 60 MNEF W=100U L=0.8U AD=130P AS=130P PD=150U PS=130U
MN2 6  2 60 60 MNEF W=125U L=0.8U AD=175P AS=250P PD=175U PS=175U
MP3 15 2 50 50 MPEF W= 50U L=0.8U AD= 80P AS= 80P PD= 80U PS= 80U
MN3 15 2 60 60 MNEF W= 20U L=0.8U AD= 40P AS= 40P PD= 45U PS= 45U
MP4 7 15  8 50 MPEF W= 80U L=0.8U AD=250P AS=250P PD=250U PS=250U
MP5 8  3 50 50 MPEF W=100U L=0.8U AD=400P AS=400P PD=350U PS=350U
MN4 7 15 60 60 MNEF W= 75U L=0.8U AD=120P AS=160P PD=120U PS=120U
MN5 7  3 60 60 MNEF W= 60U L=0.8U AD= 80P AS=160P PD= 80U PS= 80U
R1  5 16 25
MP6 4 16 50 50 MPEF W=100U L=0.8U AD=125P AS=125P PD=125U PS=100U
R2 16  9 25
MP7 4  9 50 50 MPEF W=250U L=0.8U AD=250P AS=250P PD=275U PS=275U
R3  9 10 10
MP8 4 10 50 50 MPEF W=245U L=0.8U AD=250P AS=250P PD=275U PS=275U
R4 10 11 10
MP9 4 11 50 50 MPEF W=245U L=0.8U AD=250P AS=250P PD=275U PS=275U
R5  7 17 25
MN6 4 17 60 60 MNEF W= 65U L=0.8U AD= 75P AS= 75P PD=100U PS=100U
R6 17 12 10
MN7 4 12 60 60 MNEF W= 65U L=0.8U AD= 75P AS= 75P PD=100U PS=100U
R7 12 13 10
MN8 4 13 60 60 MNEF W= 50U L=0.8U AD= 50P AS= 50P PD=100U PS= 50U
R8 13 14 10
MN9 4 14 60 60 MNEF W= 50U L=0.8U AD= 50P AS= 50P PD=100U PS= 50U
.ENDS
```

```
.SUBCKT LVCOUTBF    2   3   4   50   60
* FAST CASE PARAMETERS
* 3-STATE OUTPUT MODULE (ONLY N-CHANNEL)
* OE = 2, IN = 3,  OUT = 4,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 5  2 50 50 MPEF W=100U L=0.8U AD=200P AS=400P PD=200U PS=200U
MP2 5  3 50 50 MPEF W=175U L=0.8U AD=225P AS=450P PD=225U PS=225U
MN1 5  3  6 60 MNEF W=100U L=0.8U AD=130P AS=130P PD=150U PS=130U
MN2 6  2 60 60 MNEF W=125U L=0.8U AD=175P AS=250P PD=175U PS=175U
MP3 15 2 50 50 MPEF W= 50U L=0.8U AD= 80P AS= 80P PD= 80U PS= 80U
MN3 15 2 60 60 MNEF W= 20U L=0.8U AD= 40P AS= 40P PD= 45U PS= 45U
MP4 7 15  8 50 MPEF W= 80U L=0.8U AD=250P AS=250P PD=250U PS=250U
MP5 8  3 50 50 MPEF W=100U L=0.8U AD=400P AS=400P PD=350U PS=350U
MN4 7 15 60 60 MNEF W= 75U L=0.8U AD=120P AS=160P PD=120U PS=120U
MN5 7  3 60 60 MNEF W= 60U L=0.8U AD= 80P AS=160P PD= 80U PS= 80U
R5  7 17 25
MN6 4 17 60 60 MNEF W= 65U L=0.8U AD= 75P AS= 75P PD=100U PS=100U
R6 17 12 10
MN7 4 12 60 60 MNEF W= 65U L=0.8U AD= 75P AS= 75P PD=100U PS=100U
R7 12 13 10
MN8 4 13 60 60 MNEF W= 50U L=0.8U AD= 50P AS= 50P PD=100U PS= 50U
R8 13 14 10
MN9 4 14 60 60 MNEF W= 50U L=0.8U AD= 50P AS= 50P PD=100U PS= 50U
.ENDS

.SUBCKT LVCOUT2F    5   4   50   60
* FAST CASE PARAMETERS
* OUTPUT MODULE
* IN1 = 5, OUT = 4,  VCC = 50,  GND = 60
* 21-SEPTEMBER-1993
R1  5 16 25
MP6 4 16 50 50 MPEF W=250U L=0.8U AD=500P AS=500P PD=400U PS=250U
R2 16  9 25
MP7 4  9 50 50 MPEF W=375U L=0.8U AD=750P AS=750P PD=600U PS=375U
R3  9 10 10
MP8 4 10 50 50 MPEF W=375U L=0.8U AD=750P AS=750P PD=600U PS=375U
R4 10 11 10
MP9 4 11 50 50 MPEF W=375U L=0.8U AD=750P AS=750P PD=600U PS=375U
R5  5 17 25
MN6 4 17 60 60 MNEF W=175U L=0.8U AD=175P AS=175P PD=200U PS=175U
R6 17 12 10
MN7 4 12 60 60 MNEF W=175U L=0.8U AD=175P AS=175P PD=200U PS=175U
R7 12 13 10
MN8 4 13 60 60 MNEF W=450U L=0.8U AD=450P AS=450P PD=500U PS=450U
R8 13 14 10
MN9 4 14 60 60 MNEF W=450U L=0.8U AD=450P AS=450P PD=500U PS=450U
.ENDS
```

```
*******************************************************
*     START OF LVC CIRCUITS DESCRIPTION MODELS        *
*                    SEPT. 1994                       *
*******************************************************

.SUBCKT INVERT3  5  2  4  1  90
* INVERTING BUFFER TYPE; 3-STATE
* EQUIVALENT REFERENCE SIMULATION MODEL FAST CASE
* USE THIS MODEL FOR 74LVC240 - 544
* OE = 5, IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1   20  30  50  60      LVCINPAF
XINV1  30  35  50  60      LVCINVAF
XINV2  35  36  50  60      LVCINV1F
XOUT    5  36  40  50  60  LVCOUTAF
L4     4   40   5.97NH
C4    40  90   1.5P
L3     2  20   5.97NH
C1    20  90   1.5P
L1     1  50   6.87NH
R1     1  50   0.1
L2    90  60   6.87NH
C2    50  90   1.5P
C3    60  90   1.5P
.ENDS

.SUBCKT INVERT4  5  2  4  1  90
* INVERTING BUFFER TYPE; OPEN DRAIN
* EQUIVALENT REFERENCE SIMULATION MODEL FAST CASE
* USE THIS MODEL FOR 74LVC 38
* OE = 5, IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1   20  30  50  60      LVCINPAF
XINV1  30  35  50  60      LVCINVAF
XINV2  35  36  50  60      LVCINV1F
XOUT    5  36  40  50  60  LVCOUTBF
L4     4   40   5.97NH
C4    40  90   1.5P
L3     2  20   5.97NH
C1    20  90   1.5P
L1     1  50   6.87NH
R1     1  50   0.1
L2    90  60   6.87NH
C2    50  90   1.5P
C3    60  90   1.5P
.ENDS
```

```
.SUBCKT INVERT3N  5  2  4  1  90
* NON-INVERTING BUFFER TYPE; 3-STATE
* EQUIVALENT REFERENCE SIMULATION MODEL FAST CASE
* USE THIS MODEL FOR 74LVC125/241/244/245/373/374/543/573
* /574/623/646/652/821/823/827/841/2952/4245
* OE = 5, IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1    20  30  50  60      LVCINPAF
XINV    30  35  50  60      LVCINVAF
XOUT     5  35  40  50  60  LVCOUTAF
L4     4  40   5.97NH
C4    40  90   1.5P
L3     2  20   5.97NH
C1    20  90   1.5P
L1     1  50   6.87NH
R1     1  50   0.1
L2    90  60   6.87NH
C2    50  90   1.5P
C3    60  90   1.5P
.ENDS

.SUBCKT INVERTN  2  4  1  90
* NON-INVERTING BUFFER TYPE;
* EQUIVALENT REFERENCE SIMULATION MODEL FAST CASE
* USE THIS MODEL FOR 74LVC 08/32/74/86
* IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1    20  30  50  60      LVCINPAF
XINV1   30  35  50  60      LVCINVAF
XINV2   35  36  50  60      LVCINV1F
XOUT    36  40  50  60      LVCOUT2F
L4     4   40   5.97NH
C4    40  90   1.5P
L3     2  20   5.97NH
C1    20  90   1.5P
L1     1  50   6.87NH
R1     1  50   0.1
L2    90  60   6.87NH
C2    50  90   1.5P
C3    60  90   1.5P
.ENDS

.SUBCKT INVERT  2  4  1  90
*.SUBCKT INVERTN  2  4  1  90
* INVERTING BUFFER TYPE;
* EQUIVALENT REFERENCE SIMULATION MODEL FAST CASE
* USE THIS MODEL FOR 74LVC 00/02/04/109
* IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1    20  30  50  60      LVCINPAF
XINV    30  35  50  60      LVCINVAF
XOUT    35  40  50  60      LVCOUT2F
L4     4  40   5.97NH
C4    40  90   1.5P
L3     2  20   5.97NH
C1    20  90   1.5P
L1     1  50   6.87NH
R1     1  50   0.1
L2    90  60   6.87NH
C2    50  90   1.5P
C3    60  90   1.5P
.ENDS
```

```
.SUBCKT NANDINVN  3  2  4  1  90
* INVERTING 2-NAND BUFFER TYPE
* EQUIVALENT REFERENCE SIMULATION MODEL FAST CASE
* USE THIS MODEL FOR THE 74LVC 137/138/139
* EN = 3, IN =2, OUT = 4, VCC = 1, GND = 90
* OCTOBER-1994
XIN1    20  25       50  60    LVCINPAF
XIN2    30  35       50  60    LVCINPAF
XNAND1 25  35  36  50  60    LVCNANDF
XOUT1  36  40       50  60    LVCOUT2F
L1      2  20   5.29NH
L2      3  30   4.28NH
L3     40   4   3.78NH
L4      1  50   6.08NH
R1      1  50   0.1
L5     60  90   6.08NH
R2     60  90   0.1
C1     20  90   1.5P
C2     30  90   1.5P
C3     40  90   1.5P
C4     50  90   1.5P
C5     60  90   1.5P
.ENDS

.SUBCKT ANDINVN  3  2  4  1  90
* NON-INVERTING 2-NAND BUFFER TYPE
* EQUIVALENT REFERENCE SIMULATION MODEL FAST CASE
* USE THIS MODEL FOR THE 74LVC 157
* EN = 3, IN =2, OUT = 4, VCC = 1, GND = 90
* OCTOBER-1994
XIN1    20  25       50  60    LVCINPAF
XIN2    30  35       50  60    LVCINPAF
XAND1  25  35  36  50  60    LVCANDF
XOUT1  36  40       50  60    LVCOUT2F
L1      2  20   5.29NH
L2      3  30   4.28NH
L3     40   4   3.78NH
L4      1  50   6.08NH
R1      1  50   0.1
L5     60  90   6.08NH
R2     60  90   0.1
C1     20  90   1.5P
C2     30  90   1.5P
C3     40  90   1.5P
C4     50  90   1.5P
C5     60  90   1.5P
.ENDS
```

LVCSLOW.CIR Subcircuit

```
* LVC SUBCIRCUIT AND PRIMITIVE ELEMENTS LIBRARY
* LVCSLOW.CIR
* SLOW PROCESS CORNER
* STANDARD LOGIC PRODUCT GROUP
* PHILIPS SEMICONDUCTORS
* 4/6/95
*********************************************
*          SLOW N-CHANNEL TRANSISTOR          *
*            UCB-3 PARAMETER SET              *
*                24-JUNE-1993                 *
*********************************************
.MODEL MNES NMOS
+LEVEL = 3
+KP    = 96E-6
+VTO   = 0.66
+TOX   = 16.5E-9
+NSUB  = 3.4E15
+GAMMA = 0.72
+PHI   = 0.65
+VMAX  = 199E3
+RS    = 30
+RD    = 30
+XJ    = 0.06E-6
+LD    = 0.04E-6
+DELTA = 1.79
+THETA = 0.075
+ETA   = 0.047
+KAPPA = 0.0
+WD    = 0.06E-6
* USE PARAMETER WD ONLY IN SPICE MODEL 3
* OTHERWISE MAKE FROM THAT LINE A COMMENT
*********************************************
*         SLOW P-CHANNEL TRANSISTOR           *
*            UCB-3 PARAMETER SET              *
*                24-JUNE-1993                 *
*********************************************
.MODEL MPES PMOS
+LEVEL = 3
+KP    = 38.4E-6
+VTO   = -0.75
+TOX   = 16.5E-9
+NSUB  = 2.0E17
+GAMMA = 0.81
+PHI   = 0.65
+VMAX  = 1.0E6
+RS    = 25
+RD    = 25
+XJ    = 0.15E-6
+LD    = 0.0
+DELTA = 3.15
+THETA = 0.190
+ETA   = 0.102
+KAPPA = 0.0
+WD    = 0.03E-6
* USE PARAMETER WD ONLY IN SPICE MODEL 3
* OTHERWISE MAKE FROM THAT LINE A COMMENT
```

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*********************************************
*       START OF SUBCIRCUIT DESCRIPTION     *
*                 SEPT. 1994                *
*********************************************

.SUBCKT LVCINPAS   2   3   50   60
* SLOW CASE PARAMETERS
* STANDARD LVC INPUT P-CH 150/0.8 N-CH 70/0.8 INCL. ESD STRUCTURE
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MN1 2 60 60 60 MNES W=400U L=1.0U AD=7390P AS=208P PD=688U PS=420U
R1  4  2  100
MN2 4 60 60 60 MNES W= 43U L=1.0U AD=176P AS=208P PD= 58U PS= 58U
MP1 3  4 50 50 MPES W=150U L=0.8U AD=220P AS=400P PD=175U PS=175U
MN3 3  4 60 60 MNES W= 70U L=0.8U AD= 80P AS=170P PD= 80U PS= 80U
MP2 5  3 50 50 MPES W= 10U L=0.8U AD= 22P AS= 22P PD= 25U PS= 25U
MN4 5  3 60 60 MNES W=  4U L=0.8U AD=  9P AS=  9P PD= 12U PS= 12U
MN5 3  5 60 60 MNES W= 22U L=1.6U AD= 40P AS= 40P PD= 40U PS= 40U
.ENDS


.SUBCKT LVCINVAS   2   3   50   60
* SLOW CASE PARAMETERS
* INTERNAL INVERTER P-CH 30/0.8  N-CH 12/0.8
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 3  2 50 50 MPES W= 30U L=0.8U AD=35P AS=35P PD=35U PS=30U
MN1 3  2 60 60 MNES W= 12U L=0.8U AD=30P AS=30P PD=20U PS=15U
.ENDS

.SUBCKT LVCINV1S   2   3   50   60
* SLOW CASE PARAMETERS
* INTERNAL INVERTER P-CH 22/0.8  N-CH 16/0.8
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 3  2 50 50 MPES W= 22U L=0.8U AD=50P AS=50P PD=50U PS=50U
MN1 3  2 60 60 MNES W= 16U L=0.8U AD=25P AS=25P PD=25U PS=25U
.ENDS

.SUBCKT LVCINV2S   2   3   50   60
* SLOW CASE PARAMETERS
* INTERNAL INVERTER P-CH 10/0.8  N-CH 4/0.8
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 3  2 50 50 MPES W= 10U L=0.8U AD=15P AS=15P PD=15U PS=15U
MN1 3  2 60 60 MNES W=  4U L=0.8U AD=10P AS=10P PD=10U PS=15U
.ENDS

.SUBCKT LVCNANDS  2   3   4   50   60
* SLOW CASE PARAMETERS
* INTERNAL NAND 2-INPUT P-CH 150/0.8  N-CH  180/0.8
* IN1 = 2,  IN2 = 3, OUT = 4,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 4  2  50 50 MPES W=150U L=0.8U AD=200P AS=400P PD=100U PS=200U
MP2 4  3  50 50 MPES W=150U L=0.8U AD=200P AS=400P PD=100U PS=200U
MN1 4  2   5 60 MNES W=180U L=0.8U AD=400P AS=400P PD=400U PS=400U
MN2 5  3  60 60 MNES W=180U L=0.8U AD=400P AS=400P PD=400U PS=400U
.ENDS
```

```
.SUBCKT LVCANDS  2   3   4   50   60
* SLOW CASE PARAMETERS
* INTERNAL NAND 2-INPUT WITH NON-INV INP P-CH 150/0.8  N-CH  180/0.8
* IN1 = 2,  IN2 = 3, OUT = 4,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 4  6  50 50 MPES W=150U L=0.8U AD=200P AS=400P PD=100U PS=200U
MP2 4  3  50 50 MPES W=150U L=0.8U AD=200P AS=400P PD=100U PS=200U
MN1 4  6   5 60 MNES W=180U L=0.8U AD=400P AS=400P PD=400U PS=400U
MN2 5  3  60 60 MNES W=180U L=0.8U AD=400P AS=400P PD=400U PS=400U
MP3 6  2  50 50 MPES W= 75U L=0.8U AD=100P AS=200P PD= 50U PS=100U
MN4 6  2  60 60 MNES W= 30U L=0.8U AD= 60P AS=120P PD= 40U PS= 40U
.ENDS


.SUBCKT LVCOUTAS    2   3   4   50   60
* SLOW CASE PARAMETERS
* 3-STATE OUTPUT MODULE
* OE = 2, IN = 3,  OUT = 4,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 5  2 50 50 MPES W=100U L=0.8U AD=200P AS=400P PD=200U PS=200U
MP2 5  3 50 50 MPES W=175U L=0.8U AD=225P AS=450P PD=225U PS=225U
MN1 5  3  6 60 MNES W=100U L=0.8U AD=130P AS=130P PD=150U PS=130U
MN2 6  2 60 60 MNES W=125U L=0.8U AD=175P AS=250P PD=175U PS=175U
MP3 15 2 50 50 MPES W= 50U L=0.8U AD= 80P AS= 80P PD= 80U PS= 80U
MN3 15 2 60 60 MNES W= 20U L=0.8U AD= 40P AS= 40P PD= 45U PS= 45U
MP4 7 15  8 50 MPES W= 80U L=0.8U AD=250P AS=250P PD=250U PS=250U
MP5 8  3 50 50 MPES W=100U L=0.8U AD=400P AS=400P PD=350U PS=350U
MN4 7 15 60 60 MNES W= 75U L=0.8U AD=120P AS=160P PD=120U PS=120U
MN5 7  3 60 60 MNES W= 60U L=0.8U AD= 80P AS=160P PD= 80U PS= 80U
R1  5 16 25
MP6 4 16 50 50 MPES W=100U L=0.8U AD=125P AS=125P PD=125U PS=100U
R2 16  9 25
MP7 4  9 50 50 MPES W=250U L=0.8U AD=250P AS=250P PD=275U PS=275U
R3  9 10 10
MP8 4 10 50 50 MPES W=245U L=0.8U AD=250P AS=250P PD=275U PS=275U
R4 10 11 10
MP9 4 11 50 50 MPES W=245U L=0.8U AD=250P AS=250P PD=275U PS=275U
R5  7 17 25
MN6 4 17 60 60 MNES W= 65U L=0.8U AD= 75P AS= 75P PD=100U PS=100U
R6 17 12 10
MN7 4 12 60 60 MNES W= 65U L=0.8U AD= 75P AS= 75P PD=100U PS=100U
R7 12 13 10
MN8 4 13 60 60 MNES W= 50U L=0.8U AD= 50P AS= 50P PD=100U PS= 50U
R8 13 14 10
MN9 4 14 60 60 MNES W= 50U L=0.8U AD= 50P AS= 50P PD=100U PS= 50U
.ENDS
```

```
.SUBCKT LVCOUTBS    2   3   4   50   60
* SLOW CASE PARAMETERS
* 3-STATE OUTPUT MODULE (ONLY N-CHANNEL)
* OE = 2, IN = 3,  OUT = 4,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 5  2 50 50 MPES W=100U L=0.8U AD=200P AS=400P PD=200U PS=200U
MP2 5  3 50 50 MPES W=175U L=0.8U AD=225P AS=450P PD=225U PS=225U
MN1 5  3  6 60 MNES W=100U L=0.8U AD=130P AS=130P PD=150U PS=130U
MN2 6  2 60 60 MNES W=125U L=0.8U AD=175P AS=250P PD=175U PS=175U
MP3 15 2 50 50 MPES W= 50U L=0.8U AD= 80P AS= 80P PD= 80U PS= 80U
MN3 15 2 60 60 MNES W= 20U L=0.8U AD= 40P AS= 40P PD= 45U PS= 45U
MP4 7 15  8 50 MPES W= 80U L=0.8U AD=250P AS=250P PD=250U PS=250U
MP5 8  3 50 50 MPES W=100U L=0.8U AD=400P AS=400P PD=350U PS=350U
MN4 7 15 60 60 MNES W= 75U L=0.8U AD=120P AS=160P PD=120U PS=120U
MN5 7  3 60 60 MNES W= 60U L=0.8U AD= 80P AS=160P PD= 80U PS= 80U
R5  7 17 25
MN6 4 17 60 60 MNES W= 65U L=0.8U AD= 75P AS= 75P PD=100U PS=100U
R6 17 12 10
MN7 4 12 60 60 MNES W= 65U L=0.8U AD= 75P AS= 75P PD=100U PS=100U
R7 12 13 10
MN8 4 13 60 60 MNES W= 50U L=0.8U AD= 50P AS= 50P PD=100U PS= 50U
R8 13 14 10
MN9 4 14 60 60 MNES W= 50U L=0.8U AD= 50P AS= 50P PD=100U PS= 50U
.ENDS

.SUBCKT LVCOUT2S    5   4   50   60
* SLOW CASE PARAMETERS
* OUTPUT MODULE
* IN1 = 5, OUT = 4,  VCC = 50,  GND = 60
* 21-SEPTEMBER-1993
R1  5 16 25
MP6 4 16 50 50 MPES W=250U L=0.8U AD=500P AS=500P PD=400U PS=250U
R2 16  9 25
MP7 4  9 50 50 MPES W=375U L=0.8U AD=750P AS=750P PD=600U PS=375U
R3  9 10 10
MP8 4 10 50 50 MPES W=375U L=0.8U AD=750P AS=750P PD=600U PS=375U
R4 10 11 10
MP9 4 11 50 50 MPES W=375U L=0.8U AD=750P AS=750P PD=600U PS=375U
R5  5 17 25
MN6 4 17 60 60 MNES W=175U L=0.8U AD=175P AS=175P PD=200U PS=175U
R6 17 12 10
MN7 4 12 60 60 MNES W=175U L=0.8U AD=175P AS=175P PD=200U PS=175U
R7 12 13 10
MN8 4 13 60 60 MNES W=450U L=0.8U AD=450P AS=450P PD=500U PS=450U
R8 13 14 10
MN9 4 14 60 60 MNES W=450U L=0.8U AD=450P AS=450P PD=500U PS=450U
.ENDS
```

```
*******************************************************
*      START OF LVC CIRCUITS DESCRIPTION MODELS       *
*                     SEPT. 1994                      *
*******************************************************

.SUBCKT INVERT3  5  2  4  1  90
* INVERTING BUFFER TYPE; 3-STATE
* EQUIVALENT REFERENCE SIMULATION MODEL SLOW CASE
* USE THIS MODEL FOR 74LVC240 - 544
* OE = 5, IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1   20  30  50  60       LVCINPAS
XINV1  30  35  50  60       LVCINVAS
XINV2  35  36  50  60       LVCINV1S
XOUT    5  36  40  50  60   LVCOUTAS
L4     4   40   5.97NH
C4    40  90   1.5P
L3     2  20   5.97NH
C1    20  90   1.5P
L1     1  50   6.87NH
R1     1  50   0.1
L2    90  60   6.87NH
C2    50  90   1.5P
C3    60  90   1.5P
.ENDS

.SUBCKT INVERT4  5  2  4  1  90
* INVERTING BUFFER TYPE; OPEN DRAIN
* EQUIVALENT REFERENCE SIMULATION MODEL SLOW CASE
* USE THIS MODEL FOR 74LVC 38
* OE = 5, IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1   20  30  50  60       LVCINPAS
XINV1  30  35  50  60       LVCINVAS
XINV2  35  36  50  60       LVCINV1S
XOUT    5  36  40  50  60   LVCOUTBS
L4     4   40   5.97NH
C4    40  90   1.5P
L3     2  20   5.97NH
C1    20  90   1.5P
L1     1  50   6.87NH
R1     1  50   0.1
L2    90  60   6.87NH
C2    50  90   1.5P
C3    60  90   1.5P
.ENDS
```

```
.SUBCKT INVERT3N  5  2  4  1  90
* NON-INVERTING BUFFER TYPE; 3-STATE
* EQUIVALENT REFERENCE SIMULATION MODEL SLOW CASE
* USE THIS MODEL FOR 74LVC125/241/244/245/373/374/543/573
* /574/623/646/652/821/823/827/841/2952/4245
* OE = 5, IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1    20  30  50  60       LVCINPAS
XINV    30  35  50  60       LVCINVAS
XOUT     5  35  40  50  60   LVCOUTAS
L4     4  40   5.97NH
C4    40  90   1.5P
L3     2  20   5.97NH
C1    20  90   1.5P
L1     1  50   6.87NH
R1     1  50   0.1
L2    90  60   6.87NH
C2    50  90   1.5P
C3    60  90   1.5P
.ENDS

.SUBCKT INVERTN  2  4  1  90
* NON-INVERTING BUFFER TYPE;
* EQUIVALENT REFERENCE SIMULATION MODEL SLOW CASE
* USE THIS MODEL FOR 74LVC 08/32/74/86
* IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1    20  30  50  60       LVCINPAS
XINV1   30  35  50  60       LVCINVAS
XINV2   35  36  50  60       LVCINV1S
XOUT    36  40  50  60       LVCOUT2S
L4     4   40   5.97NH
C4    40  90   1.5P
L3     2  20   5.97NH
C1    20  90   1.5P
L1     1  50   6.87NH
R1     1  50   0.1
L2    90  60   6.87NH
C2    50  90   1.5P
C3    60  90   1.5P
.ENDS

.SUBCKT INVERT  2  4  1  90
*.SUBCKT INVERTN  2  4  1  90
* INVERTING BUFFER TYPE;
* EQUIVALENT REFERENCE SIMULATION MODEL SLOW CASE
* USE THIS MODEL FOR 74LVC 00/02/04/109
* IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1    20  30  50  60       LVCINPAS
XINV    30  35  50  60       LVCINVAS
XOUT    35  40  50  60       LVCOUT2S
L4     4  40   5.97NH
C4    40  90   1.5P
L3     2  20   5.97NH
C1    20  90   1.5P
L1     1  50   6.87NH
R1     1  50   0.1
L2    90  60   6.87NH
C2    50  90   1.5P
C3    60  90   1.5P
.ENDS
```

```
.SUBCKT NANDINVN  3  2  4  1  90
* INVERTING 2-NAND BUFFER TYPE
* EQUIVALENT REFERENCE SIMULATION MODEL SLOW CASE
* USE THIS MODEL FOR THE 74LVC 137/138/139
* EN = 3, IN =2, OUT = 4, VCC = 1, GND = 90
* OCTOBER-1994
XIN1   20  25       50  60    LVCINPAS
XIN2   30  35       50  60    LVCINPAS
XNAND1 25  35  36   50  60    LVCNANDS
XOUT1  36  40       50  60    LVCOUT2S
L1      2  20   5.29NH
L2      3  30   4.28NH
L3     40   4   3.78NH
L4      1  50   6.08NH
R1      1  50   0.1
L5     60  90   6.08NH
R2     60  90   0.1
C1     20  90   1.5P
C2     30  90   1.5P
C3     40  90   1.5P
C4     50  90   1.5P
C5     60  90   1.5P
.ENDS

.SUBCKT ANDINVN  3  2  4  1  90
* NON-INVERTING 2-NAND BUFFER TYPE
* EQUIVALENT REFERENCE SIMULATION MODEL SLOW CASE
* USE THIS MODEL FOR THE 74LVC 157
* EN = 3, IN =2, OUT = 4, VCC = 1, GND = 90
* OCTOBER-1994
XIN1   20  25       50  60    LVCINPAS
XIN2   30  35       50  60    LVCINPAS
XAND1  25  35  36   50  60    LVCANDS
XOUT1  36  40       50  60    LVCOUT2S
L1      2  20   5.29NH
L2      3  30   4.28NH
L3     40   4   3.78NH
L4      1  50   6.08NH
R1      1  50   0.1
L5     60  90   6.08NH
R2     60  90   0.1
C1     20  90   1.5P
C2     30  90   1.5P
C3     40  90   1.5P
C4     50  90   1.5P
C5     60  90   1.5P
.ENDS
```

Section 7
HLL

SPICE

CONTENTS

Each HLL device requires some combination of an input stage, an output stage, possibly an inverting stage, and some package parasitics. Table 7-1 shows HLL model combinations that correlate input, inverting, and output structures for each part type. Dashes indicate that no inverting stage is needed.

Table 7-1. HLL Model Combinations

HLL	Input Circuit	Inverter Circuit	Output Circuit	Inverting Output	Subcircuit Name
240	HLLINPA	—	HLLOUTA	Yes	INVERTER
241	HLLINPA	HLLINVA	HLLOUTA	No	INVERTERN
244	HLLINPA	HLLINVA	HLLOUTA	No	INVERTERN
245	HLLINPA	HLLINVA	HLLOUTA	No	INVERTERN
373	HLLINPA	HLLINVA	HLLOUTA	No	INVERTERN
374	HLLINPA	HLLINVA	HLLOUTA	No	INVERTERN
533	HLLINPA	—	HLLOUTA	Yes	INVERTER
534	HLLINPA	—	HLLOUTA	Yes	INVERTER
620	HLLINPA	—	HLLOUTA	Yes	INVERTER
623	HLLINPA	HLLINVA	HLLOUTA	No	INVERTERN
640	HLLINPA	—	HLLOUTA	Yes	INVERTER
646	HLLINPA	HLLINVA	HLLOUTA	No	INVERTERN
652	HLLINPA	HLLINVA	HLLOUTA	No	INVERTERN
952	HLLINPA	HLLINVA	HLLOUTA	No	INVERTERN

The data sheet section provides information on each HLL part type. Each data sheet contains a part description, part features, quick reference data, ordering information, pin configuration, logic symbol or diagram, and function table.

To do simulations on a particular part type, refer to the HLL Netlists section of the book. That section contains a file called "HLL.CIR" that contains simulation test circuits for individual device types. The file is also in the HLL directory in the attached diskette, and it is written in the Berkeley SPICE format. Figure 7-1 shows how the test circuit is assembled.

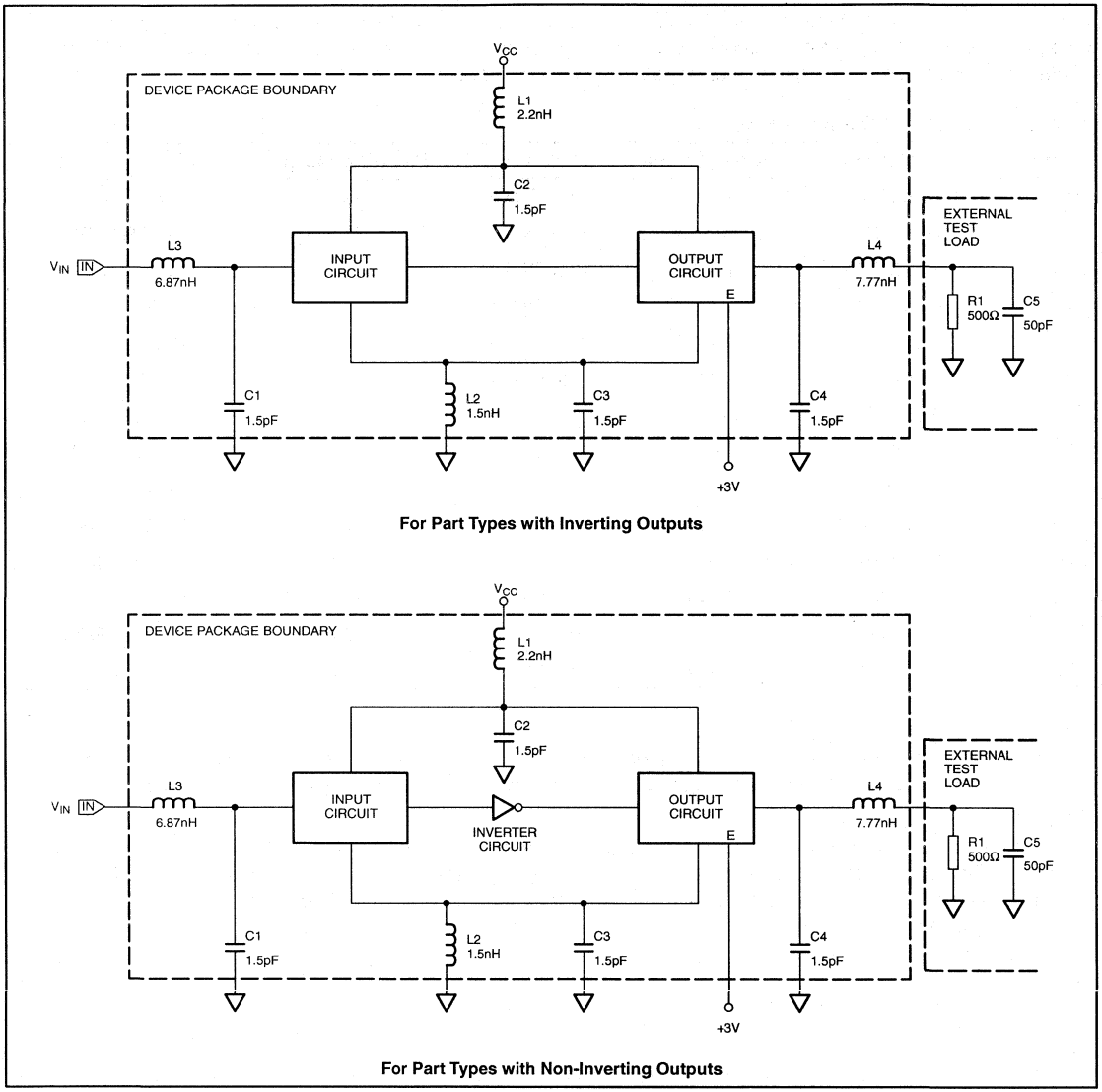


Figure 7-1. Example of HLL Test Circuits

Also in the HLL Netlists section of the book and in the HLL directory of the diskette are files for subcircuits and primitive elements, such as transistors, diodes, and resistors. These files are called HLLXXXX.CIR, the "XXXX" standing for NOMI, FAST, and SLOW, representing the nominal, fast, and slow process corners. The files contain the subcircuits for input, output, and inverter circuits, and they also have package parasitics connected to simulate a device in a package. Package parasitic values can be changed to suit the application. See the Packaging section of the book for values.

For clarification, the following illustration shows how the two programs interact with each other:

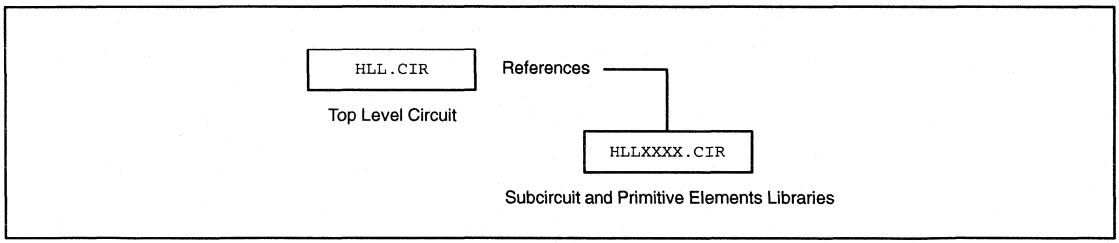


Figure 7-2. HLL SPICE Progam Hierarchy

The top level program, HLL.CIR, uses an AC test set–up with a 3V square wave input, 5ns delay, 2.5ns rise and fall times, 40ns pulse width, 70ns period, 3V V_{CC}, 3V applied to the output enable, and a 500Ω, 50pF load. These conditions may be modified to suit the application. Also, the ".INC" command that specifies the path to reference the other program should be modified to reflect your disk directory structure.

HLL Short-form Datasheets

Octal buffer/line driver; 3-State; inverting 74HL33240

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with the JEDEC 3.3V ± 0.3V supply
- CMOS low power consumption
- Flow-through pin-out architecture
- Low inductance, multiple center power and ground pins for minimum noise and ground bounce
- 3-State outputs
- Direct interface with TTL levels
- 5V to 3.3V level shifting

DESCRIPTION

The 74HL33240 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74HL33240 is an octal inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.

The 74HL33240 is identical to the 74HL244 but has inverting outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay 1An to 1Yn 2An to 2Yn	C_L = 50pF V_{CC} = 3.3V	2.1	ns
C_I	Input capacitance		3.0	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1, 2	35	pF

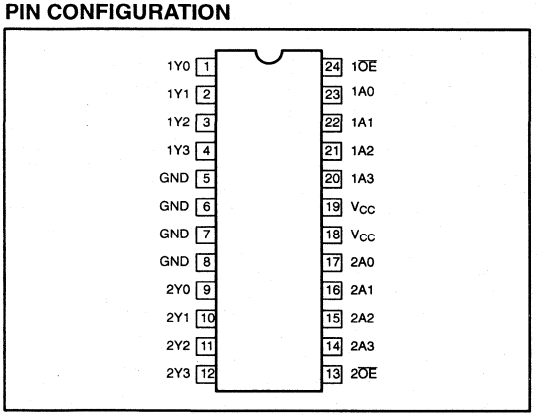
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33240D	24	SO	Plastic	SO24/SOT137A
74HL33240DB	24	SSOP	Plastic	SSOP24/SOT340

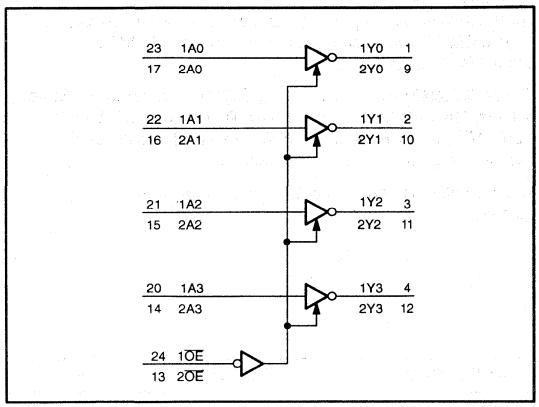
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 2, 3, 4	1Y0 to 1Y3	Bus outputs
5, 6, 7, 8	GND	Ground (0V)
9, 10, 11, 12	2Y0 to 2Y3	Bus outputs
13	$2\overline{OE}$	Output enable input (active LOW)
14, 15, 16, 17	2A3 to 2A0	Data inputs
18, 19	V_{CC}	Positive supply voltage
20, 21, 22, 23	1A3 to 1A0	Data inputs
24	$1\overline{OE}$	Output enable input (active LOW)

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUT
nOE	**nAn**	**nYn**
L	L	H
L	H	L
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF-state

Octal buffer/line driver; 3-State 74HL33241

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with the JEDEC 3.3V ± 0.3V supply
- CMOS low power consumption
- Flow-through pin-out architecture
- Low inductance, multiple center power and ground pins for minimum noise and ground bounce
- 3-State outputs
- Direct interface with TTL levels
- 5V to 3.3V level shifting

DESCRIPTION

The 74HL33241 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74HL33241 is an octal non-inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs $1\overline{OE}$ and 2OE.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay 1An to 1Yn 2An to 2Yn	C_L = 15pF V_{CC} = 3.3V	2.1	ns
C_I	Input capacitance		3.0	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1, 2	35	pF

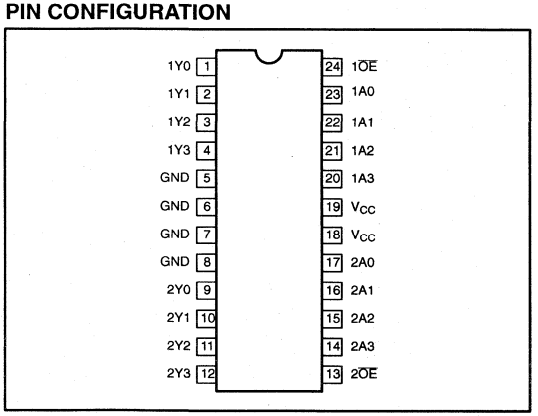
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33241D	24	SO	Plastic	SO24/SOT137A
74HL33241DB	24	SSOP	Plastic	SSOP24/SOT340

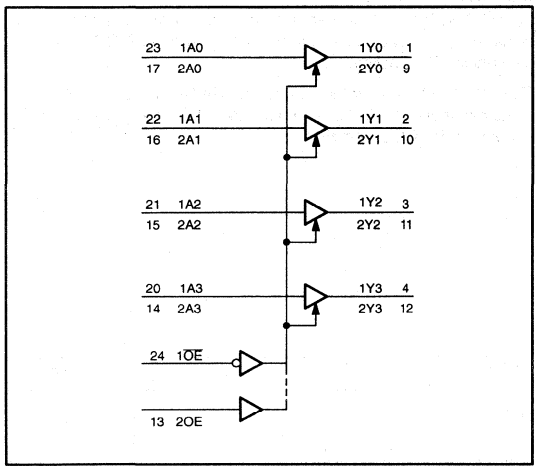
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 2, 3, 4	1Y0 to 1Y3	Bus outputs
5, 6, 7, 8	GND	Ground (0V)
9, 10, 11, 12	2Y0 to 2Y3	Bus outputs
13	2OE	Output enable input (active HIGH)
14, 15, 16, 17	2A3 to 2A0	Data inputs
18, 19	V_{CC}	Positive power supply
20, 21, 22, 23	1A3 to 1A0	Data inputs
24	$1\overline{OE}$	Output enable input (active LOW)

LOGIC SYMBOL



FUNCTION TABLES

INPUTS		OUTPUT
$1\overline{OE}$	1An	1Yn
L	L	L
L	H	H
H	X	Z

INPUTS		OUTPUT
2OE	2An	2Yn
H	L	L
H	H	H
L	X	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF-state

Octal buffer/line driver; 3-State 74HL33244

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with the JEDEC 3.3V ± 0.3V supply
- CMOS low power consumption
- Flow-through pin-out architecture
- Low inductance, multiple center power and ground pins for minimum noise and ground bounce
- 3-State outputs
- Direct interface with TTL levels
- 5V to 3.3V level shifting

DESCRIPTION

The 74HL33244 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74HL33244 is an octal non-inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.

The 74HL33244 is identical to the 74HL33240 but has non-inverting outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay 1An to 1Yn 2An to 2Yn	C_L = 15pF V_{CC} = 3.3V	2.1	ns
C_I	Input capacitance		3.0	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1, 2	35	pF

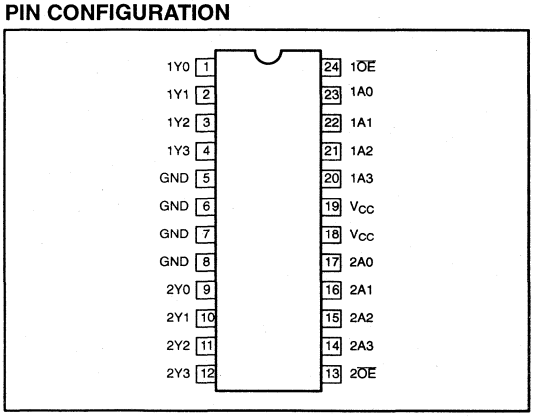
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33244D	24	SO	Plastic	SO24/SOT137A
74HL33244DB	24	SSOP	Plastic	SSOP24/SOT340

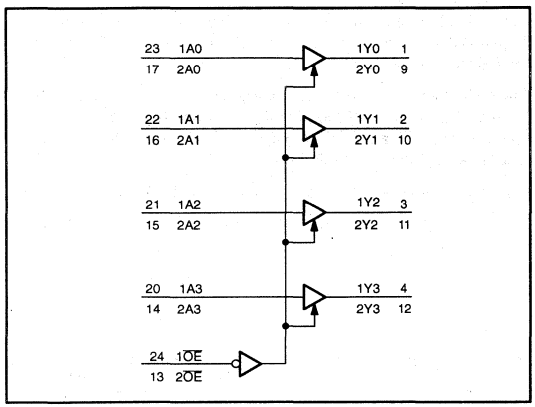
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 2, 3, 4	1Y0 to 1Y3	Bus outputs
5, 6, 7, 8	GND	Ground (0V)
9, 10, 11, 12	2Y0 to 2Y3	Bus outputs
13	$2\overline{OE}$	Output enable input (active LOW)
14, 15, 16, 17	2A3 to 2A0	Data inputs
18, 19	V_{CC}	Positive power supply
20, 21, 22, 23	1A3 to 1A0	Data inputs
24	$1\overline{OE}$	Output enable input (active LOW)

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nAn	nYn
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF-state

Octal transceiver with direction pin; 3-State 74HL33245

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with the JEDEC 3.3V ± 0.3V supply
- CMOS low power consumption
- Flow-through pin-out architecture
- Low inductance, multiple center power and ground pins for minimum noise and ground bounce
- Non-inverting 3-State outputs
- Direct interface with TTL levels

DESCRIPTION

The 74HL33245 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74HL33245 is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The 74HL33245 features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) input for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.

The 74HL33245 is identical to the 74HL33640 but has true (non-inverting) outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Bn; Bn to An	C_L = 50pF V_{CC} = 3.3V	2.2	ns
C_I	Input capacitance		3.0	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1, 2	35	pF

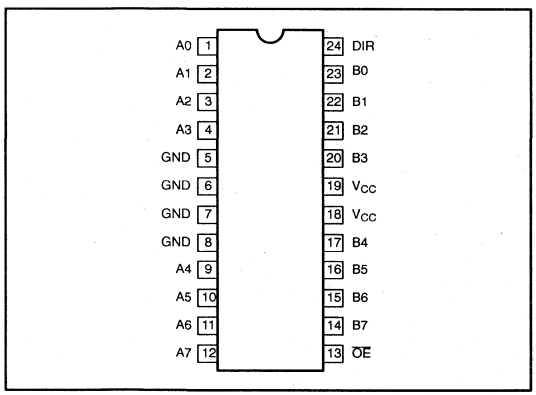
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33245D	24	SO	Plastic	SO24/SOT137A
74HL33245DB	24	SSOP	Plastic	SSOP24/SOT340

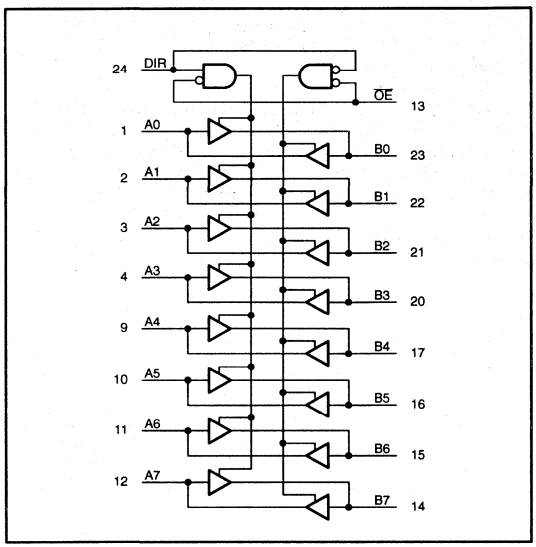
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	A0 to A7	Data inputs/outputs
5, 6, 7, 8	GND	Ground (0V)
13	$\overline{OE}$	Output enable input (active LOW)
14, 15, 16, 17, 20, 21, 22, 23	B7 to B0	Data inputs/outputs
18, 19	V_{CC}	Positive supply voltage
24	DIR	Direction control

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		INPUTS/OUTPUT	
$\overline{OE}$	DIR	An	Bn
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF-state

Octal D-type transparent latch; 3-State 74HL33373

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with the JEDEC 3.3V ± 0.3V supply
- CMOS low power consumption
- Flow-through pin-out architecture
- Low inductance, multiple center power and ground pins for minimum noise and ground bounce
- 3-State outputs
- Direct interface with TTL levels
- 5V to 3.3V level shifting

DESCRIPTION

The 74HL33373 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) are common to all internal latches.

The 74HL33373 consists of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e., a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The 74HL33373 is functionally identical to the 74HL33533, but the 74HL33533 has inverted outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay Dn to Qn; LE to Qn	C_L = 50pF V_{CC} = 3.3V	3.0 3.0	ns
C_I	Input capacitance		3.0	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	25	pF

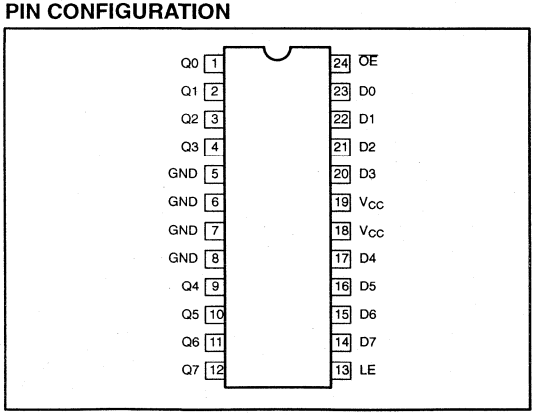
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33373D	24	SO	Plastic	SO24/SOT137A
74HL33373DB	24	SSOP	Plastic	SSOP24/SOT340

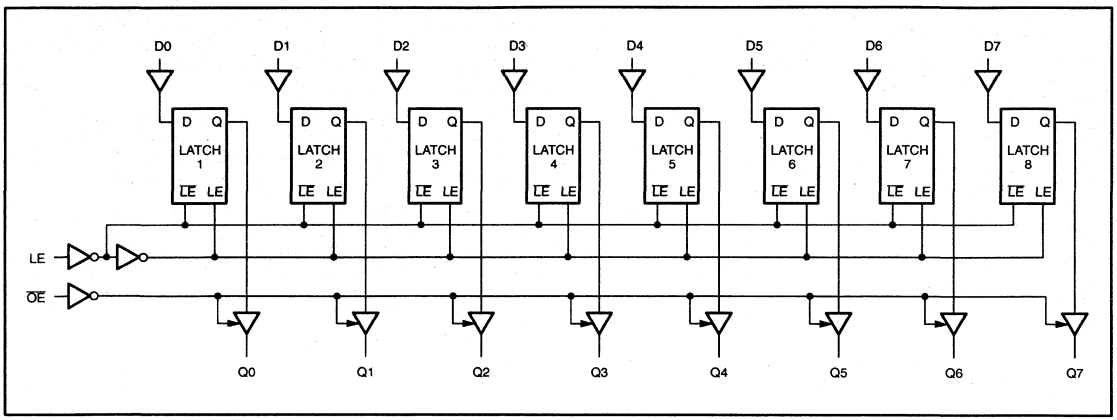
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	Q0 to Q7	Data outputs
5, 6, 7, 8	GND	Ground (0V)
13	LE	Latch enable
23, 22, 21, 20, 17, 16, 15, 14	D0 to D7	Data inputs
18, 19	V_{CC}	Positive supply voltage
24	$\overline{OE}$	Output enable input (active LOW)

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{OE}$	LE	Dn	Q0 to Q7
Enable and read register (transparent mode)	L L	H H	L H	L H
Latch and read register	L L	L L	l h	L H
Latch register and disable outputs	H	X	X	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = Don't care
Z = High impedance OFF-state

Octal D-type flip-flop; positive edge-trigger; 3-State

74HL33374

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- In accordance with the JEDEC 3.3V ± 0.3V supply
- CMOS low power consumption
- Flow-through pin-out architecture
- Low inductance, multiple center power and ground pins for minimum noise and ground bounce
- 3-State outputs
- Direct interface with TTL levels
- 5V to 3.3V level shifting

DESCRIPTION

The 74HL33374 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-State outputs for bus oriented applications. A clock (CP) input and an output enable ($\overline{OE}$) are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the 8 flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The 74HL33374 is functionally identical to the 74HL33534, but has non-inverting outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Qn	C_L = 50pF V_{CC} = 3.3V	3.2	ns
f_{max}	Maximum clock frequency		350	MHz
C_I	Input capacitance		3.0	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1, 2	28	pF

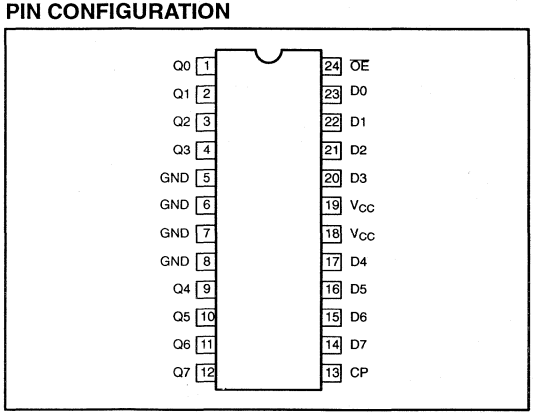
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33374D	24	SO	Plastic	SO24/SOT137A
74HL33374DB	24	SSOP	Plastic	SSOP24/SOT340

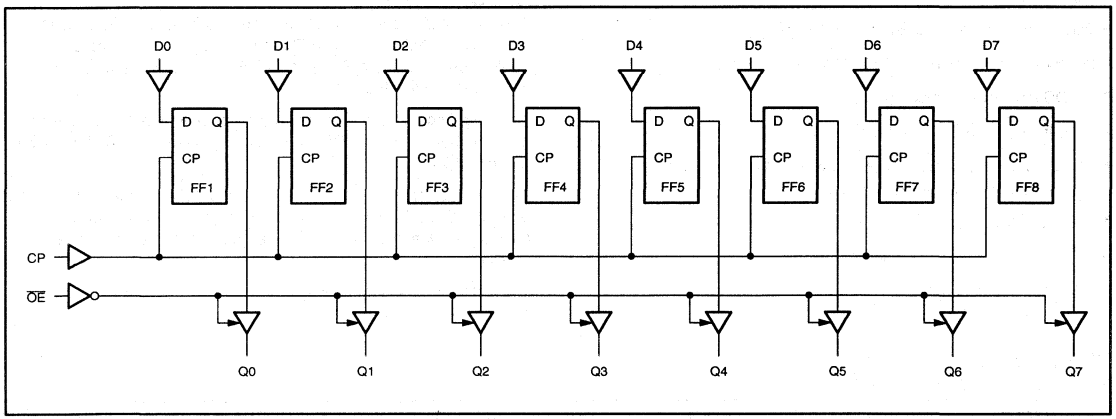
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	Q0 to Q7	Data outputs
5, 6, 7, 8	GND	Ground (0V)
13	CP	Clock input
23, 22, 21, 20, 17, 16, 15, 14	D0 TO D7	Data inputs
18, 19	V_{CC}	Positive supply voltage
24	$\overline{OE}$	Output enable input (active LOW)

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{OE}$	CP	Dn	Q0 to Q7
Load and read register	L L	↑ ↑	l h	L H
Load register and disable outputs	H H	↑ ↑	l h	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
Z = High impedance OFF-state
↑ = LOW-to-HIGH CP transition

Octal D-type transparent latch; 3-State; inverting — 74HL33533

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with the JEDEC 3.3V ± 0.3V supply
- CMOS low power consumption
- Flow-through pin-out architecture
- Low inductance, multiple center power and ground pins for minimum noise and ground bounce
- 3-State outputs
- Direct interface with TTL levels
- 5V to 3.3V level shifting

DESCRIPTION

The 74HL33533 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) are common to all internal latches.

The 74HL33533 consists of eight D-type transparent latches with 3-State inverting outputs. When LE is HIGH, data at the Dn inputs enter the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The 74HL33533 is functionally identical to the 74HL33373, but the 74HL33373 has non-inverted outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay Dn to $\overline{Q}n$; LE to $\overline{Q}n$	C_L = 50pF V_{CC} = 3.3V	3.0 3.0	ns
C_I	Input capacitance		3.0	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	25	pF

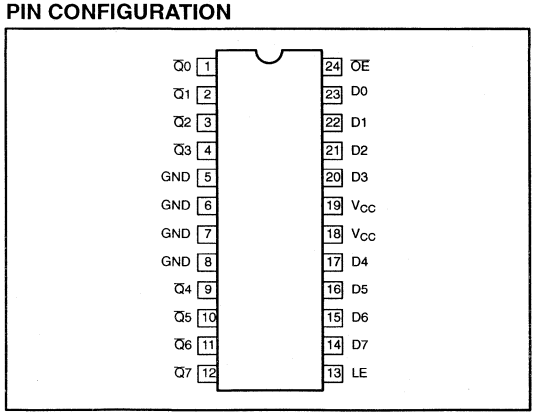
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33533D	24	SO	Plastic	SO24/SOT137A
74HL33533DB	24	SSOP	Plastic	SSOP24/SOT340

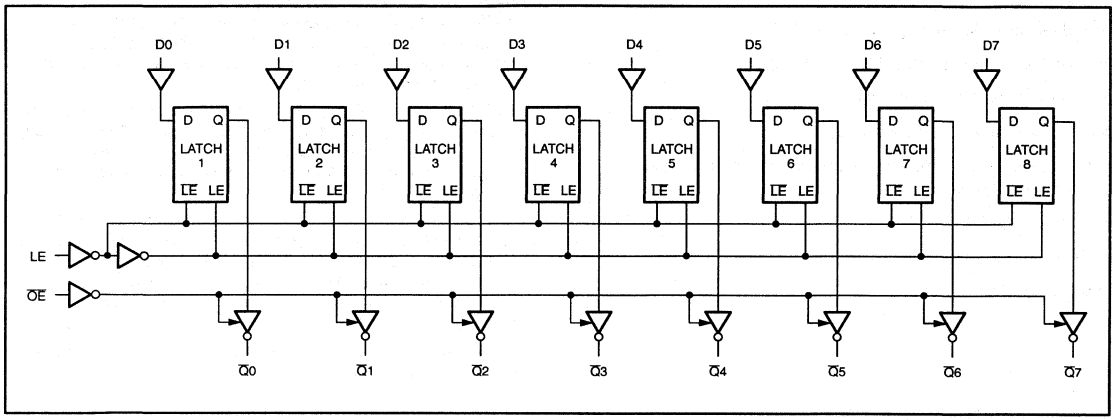
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	$\overline{Q}0$ to $\overline{Q}7$	Data outputs
5, 6, 7, 8	GND	Ground (0V)
13	LE	Latch enable
23, 22, 21, 20, 17, 16, 15, 14	D0 TO D7	Data inputs
18, 19	V_{CC}	Positive supply voltage
24	$\overline{OE}$	Output enable input (active LOW)

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{OE}$	LE	Dn	$\overline{Q0}$ to $\overline{Q7}$
Enable and read register (transparent mode)	L L	H H	L H	H L
Latch and read register	L L	L L	l h	H L
Latch register and disable outputs	H	X	X	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = Don't care
Z = High impedance OFF-state

Octal D-type flip-flop; positive edge-trigger; 3-State; inverting

74HL33534

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with the JEDEC 3.3V ± 0.3V supply
- CMOS low power consumption
- Flow-through pin-out architecture
- Low inductance, multiple center power and ground pins for minimum noise and ground bounce
- 3-State inverting outputs
- Direct interface with TTL levels
- 5V to 3.3V level shifting

DESCRIPTION

The 74HL33534 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-State outputs for bus oriented applications. A clock (CP) input and an output enable ($\overline{OE}$) are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the 8 flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The 74HL33534 is functionally identical to the 74HL33374, but has inverting outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to $\overline{Q}n$	C_L = 50pF V_{CC} = 3.3V	3.2	ns
f_{max}	Maximum clock frequency		350	MHz
C_I	Input capacitance		3.0	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1, 2	28	pF

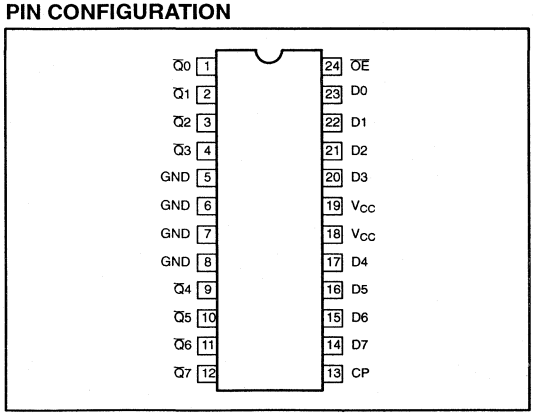
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33534D	24	SO	Plastic	SO24/SOT137A
74HL33534DB	24	SSOP	Plastic	SSOP24/SOT340

PIN CONFIGURATION



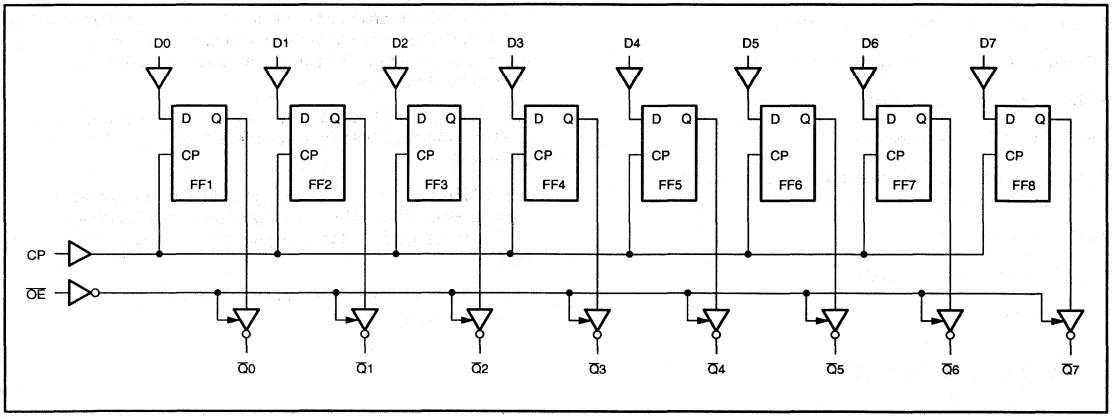
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	$\overline{Q}0$ to $\overline{Q}7$	Data outputs
5, 6, 7, 8	GND	Ground (0V)
13	CP	Clock input
23, 22, 21, 20, 17, 16, 15, 14	D0 TO D7	Data inputs
18, 19	V_{CC}	Positive supply voltage
24	$\overline{OE}$	Output enable input (active LOW)

Octal D-type flip-flop; positive edge-trigger; 3-State; inverting

74HL33534

LOGIC



FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{OE}$	CP	Dn	$\overline{Q0}$ to $\overline{Q7}$
Load and read register	L L	↑ ↑	l h	H L
Load register and disable outputs	H H	↑ ↑	l h	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
Z = High impedance OFF-state
↑ = LOW-to-HIGH CP transition

Octal receiver with dual enable; 3-State; inverting

74HL33620

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with the JEDEC 3.3V ± 0.3V supply
- CMOS low power consumption
- Flow-through pin-out architecture
- Low inductance, multiple center power and ground pins for minimum noise and ground bounce
- Inverting 3-State outputs
- Direct interface with TTL levels

DESCRIPTION

The 74HL33620 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74HL33620 is an octal transceiver featuring inverting 3-State bus compatible outputs in both send and receive directions.

This octal bus transceiver is designed for asynchronous two-way communication between data buses. The control function implementation allows maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the enable inputs (OE_{AB}, $\overline{OE}_{BA}$). The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual enable function configuration gives this transceiver the capability to store data by simultaneous enabling of OE_{AB} and $\overline{OE}_{BA}$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance OFF-state, both sets of bus lines will remain at their last states. The 8-bit codes appearing on the two sets of buses will be complementary.

The 74HL33620 is identical to the 74HL33623 but has inverting outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Bn; Bn to An	C_L = 50pF V_{CC} = 3.3V	2.2	ns
C_I	Input capacitance		3.0	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1, 2	35	pF

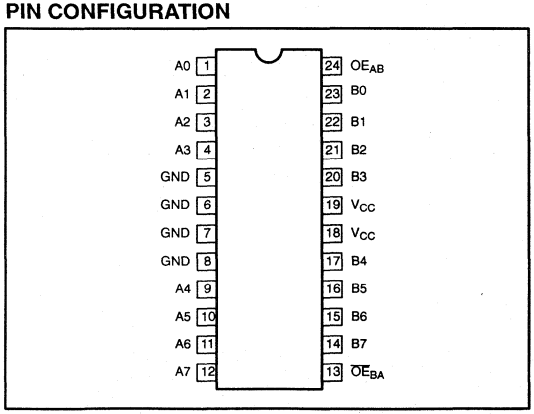
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33620D	24	SO	Plastic	SO24/SOT137A
74HL33620DB	24	SSOP	Plastic	SSOP24/SOT340

PIN CONFIGURATION



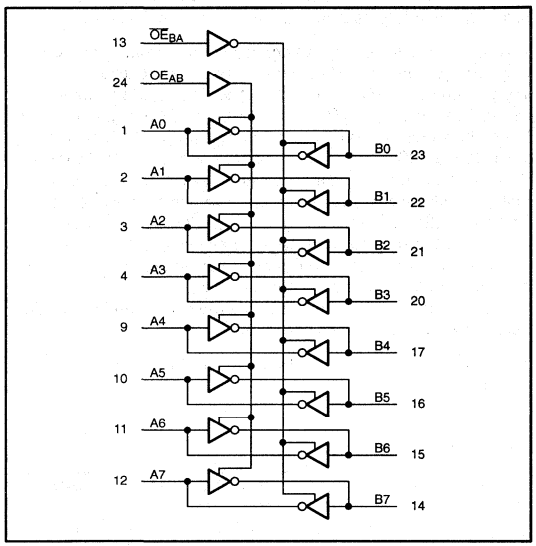
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	A0 to A7	Data inputs/outputs
5, 6, 7, 8	GND	Ground (0V)
13	$\overline{OE}_{BA}$	Output enable input (active LOW)
14, 15, 16, 17, 20, 21, 22, 23	B7 to B0	Data inputs/outputs
18, 19	V_{CC}	Positive supply voltage
24	OE_{AB}	Output enable input (active HIGH)

Octal receiver with dual enable; 3-State; inverting

74HL33620

LOGIC SYMBOL



FUNCTION TABLE

ENABLE INPUTS		OPERATION
OE_{AB}	$\overline{OE}_{BA}$	
L	L	$\overline{B}$ data to A bus
H	H	$\overline{A}$ data to B bus
L	H	Z
H	L	$\overline{B}$ data to A bus $\overline{A}$ data to B bus

H = HIGH voltage level
L = LOW voltage level
Z = High impedance OFF-state

Octal transceiver with dual enable; 3-State 74HL33623

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with the JEDEC 3.3V ±0.3V supply
- CMOS low power consumption
- Flow-through pin-out architecture
- Low inductance, multiple center power and ground pins for minimum noise and ground bounce
- Non-inverting 3-State outputs
- Direct interface with TTL levels

DESCRIPTION

The 74HL33623 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74HL33623 is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions.

This octal bus transceiver is designed for asynchronous two-way communication between data buses. The control function implementation allows maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the enable inputs (OE_{AB}, $\overline{OE}_{BA}$). The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual enable function configuration gives this transceiver the capability to store data by simultaneous enabling of OE_{AB} and $\overline{OE}_{BA}$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance OFF-state, both sets of bus lines will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical.

The 74HL33623 is identical to the 74HL33620 but has true (non-inverting) outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Bn; Bn to An	C_L = 50pF V_{CC} = 3.3V	2.2	ns
C_I	Input capacitance		3.0	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1, 2	35	pF

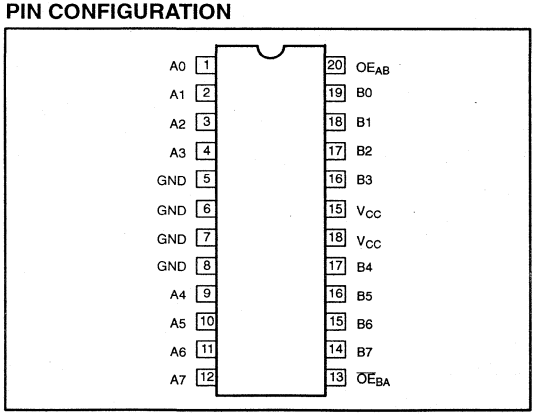
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33623D	24	SO	Plastic	SO24/SOT137A
74HL33623DB	24	SSOP	Plastic	SSOP24/SOT340

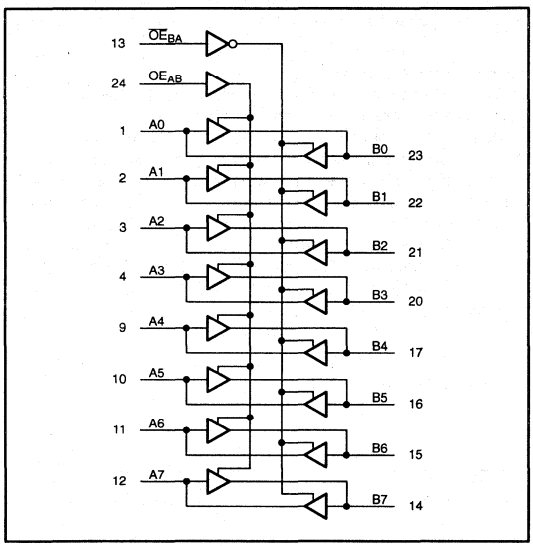
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	A0 to A7	Data inputs/outputs
5, 6, 7, 8	GND	Ground (0V)
13	$\overline{OE}_{BA}$	Output enable input (active LOW)
14, 15, 16, 17, 20, 21, 22, 23	B7 to B0	Data inputs/outputs
18, 19	V_{CC}	Positive supply voltage
24	OE_{AB}	Output enable input (active HIGH)

LOGIC SYMBOL



FUNCTION TABLE

ENABLE INPUTS		OPERATION
OE_{AB}	$\overline{OE}_{BA}$	
L	L	B data to A bus
H	H	A data to B bus
L	H	Z
H	L	B data to A bus A data to B bus

H = HIGH voltage level
L = LOW voltage level
Z = High impedance OFF-state

Octal bus transceiver with direction pin; 3-State inverting

74HL33640

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with the JEDEC 3.3V ± 0.3V supply
- CMOS low power consumption
- Flow-through pin-out architecture
- Low inductance, multiple center power and ground pins for minimum noise and ground bounce
- Inverting 3-State outputs
- Direct interface with TTL levels

DESCRIPTION

The 74HL33640 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74HL33640 is an octal transceiver featuring inverting 3-State bus compatible outputs in both send and receive directions. The 74HL33640 features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) input for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.

The 74HL33640 is identical to the 74HL33245 but has inverting outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Bn; Bn to An	C_L = 50pF V_{CC} = 3.3V	2.2	ns
C_I	Input capacitance		3.0	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1, 2	35	pF

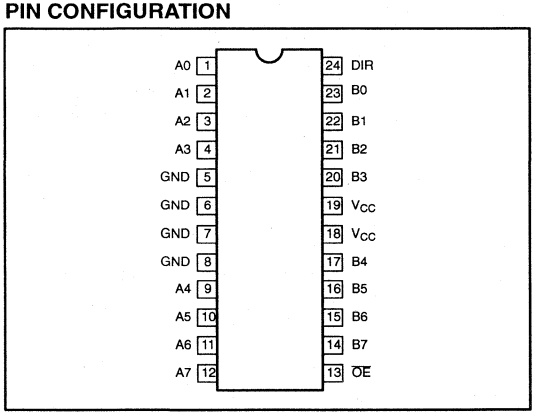
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33640D	24	SO	Plastic	SO24/SOT137A
74HL33640DB	24	SSOP	Plastic	SSOP24/SOT340

PIN CONFIGURATION



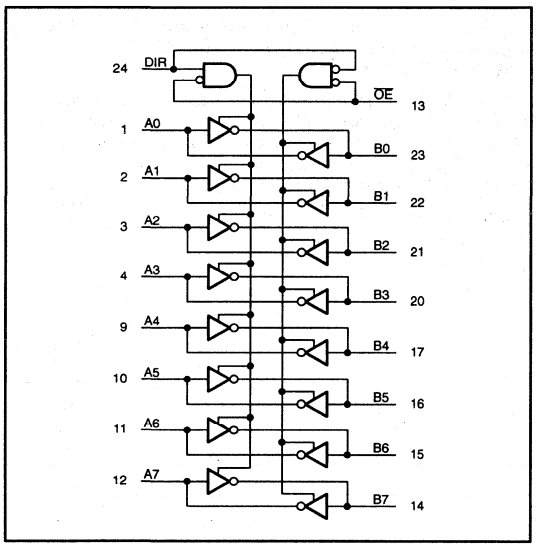
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	A0 to A7	Data inputs/outputs
5, 6, 7, 8	GND	Ground (0V)
13	$\overline{OE}$	Output enable input (active LOW)
14, 15, 16, 17, 20, 21, 22, 23	B7 to B0	Data inputs/outputs
18, 19	V_{CC}	Positive supply voltage
24	DIR	Direction control

Octal bus transceiver with direction pin; 3-State inverting

74HL33640

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		INPUTS/OUTPUT	
$\overline{OE}$	DIR	An	Bn
L	L	A = $\overline{B}$	Inputs
L	H	Inputs	B = $\overline{A}$
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF-state

Octal bus transceiver/register; 3-State 74HL33646

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with the JEDEC 3.3V ± 0.3V supply
- CMOS low power consumption
- Flow-through pin-out architecture
- Low inductance, multiple center power and ground pins for minimum noise and ground bounce
- 3-State outputs
- Direct interface with TTL levels

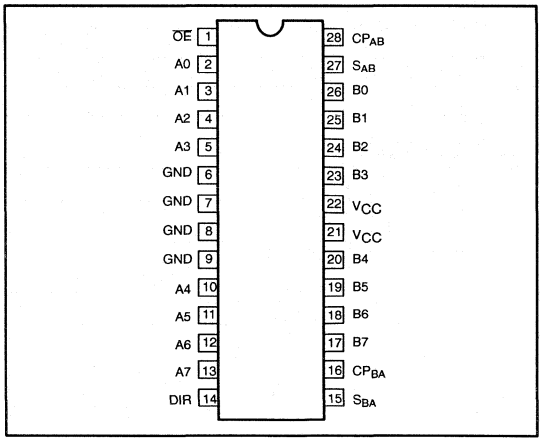
DESCRIPTION

The 74HL33646 consist of 8 non-inverting bus transceiver circuits with 3-State outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the A or B bus will be clocked in the internal registers, as the appropiate clock (CP_{AB} or CP_{BA}) goes to a HIGH logic level. Output enable ($\overline{OE}$) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the A or B register, or in both. The select source inputs (S_{AB} and S_{BA}) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when $\overline{OE}$ is active (LOW). In the isolation mode ($\overline{OE}$ = HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time.

The 74HL33646 is functionally identical to the 74HL33648, but has non-inverting data paths.

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active LOW)
2, 3, 4, 5, 10, 11, 12, 13	A0 to A7	A data inputs/outputs
6, 7, 8, 9	GND	Ground (0V)
14	DIR	Direction control input
15	S_{BA}	Select B to A source input
16	CP_{BA}	B to A clock input (LOW-to-HIGH, edge-triggered)
26, 25, 24, 23, 20, 19, 18, 17	B0 to B7	B data inputs/outputs
21, 22	V_{CC}	Positive supply voltage
27	S_{AB}	Select A to B source input
28	CP_{AB}	A to B clock input (LOW-to-HIGH, edge-triggered)

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An, Bn to Bn, An	C_L = 50pF; V_{CC} = 3.3V	3.2	ns
f_{max}	Maximum clock frequency		350	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	50	pF

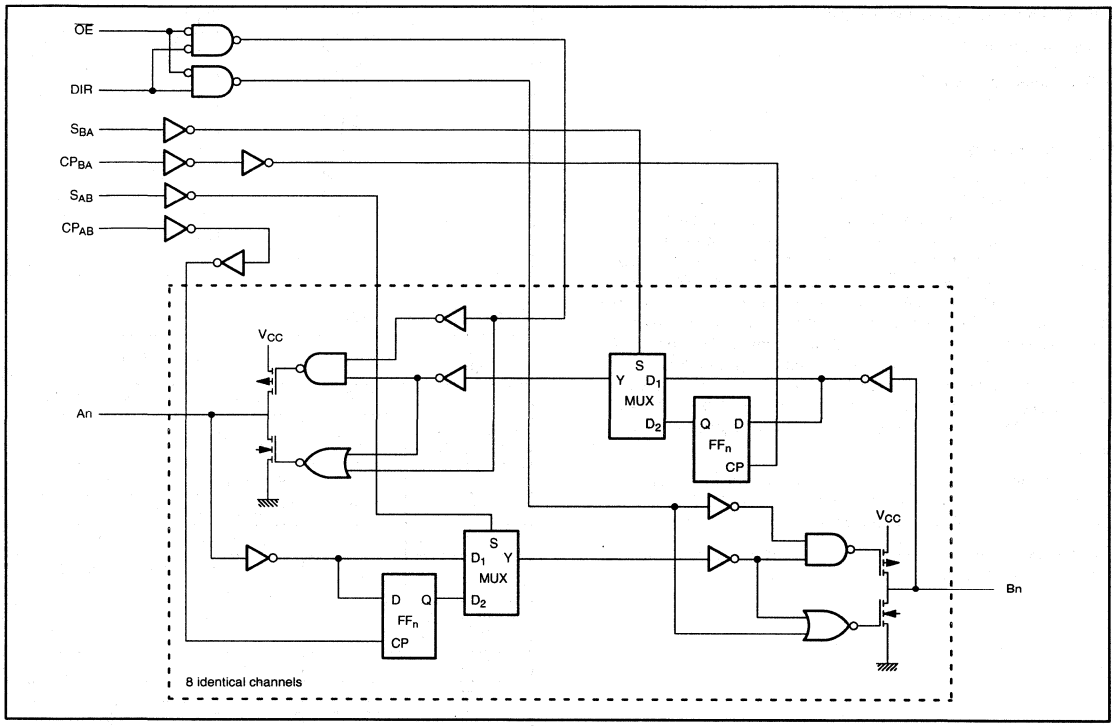
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33646D	28	SO	Plastic	SO28/SOT136A
74HL33646DB	28	SSOP	Plastic	SSOP28/SOT341

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A0 to A7	B0 to B7	
X X	X X	↑ X	X ↑	X X	X X	input un*	un* input	Store A, B unspecified* Store B, A unspecified*
H H	X X	↑ H or L	↑ H or L	X X	X X	input	input	Store A and B data, isolation Hold storage
L L	L L	X X	X H or L	X X	L H	output	input	Real-time B data to A bus Stored B data to A bus
L L	H H	X H or L	X X	L H	X X	input	output	Real-time A data to B bus Stored A data to B bus

* The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = Unspecified
H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH level transition

Octal transceiver/register with dual enable; 3-State — 74HL33652

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with the JEDEC 3.3V ±0.3V supply
- CMOS low power consumption
- Flow-through pin-out architecture
- Low inductance, multiple center power and ground pins for minimum noise and ground bounce
- 3-State outputs
- Direct interface with TTL levels

DESCRIPTION

The 74HL33652 consist of 8 non-inverting bus transceiver circuits with 3-State outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B or both buses, will be stored in the internal registers, at the appropriate clock inputs (CP_{AB} or CP_{BA}) regardless of the select inputs (S_{AB} and S_{BA}) or output enable (OE_{AB} and $\overline{OE}_{BA}$) control inputs. Depending on the select inputs S_{AB} and S_{BA} data can directly go from input to output (real time mode) or data can be controlled by the clock (storage mode), this is when the OE_n inputs this operating mode permits. The output enable inputs OE_{AB} and $\overline{OE}_{BA}$ determine the operation mode of the transceiver. When OE_{AB} is LOW, no data transmission from An to Bn is possible and when $\overline{OE}_{BA}$ is HIGH, there is no data transmission from Bn to An possible. When S_{AB} and S_{BA} are in the real time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OE_{AB} and $\overline{OE}_{BA}$. In this configuration each output reinforces its input.

The 74HL33652 is functionally identical to the 74HL33651, but has non-inverting data paths.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An, Bn to Bn, An	C_L = 50pF; V_{CC} = 3.3V	3.2	ns
f_{max}	Maximum clock frequency		350	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1, 2	50	pF

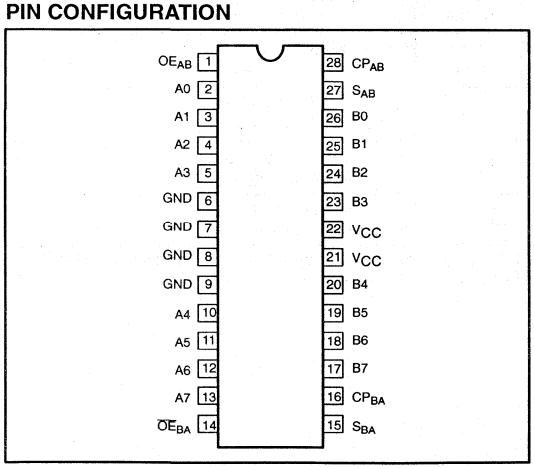
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33652D	28	SO	Plastic	SO28/SOT136A
74HL33652DB	28	SSOP	Plastic	SSOP28/SOT341

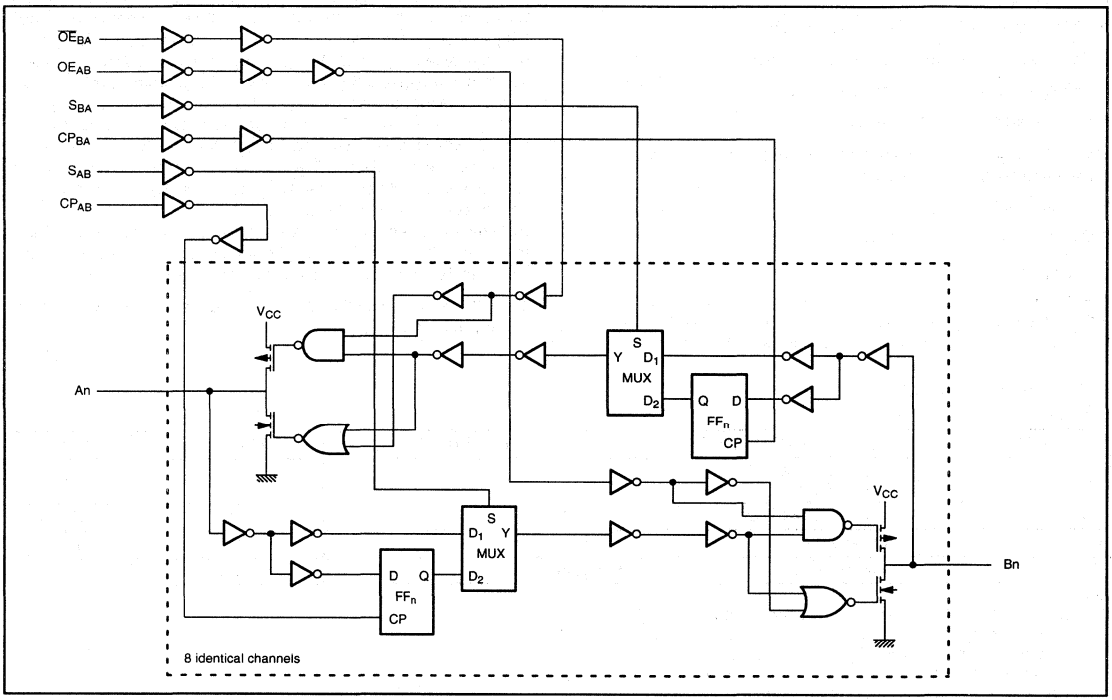
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	OE_{AB}	Output enable A to B input
2, 3, 4, 5, 10, 11, 12, 13	A0 to A7	A data inputs/outputs
6, 7, 8, 9	GND	Ground (0V)
14	$\overline{OE}_{BA}$	Output enable B to A input (active LOW)
15	S_{BA}	Select B to A source input
16	CP_{BA}	B to A clock input (LOW-to-HIGH, edge-triggered)
26, 25, 24, 23, 20, 19, 18, 17	B0 to B7	B data inputs/outputs
21, 22	V_{CC}	Positive supply voltage
27	S_{AB}	Select A to B source input
28	CP_{AB}	A to B clock input (LOW-to-HIGH, edge-triggered)

LOGIC SYMBOL



FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A_0 to A_7	B_0 to B_7	
L L	H H	H or L ↑	H or L ↑	X X	X X	input	input	isolation store A and B data
X H	H H	↑ ↑	H or L ↑	X L	X X	input input	un* output	store A, hold B store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X L	un* output	input input	hold A, store B store B in both registers
L L	L L	X X	X H or L	X X	L H	output	input	real time B data to A bus stored B data to A bus
H H	H H	X H or L	X X	L H	X X	input	output	real-time A data to B bus stored A data to B bus
H	L	H or L	H or L	H	H	output	output	stored A data to B bus and stored B data to A bus

* The data output functions may be enabled or disabled by various signals at the OE_{AB} and $\overline{OE}_{BA}$ inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

Octal registered transceiver (3-State) 74HL33952

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC 3.3V ±0.3V supply
- CMOS low power consumption
- Flow-through pin-out architecture
- Low inductance, multiple center power and ground pins for minimum noise and ground bounce
- 3-State outputs
- Direct interface with TTL levels

DESCRIPTION

The 74HL33952 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74HL33952 is an octal non-inverting registered tranceiver. Two 8-bit back to back registers store data flowing in both directions between two bi-directional buses. Data applied to the inputs is entered and stored on the rising edge of the clock (CP_{nn}) provided that the clock enable ($\overline{CE}_{nn}$) is LOW. The data is then present at the 3-State output buffers, but is only accessible when the output enable input ($\overline{OE}_{nn}$) is LOW. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

The 74HL33952 is identical to the 74HL33953, but has non-inverting outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.0ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP_{nn} to An, Bn	C_L = 50pF V_{CC} = 3.3V	3.2	ns
f_{max}	Maximum clock frequency		350	MHz
C_I	Input capacitance		3.0	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1, 2	35	pF

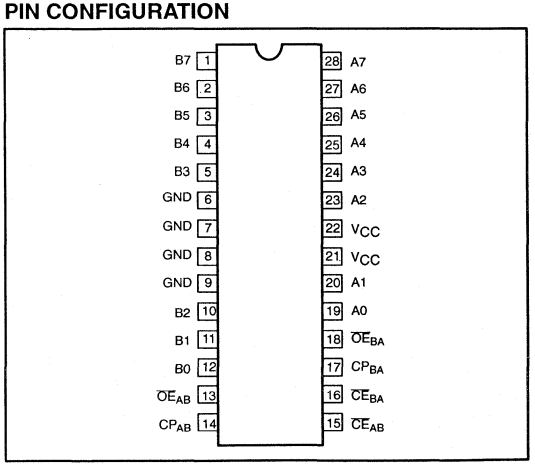
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33952D	28	SO	Plastic	SO28/SOT136A
74HL33952DB	28	SSOP	Plastic	SSOP28/SOT341

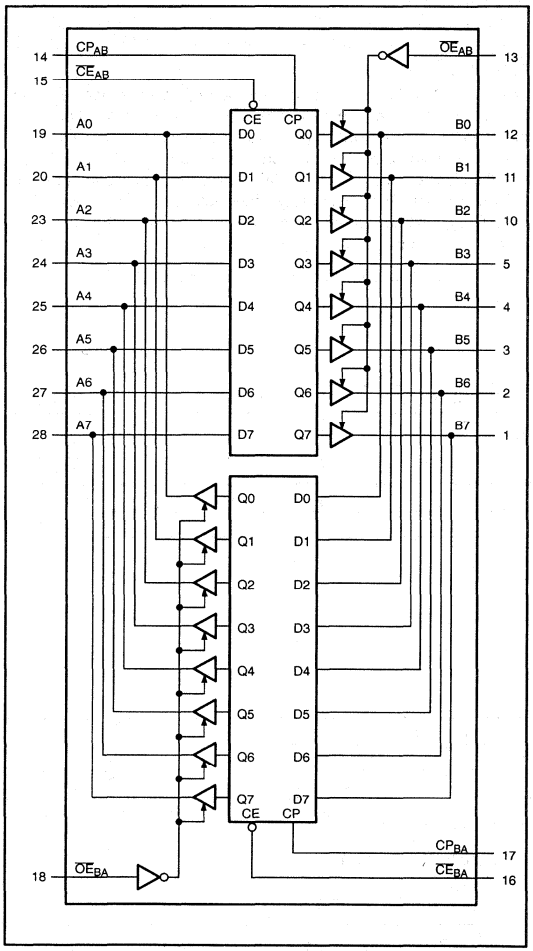
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
12, 11, 10, 5, 4, 3, 2, 1	B0 to B7	'B' data inputs/outputs
6, 7, 8, 9	GND	Ground (0V)
13, 18	$\overline{OE}_{AB}$, $\overline{OE}_{BA}$	Output enable inputs (active LOW)
14, 17	CP_{AB}, CP_{BA}	Clock inputs
15, 16	$\overline{CE}_{AB}$, $\overline{CE}_{BA}$	Clock enable inputs
19, 20, 23, 24, 25, 26, 27, 28	A0 to A7	'A' data inputs/outputs
21, 22	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE for register An or Bn

INPUTS			INTERNAL Q	OPERATING MODE
An or Bn	CP_{nn}	$\overline{CE}_{nn}$		
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	Load data

FUNCTION TABLE for output enable

INPUTS	INTERNAL Q	An or Bn OUTPUTS	OPERATING MODE
$\overline{OE}_{nn}$			
H	X	Z	Disable outputs
L	L	L	Enable outputs
L	H	H	Enable outputs

H = HIGH voltage level
L = LOW voltage level
↑ = LOW-to-HIGH level transition
NC= No change
X = Don't care
Z = High impedance OFF-state

HLL Netlists

HLL SPICE MODELS

```
* HLL Test Circuit
* HLL.CIR
* 3 Volt Advanced CMOS Logic
* Standard Logic Product Group
* Philips Semiconductors
* 3/22/95
*
* SIMULATION MODULES OF CMOS LOGIC PARTS OF PHILIPS HLL FAMILY *
*                  Berkeley SPICE FORMAT                       *
*--------------------------------------------------------------*
* IN ORDER TO SIMULATE A SPECIFIC HLL DEVICE, GO TO THE END OF *
* FILE UNDER HEADING 'START RUNNING CIRCUIT MODEL' AND REMOVE  *
* THE COMMENT STATEMENT '*' BEFORE THE REQUIRED DEVICE.        *
* ALL OTHER DEVICES MUST HAVE AN '*' COMMENT STATEMENT.        *
* IF YOU LIKE TO SIMULATE WITH FAST OR SLOW PARAMETERS, GO TO  *
* HEADING 'PROCESS MODELS' AND REMOVE THE COMMENT STATEMENT '*'*
* BEFORE THE REQUIRED PROCESS MODEL.                           *
* YOU MAY ONLY SIMULATE ONE DEVICE AT THE TIME.                *
* THE LOAD CIRCUIT AND SIMULATION TIMING SHOULD NORMALLY BE    *
* ADAPTED TO YOUR SPECIFIC SITUATION.                          *
*--------------------------------------------------------------*

****************************************************************
*                                                              *
* These HLL models represent only one data input and one output  *
* buffer of the device. Devices with a 3-state output buffer,    *
* have also an Output Enable (OE) input. Other control inputs    *
* such as DIR or CLK inputs are not modeled. Circuitry between   *
* the input and output buffers are also omitted, such as gates,  *
* registers, latches, mux's and intermediate buffers. One result *
* of this is that HLL models does not show the exact function of *
* the device. Another result of this is that propagation delays  *
* in SPICE will not necessarily match with the published AC      *
* timing specifications in the device data sheet.                *
*                                                              *
****************************************************************

.OPTIONS  ACCT   LIST  OPTS  NUMDGT=3 ITL5=25000  NOMOD

* Nominal parameters
.INC c:\spice\hll\hllnomi.cir

* Fast parameters
*.INC c:\spice\hll\hllfast.cir

* Slow parameters
*.INC c:\spice\hll\hllslow.cir
```

```
***** START RUNNING CIRCUIT MODEL ******

*XHL240   5   2   4   1   0 INVERTER
*XHL533   5   2   4   1   0 INVERTER
*XHL534   5   2   4   1   0 INVERTER
*XHL620   5   2   4   1   0 INVERTER
*XHL640   5   2   4   1   0 INVERTER
*XHL241   5   2   4   1   0 INVERTRN
 XHL244   5   2   4   1   0 INVERTRN
*XHL245   5   2   4   1   0 INVERTRN
*XHL373   5   2   4   1   0 INVERTRN
*XHL374   5   2   4   1   0 INVERTRN
*XHL623   5   2   4   1   0 INVERTRN
*XHL646   5   2   4   1   0 INVERTRN
*XHL652   5   2   4   1   0 INVERTRN
*XHL952   5   2   4   1   0 INVERTRN

********** EXTERNAL TEST LOAD **********
R1     4   0    500
C5     4   0    50PF
****************************************

VDD    1   0    DC   3.0
VIN    2   0    PULSE   0   3.0   5N   2.5N   2.5N   40N   70N
VEN    5   0    DC   3.0
.TRAN   1N   70N
.FILE TRAN V(2) V(4)
.PROBE V(2) V(4)
.END
```

HLLNOMI.CIR Subcircuit

```
* HLL SPICE Subcircuit and Primitive Element Library
* HLLNOMI.CIR
* Nominal Process Parameters
* 3 Volt Advanced CMOS Logic
* Standard Logic Product Group
* Philips Semiconductors
* 3/22/95
*            Berkeley SPICE Format
************************************************
*          NOMINAL N-CHANNEL TRANSISTOR
*             UCB-3 PARAMETER SET
*                   24-JUNE-1993
************************************************
.MODEL MNEN NMOS
+LEVEL = 3
+KP    = 114E-6
+VTO   = 0.57
+TOX   = 15E-9
+NSUB  = 7.8E16
+GAMMA = 0.70
+PHI   = 0.65
+VMAX  = 187E3
+RS    = 20
+RD    = 20
+XJ    = 0.26E-6
+LD    = 0.11E-6
+DELTA = 1.89
+THETA = 0.072
+ETA   = 0.043
+KAPPA = 0.0
+WD    = 0.0
* USE PARAMETER WD ONLY IN SPICE MODEL 3
* OTHERWISE MAKE FROM THAT LINE A COMMENT
************************************************
*         NOMINAL P-CHANNEL TRANSISTOR
*            UCB-3 PARAMETER SET
*                  24-JUNE-1993
************************************************
.MODEL MPEN PMOS
+LEVEL = 3
+KP    = 43.7E-6
+VTO   = -0.67
+TOX   = 15.0E-9
+NSUB  = 6.0E16
+GAMMA = 0.84
+PHI   = 0.65
+VMAX  = 1.0E6
+RS    = 17.5
+RD    = 17.5
+XJ    = 0.30E-6
+LD    = 0.04E-6
+DELTA = 2.88
+THETA = 0.189
+ETA   = 0.091
+KAPPA = 0.0
+WD    = -0.03E-6
* USE PARAMETER WD ONLY IN SPICE MODEL 3
* OTHERWISE MAKE FROM THAT LINE A COMMENT
```

```
*************************************************
*      START OF SUBCIRCUIT DESCRIPTION
*                    25-JUN-1993
*************************************************

.SUBCKT HLLINPAN    2    3    50    60
* NOMINAL CASE PARAMETERS
* STANDARD HLL INPUT P-CH 175/0.8 N-CH 80/0.8 INCL. ESD STRUCTURE
*   IN = 2,   OUT = 3,   VCC = 50,   GND = 60
*   01-MAY-1992
MN1 2 60 60 60 MNEN W=400U L=1.0U AD=7390P AS=208P PD=688U PS=420U
R1   4   2   100
MN2 4 60 60 60 MNEN W= 43U L=1.0U AD=176P AS=208P PD= 58U PS= 58U
MP1 3   4 50 50 MPEN W=175U L=0.8U AD=250P AS=500P PD=200U PS=200U
MN3 3   4 60 60 MNEN W= 80U L=0.8U AD=100P AS=190P PD= 90U PS= 90U
MP2 5   3 50 50 MPEN W= 10U L=0.8U AD= 22P AS= 22P PD= 25U PS= 25U
MN4 5   3 60 60 MNEN W=  4U L=0.8U AD=  9P AS=  9P PD= 12U PS= 12U
MN5 3   5 60 60 MNEN W= 25U L=1.6U AD= 40P AS= 40P PD= 40U PS= 40U
.ENDS

.SUBCKT HLLINVAN    2    3    50    60
* NOMINAL CASE PARAMETERS
* INTERNAL INVERTER P-CH 175/0.8  N-CH 80/0.8
* IN = 2,   OUT = 3,   VCC = 50,   GND = 60
* 01-MAY-1992
MP1 3   2 50 50 MPEN W=175U L=0.8U AD=250P AS=500P PD=200U PS=200U
MN1 3   2 60 60 MNEN W= 80U L=0.8U AD=100P AS=190P PD= 90U PS= 90U
.ENDS

.SUBCKT HLLOUTAN    2    3    4    50    60
* NOMINAL CASE PARAMETERS
* 3-STATE OUTPUT MODULE
*   ENABLE = 2, IN = 3,   OUT = 4,   VCC = 50,   GND = 60
*   01-MAY-1992
MP1 5   2 50 50 MPEN W=250U L=0.8U AD= 300P AS= 600P PD=300U PS=300U
MP2 5   3 50 50 MPEN W=300U L=0.8U AD= 360P AS= 700P PD=350U PS=350U
MN1 5   2   6 60 MNEN W=170U L=0.8U AD= 200P AS= 200P PD=180U PS=180U
MN2 6   3 60 60 MNEN W=250U L=0.8U AD= 300P AS= 300P PD=260U PS=260U
MP3 15 2 50 50 MPEN W= 80U L=0.8U AD= 100P AS= 100P PD=120U PS=120U
MN3 15 2 60 60 MNEN W= 30U L=0.8U AD=  45P AS=  45P PD= 50U PS= 50U
MP4 7 15   8 50 MPEN W=300U L=0.8U AD= 360P AS= 360P PD=370U PS=370U
MP5 8   3 50 50 MPEN W=400U L=0.8U AD= 480P AS= 480P PD=410U PS=410U
MN4 7 15 60 60 MNEN W=150U L=0.8U AD= 180P AS= 320P PD=180U PS=180U
MN5 7   3 60 60 MNEN W=100U L=0.8U AD= 120P AS= 250P PD=120U PS=120U
MP6 4   5 50 50 MPEN W=300U L=0.8U AD= 300P AS= 300P PD=300U PS=300U
MN6 4   7 60 60 MNEN W=100U L=0.8U AD=1320P AS= 500P PD=250U PS=200U
R1   5   9 50
MP7 4   9 50 50 MPEN W=500U L=0.8U AD= 500P AS= 500P PD=500U PS=500U
R2   9 10 20
MP8 4 10 50 50 MPEN W=600U L=0.8U AD= 600P AS= 600P PD=600U PS=600U
R3 10 11 10
MP9 4 11 50 50 MPEN W=600U L=0.8U AD= 600P AS= 600P PD=600U PS=600U
R4   7 12 100
MN7 4 12 60 60 MNEN W=200U L=0.8U AD=2640P AS=1000P PD=500U PS=400U
R5 12 13 40
MN8 4 13 60 60 MNEN W=250U L=0.8U AD=3300P AS=1250P PD=625U PS=500U
R6 13 14 20
MN9 4 14 60 60 MNEN W=250U L=0.8U AD=3300P AS=1250P PD=625U PS=500U
.ENDS
```

```
*************************************************************
*      START OF HLL CIRCUITS DESCRIPTION MODELS
*                          25-JUN-1993
*************************************************************

.SUBCKT INVERTER  5   2   4   1  90
* INVERTING BUFFER TYPE
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
* USE THIS MODEL FOR 74HL33240 - 533 - 534 - 620 - 640
*  EN = 5, IN = 2,  OUT = 4,  VCC = 1,  GND = 90
*  24-JUNE-1993
XINP 20  30  50  60       HLLINPAN
XOUT  5  30  40  50  60   HLLOUTAN
L4    4  40   7.77NH
C4   40  90   1.5P
L3    2  20   6.88NH
C1   20  90   1.5P
L1    1  50   2.2NH
L2   90  60   1.5NH
C2   50  90   1.5P
C3   60  90   1.5P
.ENDS

.SUBCKT INVERTRN  5   2   4   1  90
* NON-INVERTING BUFFER TYPE
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
* USE THIS MODEL FOR 74HL33241 - 244 - 245 - 373 - 374
* 623 - 646 - 652 - 952
*  EN = 5, IN = 2,  OUT = 4,  VCC = 1,  GND = 90
*  24-JUNE-1993
XINP 20  30  50  60       HLLINPAN
XINV 30  35  50  60       HLLINVAN
XOUT  5  35  40  50  60   HLLOUTAN
L4    4  40   7.77NH
C4   40  90   1.5P
L3    2  20   6.88NH
C1   20  90   1.5P
L1    1  50   2.2NH
L2   90  60   1.5NH
C2   50  90   1.5P
C3   60  90   1.5P
.ENDS
```

HLLFAST.CIR Subcircuit

```
* HLL SPICE Subcircuit and Primitive Element Library
* HLLFAST.CIR
* Fast Process Parameters
* 3 Volt Advanced CMOS Logic
* Standard Logic Product Group
* Philips Semiconductors
* 3/22/95
*               Berkeley SPICE Format
*************************************************
*          FAST N-CHANNEL TRANSISTOR
*            UCB-3 PARAMETER SET
*                  24-JUNE-1993
*************************************************
.MODEL MNEF NMOS
+LEVEL = 3
+KP    = 134E-6
+VTO   = 0.46
+TOX   = 13.5E-9
+NSUB  = 8.9E16
+GAMMA = 0.54
+PHI   = 0.65
+VMAX  = 160E3
+RS    = 10
+RD    = 10
+XJ    = 0.31E-6
+LD    = 0.18E-6
+DELTA = 1.46
+THETA = 0.070
+ETA   = 0.025
+KAPPA = 0.0
+WD    = -0.05E-6
* USE PARAMETER WD ONLY IN SPICE MODEL 3
* OTHERWISE MAKE FROM THAT LINE A COMMENT
*************************************************
*         FAST P-CHANNEL TRANSISTOR
*            UCB-3 PARAMETER SET
*                  24-JUNE-1993
*************************************************
.MODEL MPEF PMOS
+LEVEL = 3
+KP    = 47.3E-6
+VTO   = -0.55
+TOX   = 13.5E-9
+NSUB  = 7.9E16
+GAMMA = 0.65
+PHI   = 0.65
+VMAX  = 1.0E6
+RS    = 10
+RD    = 10
+XJ    = 0.28E-6
+LD    = 0.11E-6
+DELTA = 4.80
+THETA = 0.189
+ETA   = 0.055
+KAPPA = 0.0
+WD    = -0.12E-6
* USE PARAMETER WD ONLY IN SPICE MODEL 3
* OTHERWISE MAKE FROM THAT LINE A COMMENT
```

```
*********************************************
*     START OF SUBCIRCUIT DESCRIPTION
*                    25-JUN-1993
*********************************************

.SUBCKT HLLINPAF   2   3   50   60
* FAST PARAMETERS
* STANDARD HLL INPUT P-CH 175/0.8 N-CH 80/0.8 INCL. ESD STRUCTURE
*  IN = 2,  OUT = 3,  VCC = 50,  GND = 60
*  01-MAY-1992
MN1 2 60 60 60 MNEF W=400U L=1.0U AD=7390P AS=208P PD=688U PS=420U
R1  4  2  100
MN2 4 60 60 60 MNEF W= 43U L=1.0U AD=176P AS=208P PD= 58U PS= 58U
MP1 3  4 50 50 MPEF W=175U L=0.8U AD=250P AS=500P PD=200U PS=200U
MN3 3  4 60 60 MNEF W= 80U L=0.8U AD=100P AS=190P PD= 90U PS= 90U
MP2 5  3 50 50 MPEF W= 10U L=0.8U AD= 22P AS= 22P PD= 25U PS= 25U
MN4 5  3 60 60 MNEF W=  4U L=0.8U AD=  9P AS=  9P PD= 12U PS= 12U
MN5 3  5 60 60 MNEF W= 25U L=1.6U AD= 40P AS= 40P PD= 40U PS= 40U
.ENDS

.SUBCKT HLLINVAF   2   3   50   60
* FAST PARAMETERS
* INTERNAL INVERTER P-CH 175/0.8  N-CH 80/0.8
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* 01-MAY-1992
MP1 3  2 50 50 MPEF W=175U L=0.8U AD=250P AS=500P PD=200U PS=200U
MN1 3  2 60 60 MNEF W= 80U L=0.8U AD=100P AS=190P PD= 90U PS= 90U
.ENDS

.SUBCKT HLLOUTAF    2   3   4   50   60
* FAST PARAMETERS
* 3-STATE OUTPUT MODULE
*  ENABLE = 2, IN = 3,  OUT = 4,  VCC = 50,  GND = 60
*  01-MAY-1992
MP1 5  2 50 50 MPEF W=250U L=0.8U AD= 300P AS= 600P PD=300U PS=300U
MP2 5  3 50 50 MPEF W=300U L=0.8U AD= 360P AS= 700P PD=350U PS=350U
MN1 5  2  6 60 MNEF W=170U L=0.8U AD= 200P AS= 200P PD=180U PS=180U
MN2 6  3 60 60 MNEF W=250U L=0.8U AD= 300P AS= 300P PD=260U PS=260U
MP3 15 2 50 50 MPEF W= 80U L=0.8U AD= 100P AS= 100P PD=120U PS=120U
MN3 15 2 60 60 MNEF W= 30U L=0.8U AD=  45P AS=  45P PD= 50U PS= 50U
MP4 7 15  8 50 MPEF W=300U L=0.8U AD= 360P AS= 360P PD=370U PS=370U
MP5 8  3 50 50 MPEF W=400U L=0.8U AD= 480P AS= 480P PD=410U PS=410U
MN4 7 15 60 60 MNEF W=150U L=0.8U AD= 180P AS= 320P PD=180U PS=180U
MN5 7  3 60 60 MNEF W=100U L=0.8U AD= 120P AS= 250P PD=120U PS=120U
MP6 4  5 50 50 MPEF W=300U L=0.8U AD= 300P AS= 300P PD=300U PS=300U
MN6 4  7 60 60 MNEF W=100U L=0.8U AD=1320P AS= 500P PD=250U PS=200U
R1  5  9 50
MP7 4  9 50 50 MPEF W=500U L=0.8U AD= 500P AS= 500P PD=500U PS=500U
R2  9 10 20
MP8 4 10 50 50 MPEF W=600U L=0.8U AD= 600P AS= 600P PD=600U PS=600U
R3 10 11 10
MP9 4 11 50 50 MPEF W=600U L=0.8U AD= 600P AS= 600P PD=600U PS=600U
R4  7 12 100
MN7 4 12 60 60 MNEF W=200U L=0.8U AD=2640P AS=1000P PD=500U PS=400U
R5 12 13 40
MN8 4 13 60 60 MNEF W=250U L=0.8U AD=3300P AS=1250P PD=625U PS=500U
R6 13 14 20
MN9 4 14 60 60 MNEF W=250U L=0.8U AD=3300P AS=1250P PD=625U PS=500U
.ENDS
```

```
*************************************************************
*      START OF HLL CIRCUITS DESCRIPTION MODELS
*                              25-JUN-1993
*************************************************************

.SUBCKT INVERTER  5   2   4   1  90
* INVERTING BUFFER TYPE
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
* USE THIS MODEL FOR 74HL33240 - 533 - 534 - 620 - 640
*  EN = 5, IN = 2,  OUT = 4,  VCC = 1,  GND = 90
*  24-JUNE-1993
XINP 20  30  50  60       HLLINPAF
XOUT  5  30  40  50  60   HLLOUTAF
L4    4  40   7.77NH
C4   40  90   1.5P
L3    2  20   6.88NH
C1   20  90   1.5P
L1    1  50   2.2NH
L2   90  60   1.5NH
C2   50  90   1.5P
C3   60  90   1.5P
.ENDS

.SUBCKT INVERTRN  5   2   4   1  90
* NON-INVERTING BUFFER TYPE
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
* USE THIS MODEL FOR 74HL33241 - 244 - 245 - 373 - 374
* 623 - 646 - 652 - 952
*  EN = 5, IN = 2,  OUT = 4,  VCC = 1,  GND = 90
*  24-JUNE-1993
XINP 20  30  50  60       HLLINPAF
XINV 30  35  50  60       HLLINVAF
XOUT  5  35  40  50  60   HLLOUTAF
L4    4  40   7.77NH
C4   40  90   1.5P
L3    2  20   6.88NH
C1   20  90   1.5P
L1    1  50   2.2NH
L2   90  60   1.5NH
C2   50  90   1.5P
C3   60  90   1.5P
.ENDS
```

HLLSLOW.CIR Subcircuit

```
* HLL SPICE Subcircuit and Primitive Element Library
* HLLSLOW.CIR
* Slow Process Parameters
* 3 Volt Advanced CMOS Logic
* Standard Logic Product Group
* Philips Semiconductors
* 3/22/95
*              Berkeley SPICE Format
************************************************
*          SLOW N-CHANNEL TRANSISTOR
*            UCB-3 PARAMETER SET
*                   24-JUNE-1993
************************************************
.MODEL MNES NMOS
+LEVEL = 3
+KP    = 96E-6
+VTO   = 0.66
+TOX   = 16.5E-9
+NSUB  = 3.4E15
+GAMMA = 0.72
+PHI   = 0.65
+VMAX  = 199E3
+RS    = 30
+RD    = 30
+XJ    = 0.06E-6
+LD    = 0.04E-6
+DELTA = 1.79
+THETA = 0.075
+ETA   = 0.047
+KAPPA = 0.0
+WD    = 0.06E-6
* USE PARAMETER WD ONLY IN SPICE MODEL 3
* OTHERWISE MAKE FROM THAT LINE A COMMENT
************************************************
*         SLOW P-CHANNEL TRANSISTOR
*            UCB-3 PARAMETER SET
*                   24-JUNE-1993
************************************************
.MODEL MPES PMOS
+LEVEL = 3
+KP    = 38.4E-6
+VTO   = -0.75
+TOX   = 16.5E-9
+NSUB  = 2.0E17
+GAMMA = 0.81
+PHI   = 0.65
+VMAX  = 1.0E6
+RS    = 25
+RD    = 25
+XJ    = 0.15E-6
+LD    = 0.0
+DELTA = 3.15
+THETA = 0.190
+ETA   = 0.102
+KAPPA = 0.0
+WD    = 0.03E-6
* USE PARAMETER WD ONLY IN SPICE MODEL 3
* OTHERWISE MAKE FROM THAT LINE A COMMENT
```

```
*********************************************
*      START OF SUBCIRCUIT DESCRIPTION
*                    25-JUN-1993
*********************************************

.SUBCKT HLLINPAS   2   3   50   60
* SLOW PARAMETERS
* STANDARD HLL INPUT P-CH 175/0.8 N-CH 80/0.8 INCL. ESD STRUCTURE
*  IN = 2,  OUT = 3,  VCC = 50,  GND = 60
*  01-MAY-1992
MN1 2 60 60 60 MNES W=400U L=1.0U AD=7390P AS=208P PD=688U PS=420U
R1  4  2  100
MN2 4 60 60 60 MNES W= 43U L=1.0U AD=176P AS=208P PD= 58U PS= 58U
MP1 3  4 50 50 MPES W=175U L=0.8U AD=250P AS=500P PD=200U PS=200U
MN3 3  4 60 60 MNES W= 80U L=0.8U AD=100P AS=190P PD= 90U PS= 90U
MP2 5  3 50 50 MPES W= 10U L=0.8U AD= 22P AS= 22P PD= 25U PS= 25U
MN4 5  3 60 60 MNES W=  4U L=0.8U AD=  9P AS=  9P PD= 12U PS= 12U
MN5 3  5 60 60 MNES W= 25U L=1.6U AD= 40P AS= 40P PD= 40U PS= 40U
.ENDS

.SUBCKT HLLINVAS   2   3   50   60
* SLOW PARAMETERS
* INTERNAL INVERTER P-CH 175/0.8  N-CH 80/0.8
* IN = 2, OUT = 3,  VCC = 50,  GND = 60
* 01-MAY-1992
MP1 3  2 50 50 MPES W=175U L=0.8U AD=250P AS=500P PD=200U PS=200U
MN1 3  2 60 60 MNES W= 80U L=0.8U AD=100P AS=190P PD= 90U PS= 90U
.ENDS

.SUBCKT HLLOUTAS    2   3   4   50   60
* SLOW PARAMETERS
* 3-STATE OUTPUT MODULE
*  EN = 2, IN = 3,  OUT = 4,  VCC = 50,  GND = 60
*  01-MAY-1992
MP1 5  2 50 50 MPES W=250U L=0.8U AD= 300P AS= 600P PD=300U PS=300U
MP2 5  3 50 50 MPES W=300U L=0.8U AD= 360P AS= 700P PD=350U PS=350U
MN1 5  2  6 60 MNES W=170U L=0.8U AD= 200P AS= 200P PD=180U PS=180U
MN2 6  3 60 60 MNES W=250U L=0.8U AD= 300P AS= 300P PD=260U PS=260U
MP3 15 2 50 50 MPES W= 80U L=0.8U AD= 100P AS= 100P PD=120U PS=120U
MN3 15 2 60 60 MNES W= 30U L=0.8U AD=  45P AS=  45P PD= 50U PS= 50U
MP4 7 15  8 50 MPES W=300U L=0.8U AD= 360P AS= 360P PD=370U PS=370U
MP5 8  3 50 50 MPES W=400U L=0.8U AD= 480P AS= 480P PD=410U PS=410U
MN4 7 15 60 60 MNES W=150U L=0.8U AD= 180P AS= 320P PD=180U PS=180U
MN5 7  3 60 60 MNES W=100U L=0.8U AD= 120P AS= 250P PD=120U PS=120U
MP6 4  5 50 50 MPES W=300U L=0.8U AD= 300P AS= 300P PD=300U PS=300U
MN6 4  7 60 60 MNES W=100U L=0.8U AD=1320P AS= 500P PD=250U PS=200U
R1  5  9 50
MP7 4  9 50 50 MPES W=500U L=0.8U AD= 500P AS= 500P PD=500U PS=500U
R2  9 10 20
MP8 4 10 50 50 MPES W=600U L=0.8U AD= 600P AS= 600P PD=600U PS=600U
R3 10 11 10
MP9 4 11 50 50 MPES W=600U L=0.8U AD= 600P AS= 600P PD=600U PS=600U
R4  7 12 100
MN7 4 12 60 60 MNES W=200U L=0.8U AD=2640P AS=1000P PD=500U PS=400U
R5 12 13 40
MN8 4 13 60 60 MNES W=250U L=0.8U AD=3300P AS=1250P PD=625U PS=500U
R6 13 14 20
MN9 4 14 60 60 MNES W=250U L=0.8U AD=3300P AS=1250P PD=625U PS=500U
.ENDS
```

```
*************************************************************
*      START OF HLL CIRCUITS DESCRIPTION MODELS
*                              25-JUN-1993
*************************************************************

.SUBCKT INVERTER  5   2   4   1  90
* INVERTING BUFFER TYPE
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
* USE THIS MODEL FOR 74HL33240 - 533 - 534 - 620 - 640
*  EN = 5, IN = 2,  OUT = 4,  VCC = 1,  GND = 90
*  24-JUNE-1993
XINP 20  30  50  60       HLLINPAS
XOUT  5  30  40  50  60   HLLOUTAS
L4    4  40   7.77NH
C4   40  90   1.5P
L3    2  20   6.88NH
C1   20  90   1.5P
L1    1  50   2.2NH
L2   90  60   1.5NH
C2   50  90   1.5P
C3   60  90   1.5P
.ENDS

.SUBCKT INVERTRN  5   2   4   1  90
* NON-INVERTING BUFFER TYPE
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
* USE THIS MODEL FOR 74HL33241 - 244 - 245 - 373 - 374
* 623 - 646 - 652 - 952
*  EN = 5, IN = 2,  OUT = 4,  VCC = 1,  GND = 90
*  24-JUNE-1993
XINP 20  30  50  60       HLLINPAS
XINV 30  35  50  60       HLLINVAS
XOUT  5  35  40  50  60   HLLOUTAS
L4    4  40   7.77NH
C4   40  90   1.5P
L3    2  20   6.88NH
C1   20  90   1.5P
L1    1  50   2.2NH
L2   90  60   1.5NH
C2   50  90   1.5P
C3   60  90   1.5P
.ENDS
```

Section 8
ALVC

SPICE

CONTENTS

Each ALVC device requires some combination of one or two input stages, an output stage, possibly one or two inverting stages, and some package parasitics. Table 8-1 shows ALVC model combinations that correlate input, inverting, and output structures for each part type. Dashes indicate that a particular stage is not needed.

Table 8-1. ALVC Model Combinations

ALVC16	Input Circuit	Inverter Circuit	Output Circuit	Inverting Output	Subcircuit Name
240	LVCINPA	LVCINVA/INV1	LVCOUTA	Yes	INVERT3
241	LVCINPA	LVCINVA	LVCOUTA	No	INVERT3N
244	LVCINPA	LVCINVA	LVCOUTA	No	INVERT3N
245	LVCINPA	LVCINVA	LVCOUTA	No	INVERT3N
373	LVCINPA	LVCINVA	LVCOUTA	No	INVERT3N
374	LVCINPA	LVCINVA	LVCOUTA	No	INVERT3N
540	LVCINPA	LVCINVA/INV1	LVCOUTA	Yes	INVERT3
541	LVCINPA	LVCINVA	LVCOUTA	No	INVERT3N
623	LVCINPA	LVCINVA	LVCOUTA	No	INVERT3N
4245	LVCINPA	LVCINVA	LVCOUTA	No	INVERT3N

The data sheet section provides information on each ALVC part type. Each data sheet contains a part description, part features, quick reference data, ordering information, pin configuration, logic symbol or diagram, and function table.

To do simulations on a particular part type, refer to the ALVC Netlists section of the book. That section contains a file called "ALVC.CIR" that contains simulation test circuits for individual device types. The file is also in the ALVC directory in the attached diskette, and it is written in the Berkeley SPICE format only. Figure 8-1 shows examples of how the test circuits are assembled.

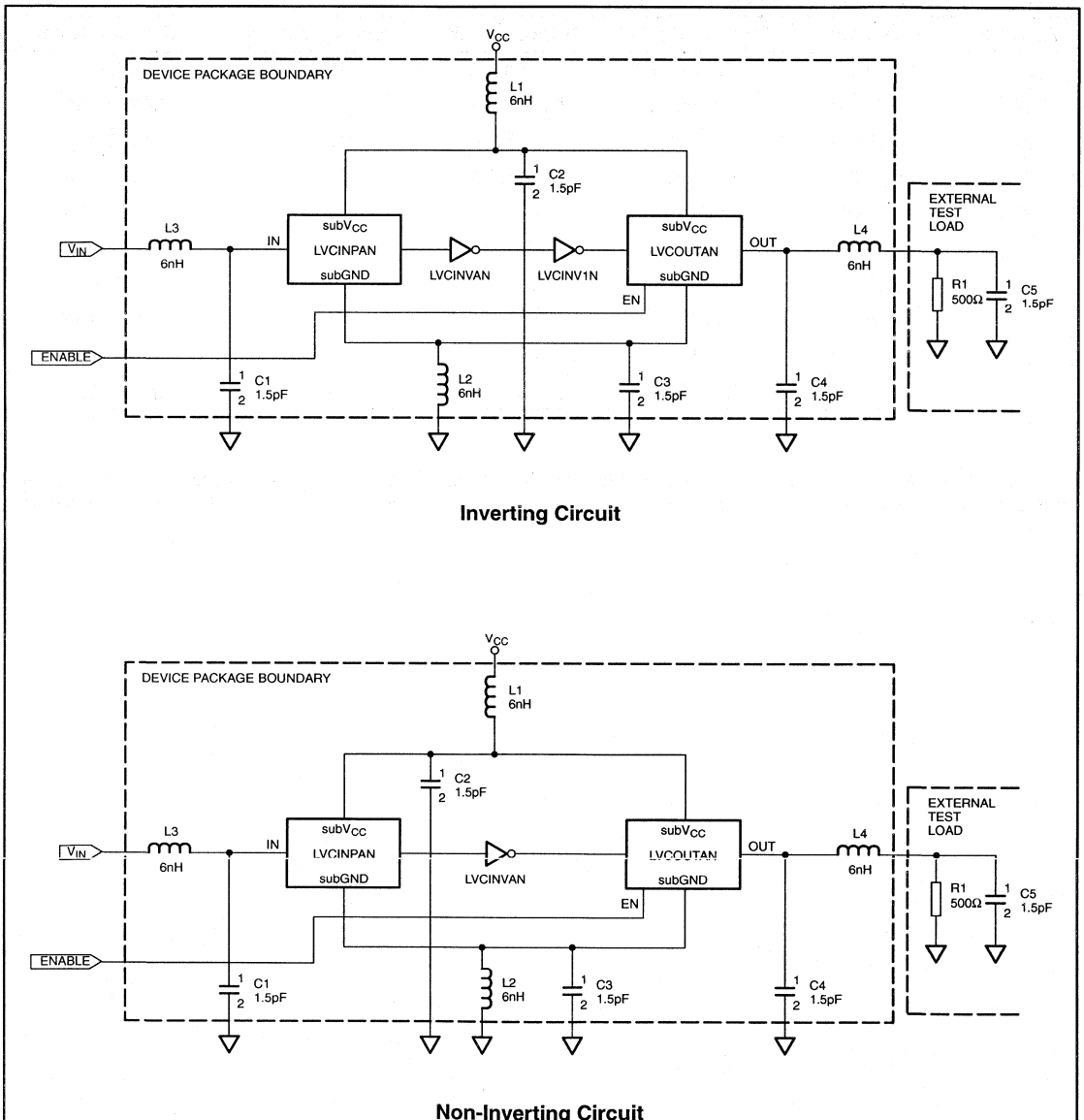


Figure 8-1. Examples of ALVC Test Circuits

Also in the ALVC Netlists section of the book and in the ALVC directory of the diskette are files for subcircuits and primitive elements, such as transistors, diodes, and resistors. These files are called LVCXXXX.CIR, the "XXXX" standing for NOMI, FAST, and SLOW, representing the nominal, fast, and slow process corners. The files contain the subcircuits for input, output, and inverter circuits, and they also have package parasitics connected to simulate a device in a package. Package parasitic values can be changed to suit the application. See the Packaging section of the book for values.

For clarification, the following illustration shows how the three programs interact with each other:

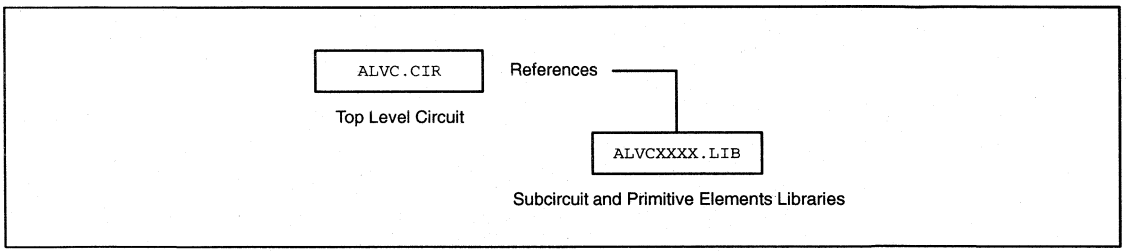


Figure 8-2. ALVC SPICE Program Hierarchy

The top level program, ALVC.CIR, uses an AC test set-up with a 3V square wave input, 5ns delay, 2.5ns rise and fall times, 40ns pulse width, 70ns period, 3V V_{CC}, 3V applied to the output enable, and a 500Ω, 50pF load. These conditions may be modified to suit the application. Also, the ".INC" command that specifies the path to reference the other program should be modified to reflect your disk directory structure.

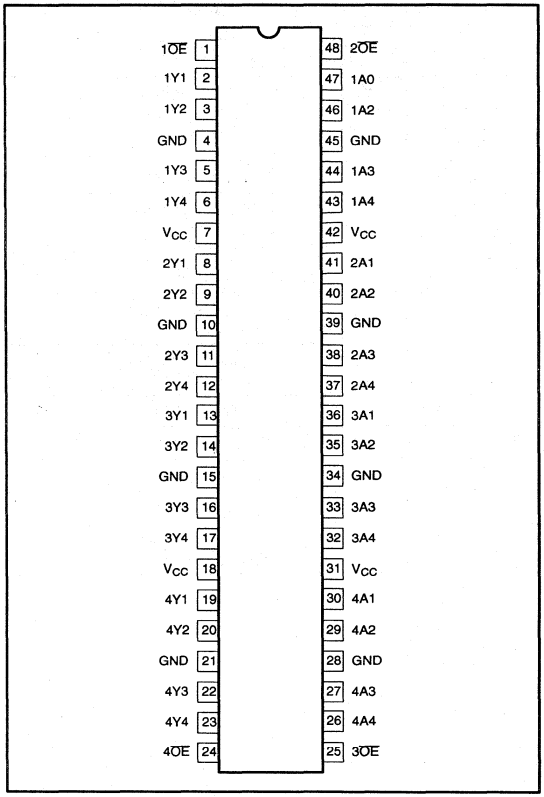
ALVC Short-form Datasheets

16-bit buffer/line driver; 3-State; inverting 74ALVC16240

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Compliese with JEDEC standard no. 8-1A
- CMOS low power consumption
- Multibyte™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Bushold on data inputs
- Output drive capability 50Ω transmission lines @ 85°C

PIN CONFIGURATION



DESCRIPTION

The 74ALVC16240 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74ALVC16240 is a 16-bit inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on nOE causes the outputs to assume a high impedance OFF-state.

The 74ALVC16240 is identical to the 74ALVC16244 but has inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay 1An to 1Yn; 2An to 2Yn	C_L = 50pF V_{CC} = 3.3V	2.1	ns
C_I	Input capacitance		3.0	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1, 2	30	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

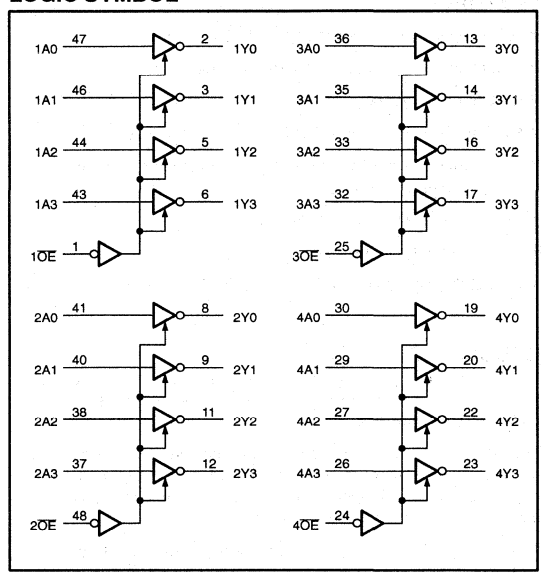
ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16240DL	48	SSOP48	Plastic	SSOP48/SOT370
74ALVC16240DGG	48	TSSOP48	Plastic	TSSOP48/SOT362

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	'1' output enable input (active LOW)
2, 3, 5, 6	1Y0 to 1Y3	1Y data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
8, 9, 11, 12	2Y0 to 2Y3	2Y data outputs
13, 14, 16, 17	3Y0 to 3Y3	3Y data outputs
19, 20, 22, 23	4Y0 to 4Y3	4Y data outputs
24	$4\overline{OE}$	'4' output enable input (active LOW)
25	$3\overline{OE}$	'3' output enable input (active LOW)
30, 29, 27, 26	4A0 to 4A3	4A data inputs
36, 35, 33, 32	3A0 to 3A3	3A data inputs
41, 40, 38, 37	2A0 to 2A3	2A data inputs
47, 46, 44, 43	1A0 to 1A3	1A data inputs
48	$2\overline{OE}$	'2' output enable input (active LOW)

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nAn	nYn
L	L	H
L	H	L
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

16-bit buffer/line driver; 3-State | 74ALVC16241

FEATURES

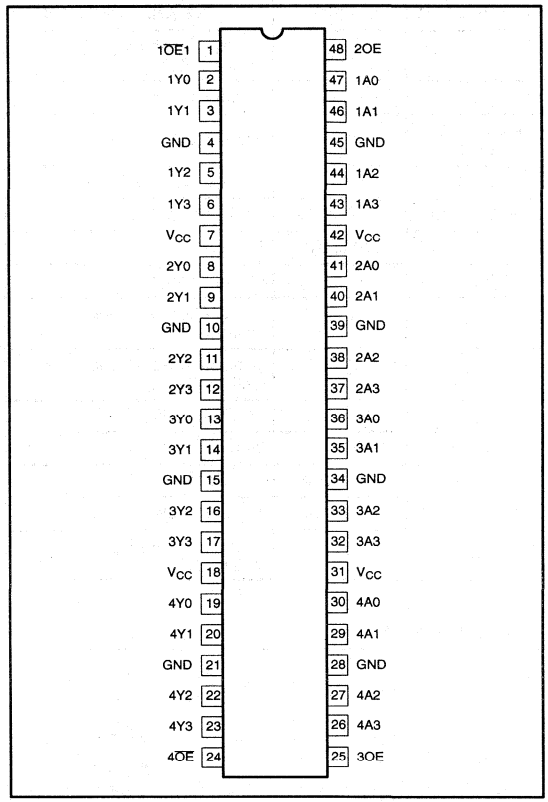
- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Multibyte™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bushold
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74ALVC16241 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74ALVC16241 is a 16-bit buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs nOE and nOE. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer.

PIN CONFIGURATION



QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nAn to nYn	C_L = 50pF V_{CC} = 3.3V	2.1	ns
C_I	Input capacitance		3.0	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1, 2	30	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

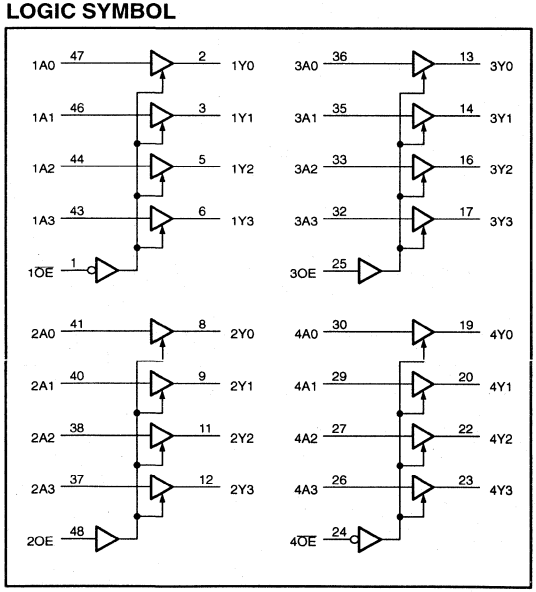
ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16241DL	48	SSOP48	Plastic	SSOP48/SOT370
74ALVC16241DGG	48	TSSOP48	Plastic	TSSOP48/SOT362

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	'1' output enable input (active LOW)
2, 3, 5, 6	1Y0 to 1Y3	1Y data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
8, 9, 11, 12	2Y0 to 2Y3	2Y data outputs
13, 14, 16, 17	3Y0 to 3Y3	3Y data outputs
19, 20, 22, 23	4Y0 to 4Y3	4Y data outputs
24	$4\overline{OE}$	'4' output enable input (active LOW)
25	3OE	'3' output enable input (active LOW)
30, 29, 27, 26	4A0 to 4A3	4A data inputs
36, 35, 33, 32	3A0 to 3A3	3A data inputs
41, 40, 38, 37	2A0 to 2A3	2A data inputs
47, 46, 44, 43	1A0 to 1A3	1A data inputs
48	2OE	'2' output enable input (active LOW)

LOGIC SYMBOL



FUNCTION TABLES

INPUTS		OUTPUT
$n\overline{OE}$	1An, 4An	1Yn, 4Yn
L	H	H
L	L	L
H	X	Z

INPUTS		OUTPUT
nOE	2An, 3An	2Yn, 3Yn
H	H	H
H	L	L
L	X	Z

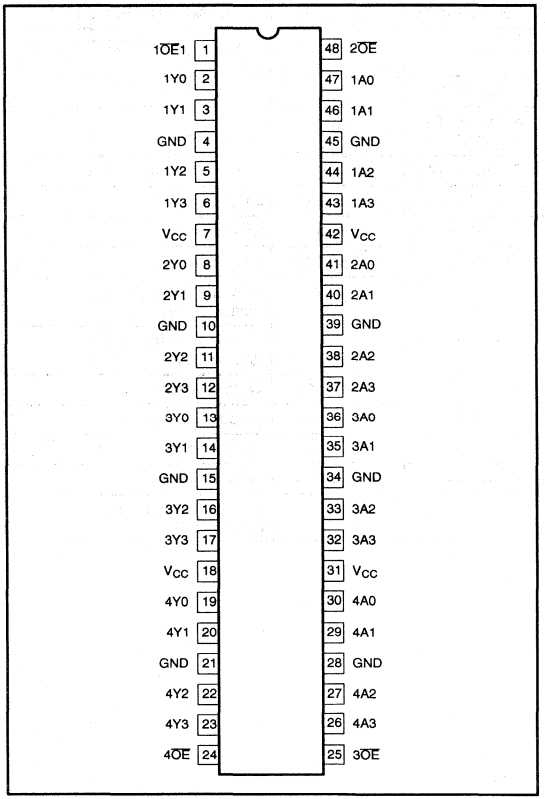
H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

16-bit buffer/line driver; 3-State | 74ALVC16244

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Multibyte™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Bushold on data inputs
- Output drive capability 50Ω transmission lines @ 85°C

PIN CONFIGURATION



DESCRIPTION

The 74ALVC16244 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74ALVC16244 is a 16-bit non-inverting buffer/line driver with 3-State outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The 3-State outputs are controlled by the output enable inputs 1$\overline{OE}$ and 2$\overline{OE}$. A HIGH on n$\overline{OE}$ causes the outputs to assume a high impedance OFF-state. Active bushold circuitry is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer.

The 74ALVC16244 is identical to the 74ALVC16240 but has non-inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay 1An to 1Yn; 2An to 2Yn	C_L = 15pF V_{CC} = 3.3V	2.1	ns
C_I	Input capacitance		3.0	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1, 2	30	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

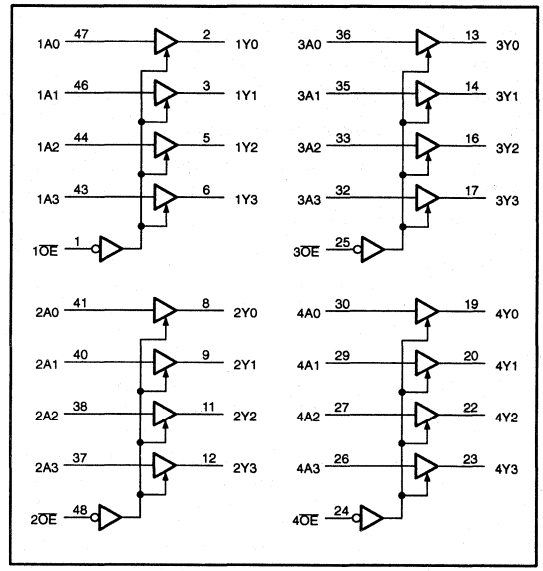
ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16244DL	48	SSOP48	Plastic	SSOP48/SOT370
74ALVC16244DGG	48	TSSOP48	Plastic	TSSOP48/SOT362

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	'1' output enable input (active LOW)
2, 3, 5, 6	1Y0 to 1Y3	1Y data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
8, 9, 11, 12	2Y0 to 2Y3	2Y data outputs
13, 14, 16, 17	3Y0 to 3Y3	3Y data outputs
19, 20, 22, 23	4Y0 to 4Y3	4Y data outputs
24	$4\overline{OE}$	'4' output enable input (active LOW)
25	$3\overline{OE}$	'3' output enable input (active LOW)
30, 29, 27, 26	4A0 to 4A3	4A data inputs
36, 35, 33, 32	3A0 to 3A3	3A data inputs
41, 40, 38, 37	2A0 to 2A3	2A data inputs
47, 46, 44, 43	1A0 to 1A3	1A data inputs
48	$2\overline{OE}$	'2' output enable input (active LOW)

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nAn	nYn
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

16-bit bus transceiver with direction pin; 3-State 74ALVC16245

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Multibyte™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bushold
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74ALVC16245 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74ALVC16245 is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The 74ALVC16245 features two output enable ($n\overline{OE}$) inputs for easy cascading and two send/receive (nDIR) inputs for direction control. $n\overline{OE}$ controls the outputs so that the buses are effectively isolated. This device can be used as two 8-bit transceivers or one 16-bit transceiver.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Bn; Bn to An	C_L = 50pF V_{CC} = 3.3V	2.2	ns
C_I	Input capacitance		3.0	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1, 2	30	pF

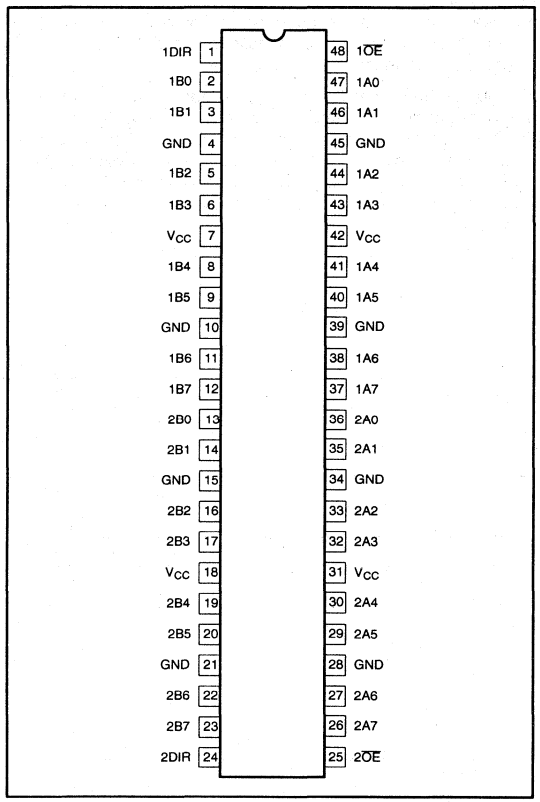
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16245DL	48	SSOP48	Plastic	SSOP48/SOT370
74ALVC16245DGG	48	TSSOP48	Plastic	TSSOP48/SOT362

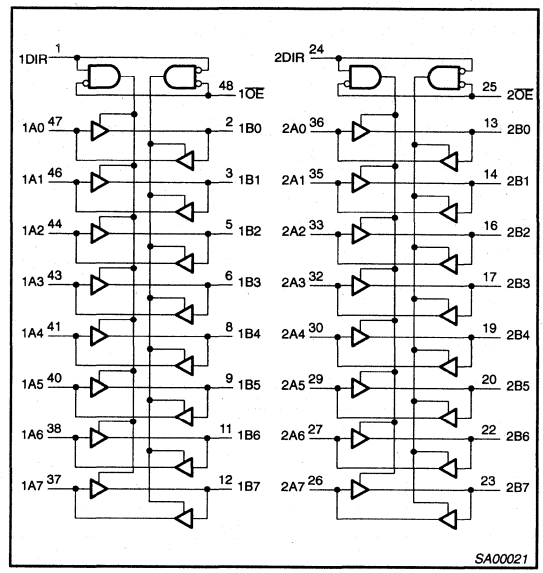
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	1DIR	'1' direction control
2, 3, 5, 6, 8, 9, 11, 12	1B0 to 1B7	1B data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2B0 to 2B7	2B data inputs/outputs
24	2DIR	'2' direction control
25	$2\overline{OE}$	'2' output enable input (active LOW)
36, 35, 33, 32, 30, 29, 27, 26	2A0 to 2A7	2A data inputs/outputs
47, 46, 44, 43, 41, 40, 38, 37	1A0 to 1A7	1A data inputs/outputs
48	$1\overline{OE}$	'1' output enable input (active LOW)

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		INPUTS/OUTPUT	
$n\overline{OE}$	nDIR	nAn	nBn
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

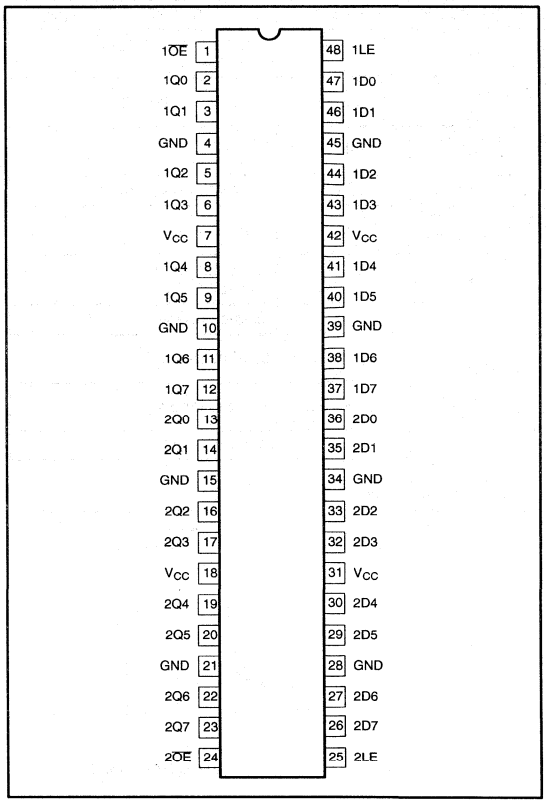
H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF–state

16-bit D-type transparent latch; 3-State 74ALVC16373

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Multibyte™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bushold
- Output drive capability 50Ω transmission lines @ 85°C

PIN CONFIGURATION



DESCRIPTION

The 74ALVC16373 is a 16-bit D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. One latch enable (LE) input and one output enable ($\overline{OE}$) are provided for each octal.

The 74ALVC16373 consists of 2 sections of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the Dn inputs enter the latches. In this condition the latches are transparent, i.e., a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay Dn to Qn; LE to Qn	C_L = 50pF V_{CC} = 3.3V	3.0 3.0	ns
C_I	Input capacitance		3.0	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	25	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

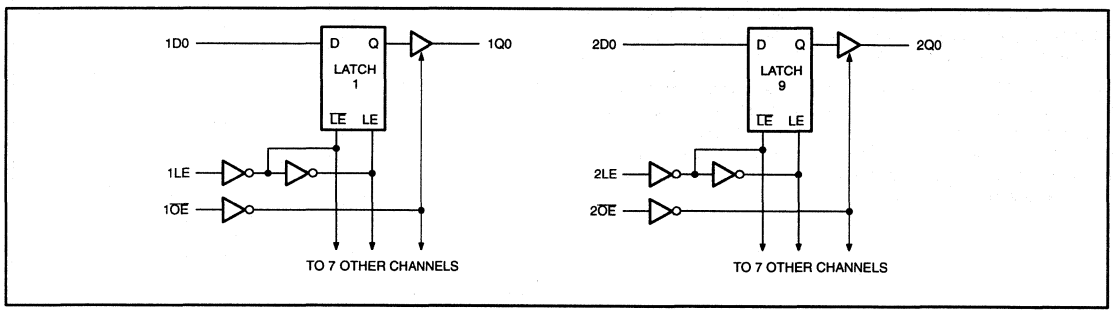
ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16373DL	48	SSOP48	Plastic	SSOP48/SOT370
74ALVC16373DGG	48	TSSOP48	Plastic	TSSOP48/SOT362

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	'1'output enable input (active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	1Q data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	2Q data inputs/outputs
24	$2\overline{OE}$	'2' output enable input (active LOW)
25	2LE	'2' latch enable
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	2D data inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	1D data inputs
48	1LE	'1' latch enable

LOGIC DIAGRAM



FUNCTION TABLE (per section of eight bits)

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	Dn		Q0 to Q7
enable and read register (transparent mode)	L L	H H	L H	L H	L H
latch and read register	L L	L L	l h	L H	L H
latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = don't care
Z = high impedance OFF-state

16-bit edge triggered D-type flip-flop; 3-State 74ALVC16374

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Multibyte™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bushold
- Output drive capability 50Ω transmission lines @ 85°C

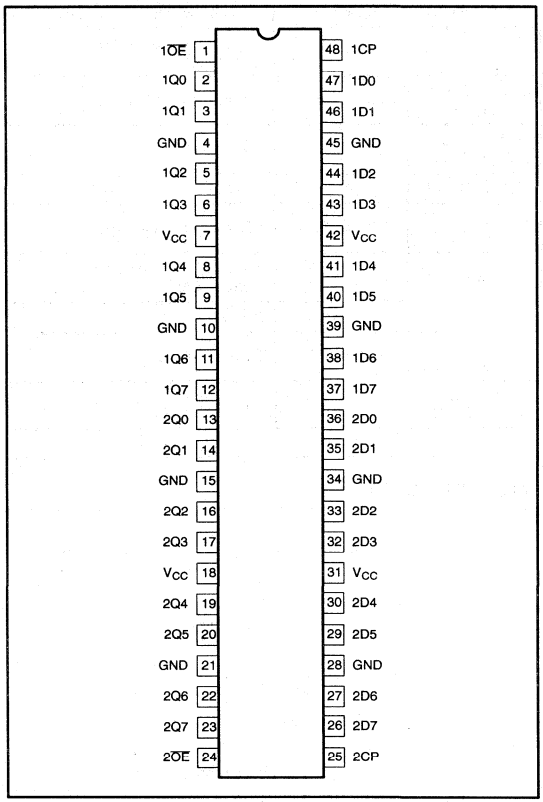
DESCRIPTION

The 74ALVC16374 is a 16-bit edge-triggered flip-flop featuring separate D-type inputs for each flip-flop and 3-State outputs for bus oriented applications.The 74ALVC16374 consists of 2 sections of eight edge-triggered flip-flops. A clock (CP) input and an output enable ($\overline{OE}$) are provided for each octal.

The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

PIN CONFIGURATION



QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay Dn to Qn	C_L = 50pF V_{CC} = 3.3V	3.2	ns
f_{MAX}	Maximum clock frequency		350	MHz
C_I	Input capacitance		3.0	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1, 2	28	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

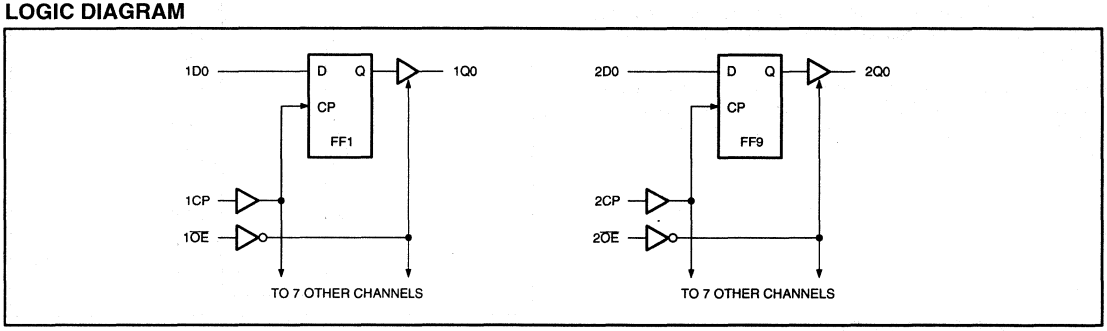
ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16374DL	48	SSOP48	Plastic	SSOP48/SOT370
74ALVC16374DGG	48	TSSOP48	Plastic	TSSOP48/SOT362

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	'1' output enable input (active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	1Q data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	'2Q' data inputs/outputs
24	$2\overline{OE}$	'1' output enable input (active LOW)
25	2CP	'2' clock input
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	2D data inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	1D data inputs
48	1CP	'1' clock input

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0 to Q_7
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH CP transition

18-bit universal bus transceiver; 3-State 74ALVC16500

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Univeral bus transceiver with D-type latches and D-type flip-flops capable of operating in transparant, latched or clocked mode.
- All inputs have bushold circuitry
- Output drive capability 50Ω transmission lines @ 85°C
- 3-State non-inverting outputs for bus oriented applications

DESCRIPTION

The 74ALVC16500 is an 18-bit universal bus transceiver.

Data flow in each direction is controlled by output enable (OE_{AB}, $\overline{OE}_{BA}$), latch-enable (LE_{AB}, LE_{BA}) and clock inputs (CP_{AB}, $\overline{CP}_{BA}$).

When LE_{AB} is HIGH, the A-B dataflow is transparant. When LE_{AB} is LOW, and $\overline{CP}_{AB}$ is held at LOW or HIGH, the A data is latched; on the HIGH-to-LOW transition of $\overline{CP}_{AB}$ the A-data is stored in the latch/flip-flop.

The outputs are active when OE_{AB} is HIGH. When OE_{AB} is LOW the B-outputs are in 3-State.

Similarly, the LE_{BA}, $\overline{OE}_{BA}$ and $\overline{CP}_{BA}$ control the B-to-A dataflow. Please note that both output enables are complementary: OE_{AB} is active HIGH, $\overline{OE}_{BA}$ is active LOW.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Bn LE_{AB} to An	C_L = 50pF V_{CC} = 3.3V	3.0 3.2	ns
C_I	Input capacitance		5.0	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	22	pF

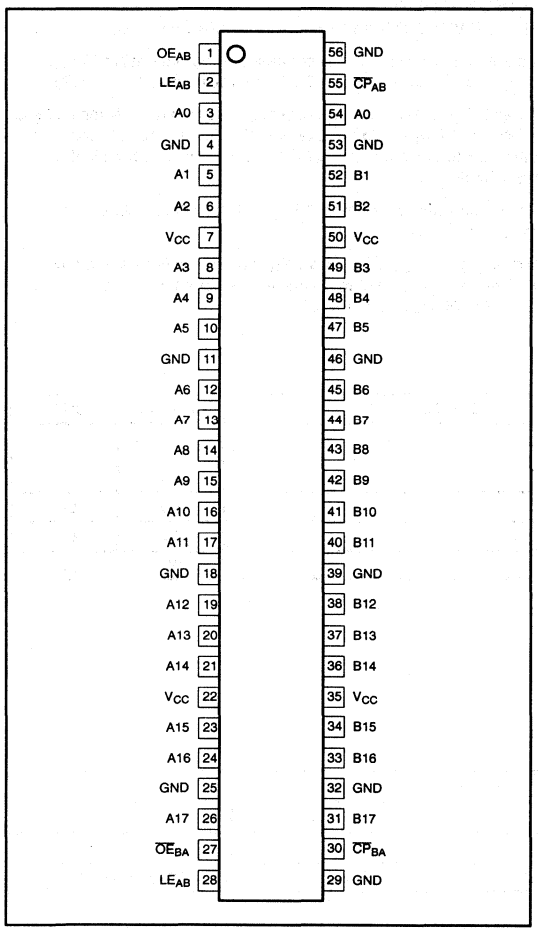
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16500DL	56	SSOP56	Plastic	SSOP56/SOT371
74ALVC16500DGG	56	TSSOP56	Plastic	TSSOP56/SOT364

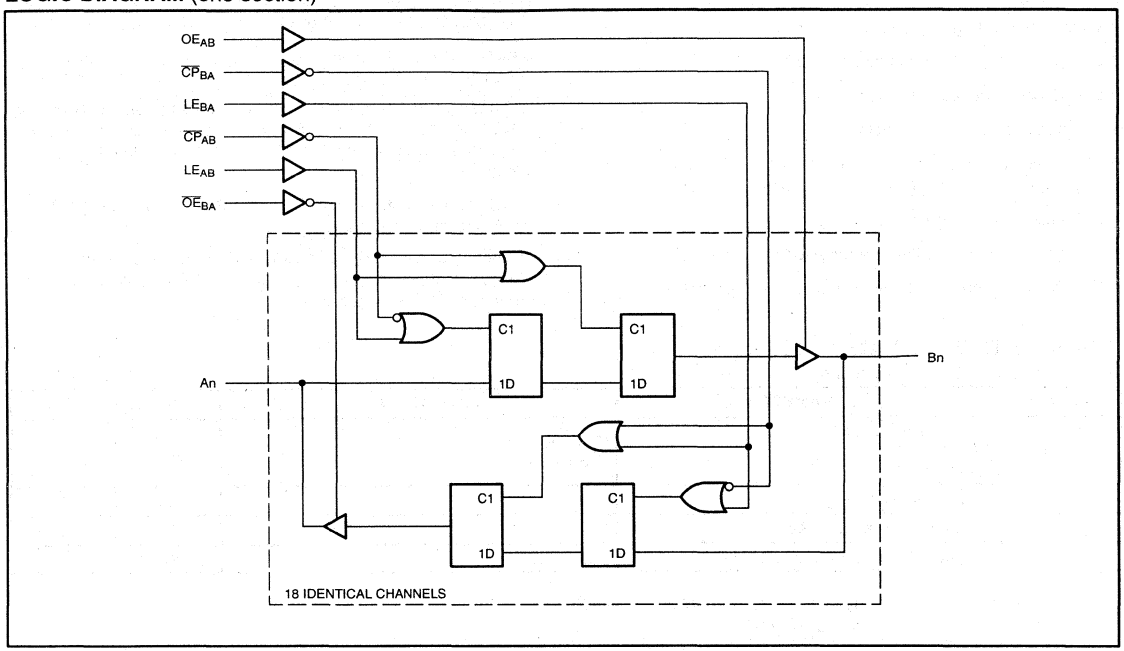
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}_{AB}$	Output enable A-to-B
2	LE_{AB}	Latch enable A-to-B
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0 to A17	'A' data inputs/outputs
4, 11, 18, 25, 29, 32, 39, 46, 53, 56	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage
27	OE_{BA}	Output enable B-to-A
28	LE_{BA}	Latch enable B-to-A
30	$\overline{CP}_{BA}$	Clock input B-to-A, HIGH-to-LOW
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0 to B17	'B' data inputs/outputs
55	$\overline{CP}_{AB}$	Clock input A-to-B, HIGH-to-LOW

LOGIC DIAGRAM (one section)



FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
OE_{AB}[1]	LE_{XX}	$\overline{CP}_{XX}$	DATA		
L	X	X	X	Z	Disabled
H H	H H	X X	H L	H L	Transparant
L L	L L	↓ ↓	h l	Z Z	Disabled + latch
H H	L L	↓ ↓	h l	H L	Latch + display
H H	L L	H L	X X	NC NC1	Hold

NOTE:

1. For the B-to-A direcion $\overline{OE}_{BA}$ is the inverse of OE_{AB}

XX = AB for A-to-B direction, BA for B-to-A direction
H = HIGH voltage level
L = LOW voltage level
h = HIGH state must be present one setup time before the LOW-to-HIGH transition of $\overline{CP}$
l = LOW state must be present one setup time before the LOW-to-HIGH transition of $\overline{CP}$
X = Don't care
↓ = HIGH-to-LOW level transition
NC = No change
NC1 = No change provided that CP was LOW before LE_{XX} went LOW
Z = High impedance "off" state

18-bit universal bus transceiver; 3-State 74ALVC16501

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- Univeral bus transceiver with D-type latches and D-type flip-flops capabable of operating in transparant, latched or clocked mode.
- All inputs have bushold circuitry
- Output drive capability 50Ω transmission lines @ 85°C
- 3-State non-inverting outputs for bus oriented applications

DESCRIPTION

The 74ALVC16501 is an 18-bit universal bus transceiver.

Data flow in each direction is controlled by output enable (OE_{AB}, $\overline{OE}_{BA}$), latch-enable (LE_{AB}, LE_{BA}) and clock inputs (CP_{AB}, CP_{BA}).

When LE_{AB} is HIGH, the A-B dataflow is transparant. When LE_{AB} is LOW, and CP_{AB} is held at LOW or HIGH, the A data is latched; on the LOW-to-HIGH transition of CP_{AB} the A-data is stored in the latch/flip-flop.

The outputs are active when OE_{AB} is HIGH. When OE_{AB} is LOW the B-outputs are in 3-State.

Similarly, the LE_{BA}, $\overline{OE}_{BA}$ and CP_{BA} control the B-to-A dataflow. Please note that both output enables are complementary: OE_{AB} is active HIGH, $\overline{OE}_{BA}$ is active LOW.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Bn LE_{AB} to An	C_L = 50pF V_{CC} = 3.3V	 3.0 3.2	ns
C_I	Input capacitance		5.0	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	22	pF

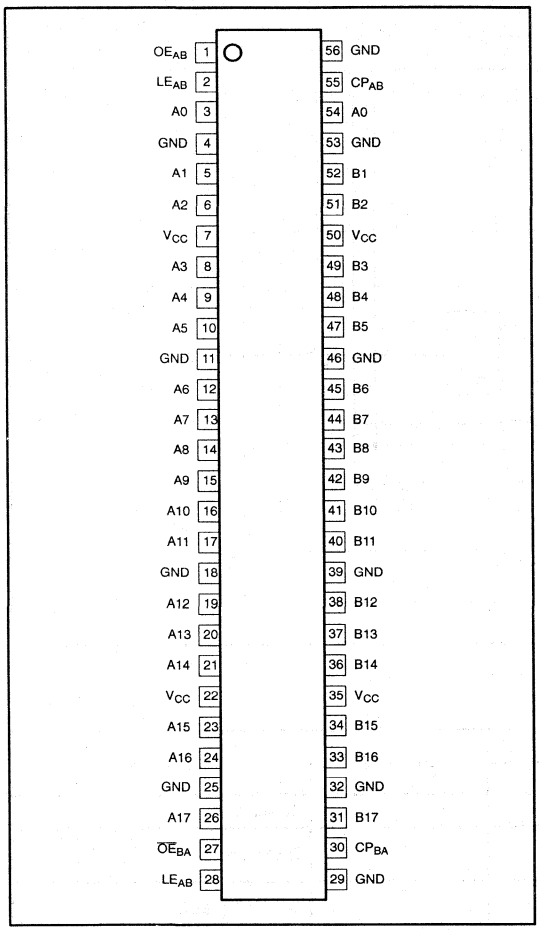
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16501DL	56	SSOP56	Plastic	SSOP56/SOT371
74ALVC16501DGG	56	TSSOP56	Plastic	TSSOP56/SOT364

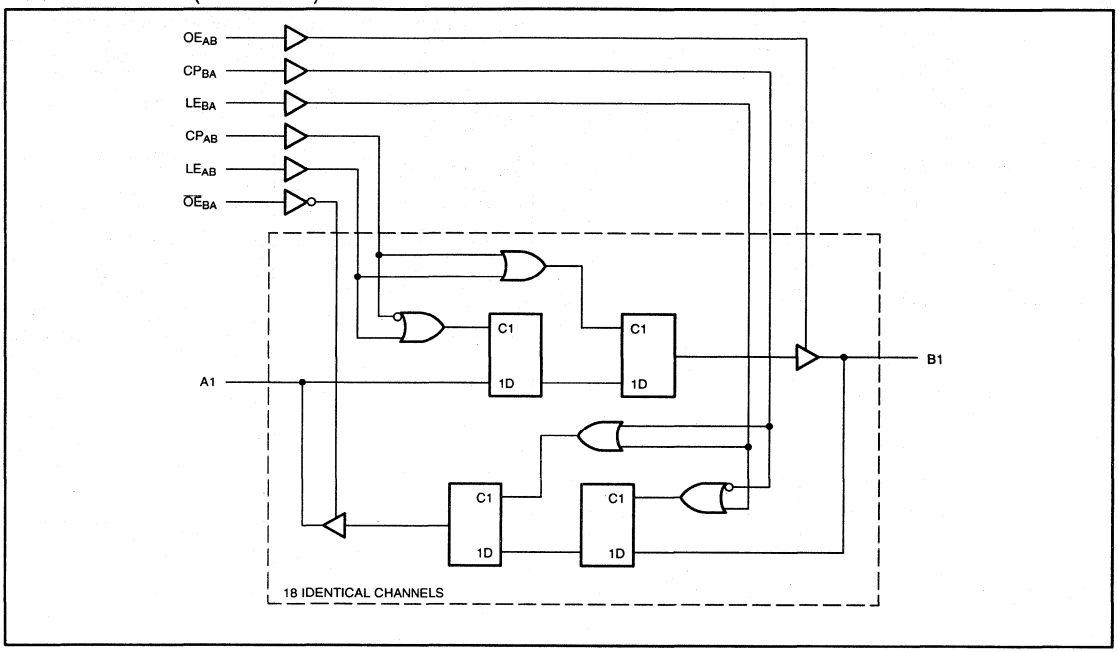
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}_{AB}$	Output enable A-to-B
2	LE_{AB}	Latch enable A-to-B
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0 to A17	'A' data inputs/outputs
4, 11, 18, 25, 29, 32, 39, 46, 53, 56	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage
27	$\overline{OE}_{BA}$	Output enable B-to-A
28	LE_{BA}	Latch enable B-to-A
30	CP_{BA}	Clock input B-to-A, HIGH-to-LOW
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0 to B17	'B' data inputs/outputs
55	$\overline{CP}_{AB}$	Clock input A-to-B, HIGH-to-LOW

LOGIC DIAGRAM (one section)



FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
OE_{AB}[1]	LE_{XX}	CP_{XX}	DATA		
L	X	X	X	Z	Disabled
H H	H H	X X	H L	H L	Transparant
L L	L L	↑ ↑	h l	Z Z	Disabled + latch
H H	L L	↑ ↑	h l	H L	Latch + display
H H	L L	L H	X X	NC NC1	Hold

NOTE:
1. For the B-to-A direcion $\overline{OE}_{BA}$ is the inverse of OE_{AB}

XX = AB for A-to-B direction, BA for B-to-A direction
H = HIGH voltage level
L = LOW voltage level
h = HIGH state must be present one setup time before the LOW-to-HIGH transition of CP
l = LOW state must be present one setup time before the LOW-to-HIGH transition of CP
X = Don't care
↑ = LOW-to-HIGH level transition
NC = No change
NC1 = No change provided that CP was LOW before LE_{XX} went LOW
Z = High impedance "off" state

16-bit buffer/line driver; 3-State; inverting — 74ALVC16540

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Multibyte™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bushold
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74ALVC16540 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74ALVC16540 is a 16-bit inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs $1\overline{OE}_n$ and $2\overline{OE}_n$. A HIGH on $n\overline{OE}_n$ causes the outputs to assume a high impedance OFF-state.

The 74ALVC16540 is identical to the 74ALVC16541 but has inverting outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay 1An to 1Yn; 2An to 2Yn	C_L = 50pF V_{CC} = 3.3V	2.1	ns
C_I	Input capacitance		3.0	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1, 2	30	pF

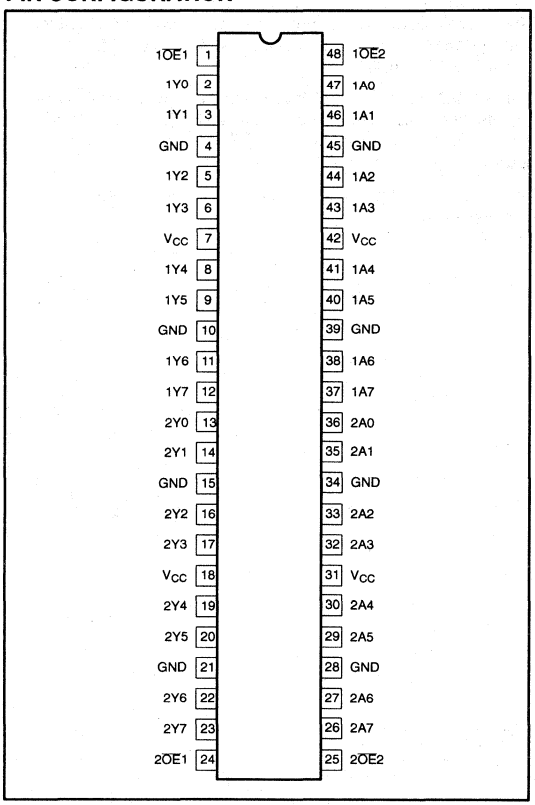
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16540DL	48	SSOP48	Plastic	SSOP48/SOT370
74ALVC16540DGG	48	TSSOP48	Plastic	TSSOP48/SOT362

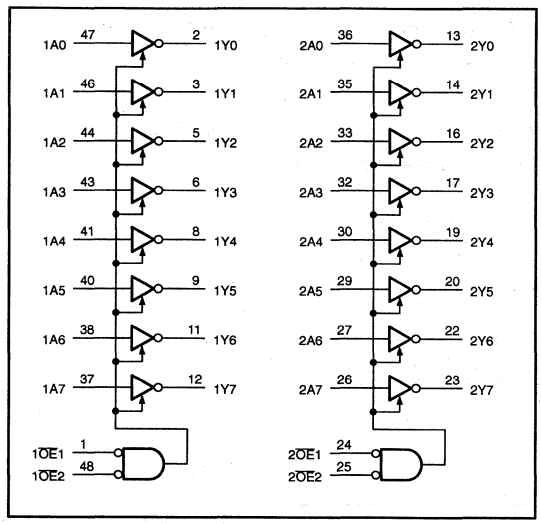
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 24	n$\overline{OE}$1	'1' output enable input (active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Y0 to 1Y7	1Y data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2Y0 to 2Y7	2Y data outputs
25, 48	n$\overline{OE}$2	'2' outut enable input (active LOW)
36, 35, 33, 32, 30, 29, 27, 26	2A0 to 2A7	2A data inputs
47, 46, 44, 43, 41, 40, 38, 37	1A0 to 1A7	1A data inputs

LOGIC SYMBOL



FUNCTION TABLE

INPUTS			OUTPUT
n$\overline{OE}$1	n$\overline{OE}$2	nAn	nYn
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

16-bit D-type registered transceiver; 3-State — 74ALVC16543

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- Complkies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- 16-bit transceiver with D-type latch
- Combines 74ALVC16245 and 74ALVC16373 type functions in one chip
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- 3-State non-inverting outputs for bus oriented applications

DESCRIPTION

The 74ALVC16543 is a dual octal registered transceiver. Each section contains two sets of D-type latches for temporary storage of the data flow in either direction. Separate latch enable ($\overline{LE}_{AB}$, $\overline{LE}_{BA}$) and output enable ($\overline{OE}_{AB}$, $\overline{OE}_{BA}$) inputs are provided for each register to permit independent control in either direction of the data flow.

The 74ALVC16543 contains two sections each consisting of two sets of eight D-type latches with separate inputs and controls for each set. For data flow from A to B, for example, the A-to-B enable ($n\overline{E}_{AB}$, where n equals 1 or 2) input must be LOW in order to enter data from nA0-nA7 or take data from nB0-nB7, as indicated in the function table. With $n\overline{E}_{AB}$ LOW, a LOW signal on the A-to-B latch enable ($n\overline{LE}_{AB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $n\overline{LE}_{AB}$ signal stores the A data into the latches. With $\overline{E}_{AB}$ and $\overline{OE}_{AB}$ both LOW, the 3-State B output buffers are active and display the data present at the output of the A latches. Similarly, the $\overline{E}_{BA}$, $\overline{LE}_{BA}$ and $\overline{OE}_{BA}$ signals control the data flow from B-to-A.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.5ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay Dn to Qn; LE to Qn	C_L = 50pF V_{CC} = 3.3V	3.0 3.2	ns
C_I	Input capacitance		3.0	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	22	pF

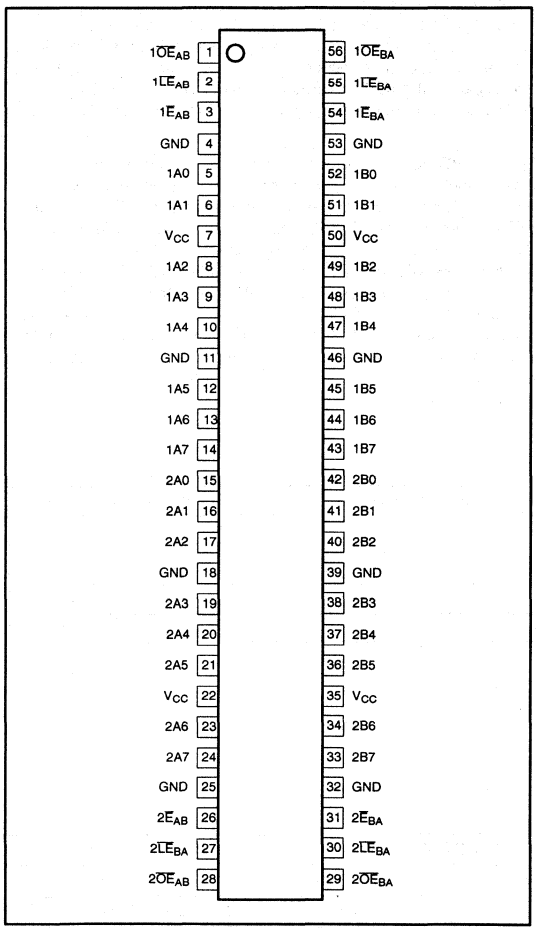
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16543DL	56	SSOP56	Plastic	SSOP56/SOT371
74ALVC16543DGG	56	TSSOP56	Plastic	TSSOP56/SOT364

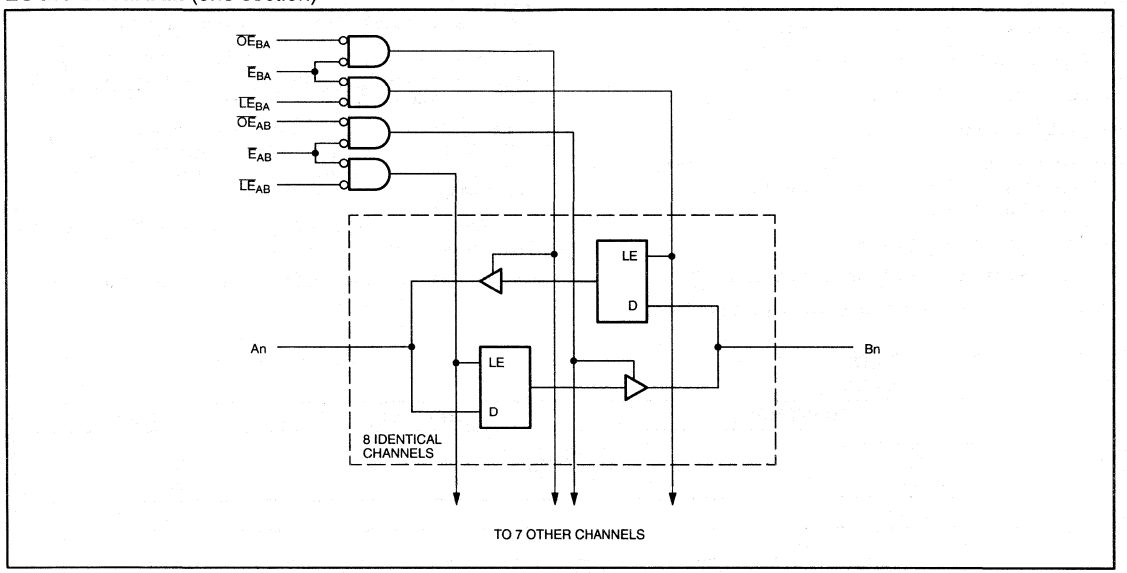
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 28	n$\overline{OE}_{AB}$	Output enable A-to-B for register 1 or 2
2, 27	n$\overline{LE}_{AB}$	Latch enable A-to-B for register 1 or 2
3, 26	n$\overline{E}_{AB}$	A-to-B enable for register 1 or 2
5, 6, 8, 9, 10, 12, 13, 14	1A0 to 1A7	1A data inputs/outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage
15, 16, 17, 19, 20, 21, 23, 24	2B0 to 2B7	2B data inputs/outputs
29, 56	n$\overline{OE}_{BA}$	Output enable B-to-A for register 1 or 2
30, 55	n$\overline{LE}_{BA}$	Latch enable B-to-A for register 1 or 2
31, 54	n$\overline{E}_{BA}$	B-to-A enable for register 1 or 2
42, 41, 40, 38, 37, 36, 34, 33	2B0 to 2B7	2B data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43	1B0 to 1B7	1B data inputs/outputs

LOGIC DIAGRAM (one section)



FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OE}_{XX}$	$\overline{E}_{XX}$	$\overline{LE}_{XX}$	DATA		
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	H L	Latch + Display
L L	L L	L L	H L	H L	Transparent
L	L	H	X	NC	Hold

XX = AB for A-to-B direction, BA for B-to-A direction
H = HIGH voltage level
L = LOW voltage level
h = HIGH state must be present one setup time before the LOW-to-HIGH transition of $\overline{LE}_{AB}$, $\overline{LE}_{BA}$, $\overline{E}_{AB}$ or $\overline{E}_{BA}$
l = LOW state must be present one setup time before the LOW-to-HIGH transition of $\overline{LE}_{AB}$, $\overline{LE}_{BA}$, $\overline{E}_{AB}$ or $\overline{E}_{BA}$
X = Don't care
↑ = LOW-to-HIGH level transition
NC = No change
Z = High impedance "off" state

18-bit universal bus transceiver; 3-State 74ALVC16600

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Universal bus transceiver with D-type latches and D-type flip-flops capable of operating in transparant, latched, clocked or clocked-enabled mode.
- All inputs have bushold circuitry
- Output drive capability 50Ω transmission lines @ 85°C
- 3-State non-inverting outputs for bus oriented applications

DESCRIPTION

The 74ALVC16600 is an 18-bit universal bus transceiver.

Data flow in each direction is controlled by output enable ($\overline{OE}_{AB}$, $\overline{OE}_{BA}$), latch-enable (LE_{AB}, LE_{BA}) and clock inputs ($\overline{CP}_{AB}$, $\overline{CP}_{BA}$). The clock enable inputs ($\overline{CE}_{AB}$, $\overline{CE}_{BA}$) control the clock.

When LE_{AB} is HIGH, the A-B dataflow is transparant. When LE_{AB} is LOW, and $\overline{CP}_{AB}$ is held at LOW or HIGH, the A data is latched; on the HIGH-to-LOW transition of $\overline{CP}_{AB}$ the A-data is stored in the latch/flip-flop.

The outputs are active when $\overline{OE}_{AB}$ is LOW. When $\overline{OE}_{AB}$ is LOW the B-outputs are in 3-State.

Similarly, the LE_{BA}, $\overline{OE}_{BA}$ and $\overline{CP}_{BA}$ control the B-to-A dataflow.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.5ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Bn; LE_{AB} to An	C_L = 50pF V_{CC} = 3.3V	3.0 3.2	ns
C_I	Input capacitance		5.0	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	22	pF

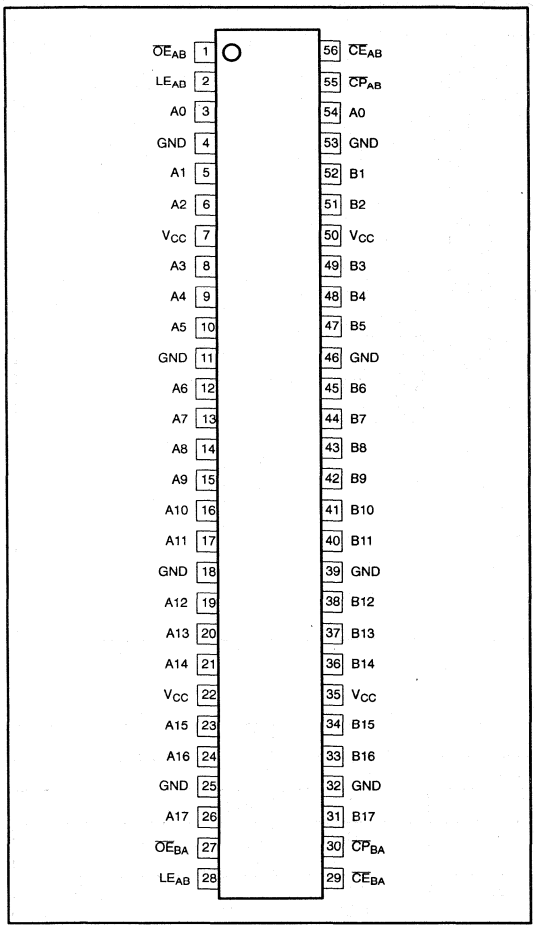
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16600DL	56	SSOP56	Plastic	SSOP56/SOT371
74ALVC16600DGG	56	TSSOP56	Plastic	TSSOP56/SOT364

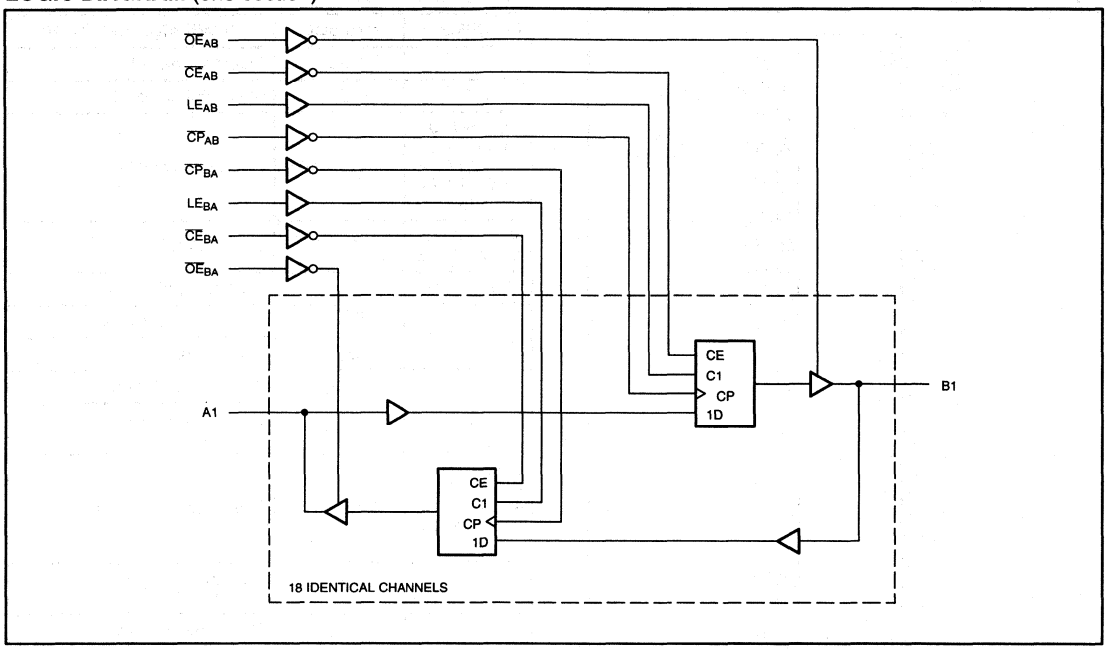
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}_{AB}$	Output enable A-to-B
2	LE_{AB}	Latch enable A-to-B
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0 to A17	'A' data inputs/outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage
27	$\overline{OE}_{BA}$	Output enable B-to-A
28	LE_{BA}	Latch enable B-to-A
29	$\overline{CE}_{BA}$	Clock enable B-to-A
30	$\overline{CP}_{BA}$	Clock input B-to-A, HIGH-to-LOW
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0 to B17	'B' data inputs/outputs
55	$\overline{CP}_{AB}$	Clock input A-to-B, HIGH-to-LOW
56	$\overline{CE}_{AB}$	Clock enable A-to-B

LOGIC DIAGRAM (one section)



FUNCTION TABLE

INPUTS					OUTPUTS	STATUS
$\overline{CE}_{XX}$	$\overline{OE}_{XX}$	LE_{XX}	$\overline{CP}_{XX}$	DATA		
X	H	X	X	X	Z	Disabled
X X	L L	H H	X X	H L	H L	Transparent
H H	L L	L L	X X	X X	NC NC1	Hold
L L	L L	L L	↓ ↓	h l	Z Z	Disabled + latch
L L	L L	L L	↓ ↓	h l	H L	Latch + display
L L	L L	L L	H L	X X	NC NC1	Hold

XX = AB for A-to-B direction, BA for B-to-A direction
H = HIGH voltage level
L = LOW voltage level
h = HIGH state must be present one setup time before the LOW-to-HIGH transition of $\overline{CP}_{XX}$
l = LOW state must be present one setup time before the LOW-to-HIGH transition of $\overline{CP}_{XX}$
X = Don't care
↓ = HIGH-to-LOW level transition
NC = No change
NC1 = No change provided that $\overline{CP}_{XX}$ was LOW before LE_{XX} went LOW
Z = High impedance "off" state

18-bit universal bus transceiver; 3-State — 74ALVC16601

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- Univeral bus transceiver with D-type latches and D-type flip-flops capable of operating in transparant, latched or clocked mode.
- All inputs have bushold circuitry
- Output drive capability 50Ω transmission lines @ 85°C
- 3-State non-inverting outputs for bus oriented applications

DESCRIPTION

The 74ALVC16601 is an 18-bit universal bus transceiver.

Data flow in each direction is controlled by output enable (OE_{AB}, $\overline{OE}_{BA}$), latch-enable (LE_{AB}, LE_{BA}) and clock inputs (CP_{AB}, CP_{BA}).

When LE_{AB} is HIGH, the A-B dataflow is transparant. When LE_{AB} is LOW, and CP_{AB} is held at LOW or HIGH, the A data is latched; on the LOW-to-HIGH transition of CP_{AB} the A-data is stored in the latch/flip-flop.

The outputs are active when $\overline{OE}_{AB}$ is HIGH. When OE_{AB} is LOW the B-outputs are in 3-State.

Similarly, the LE_{BA}, OE_{BA} and CP_{BA} control the B-to-A dataflow. Please note that both output enables are complementary: OE_{AB} is active HIGH, $\overline{OE}_{BA}$ is active LOW.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Bn; LE_{AB} to An	C_L = 50pF V_{CC} = 3.3V	3.0 3.2	ns
C_I	Input capacitance		5.0	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	22	pF

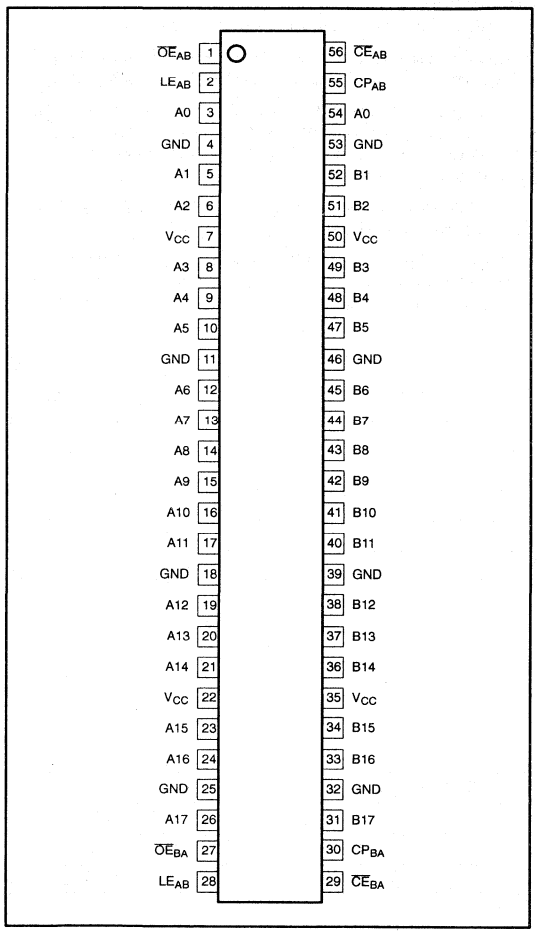
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16601DL	56	SSOP56	Plastic	SSOP56/SOT371
74ALVC16601DGG	56	TSSOP56	Plastic	TSSOP56/SOT364

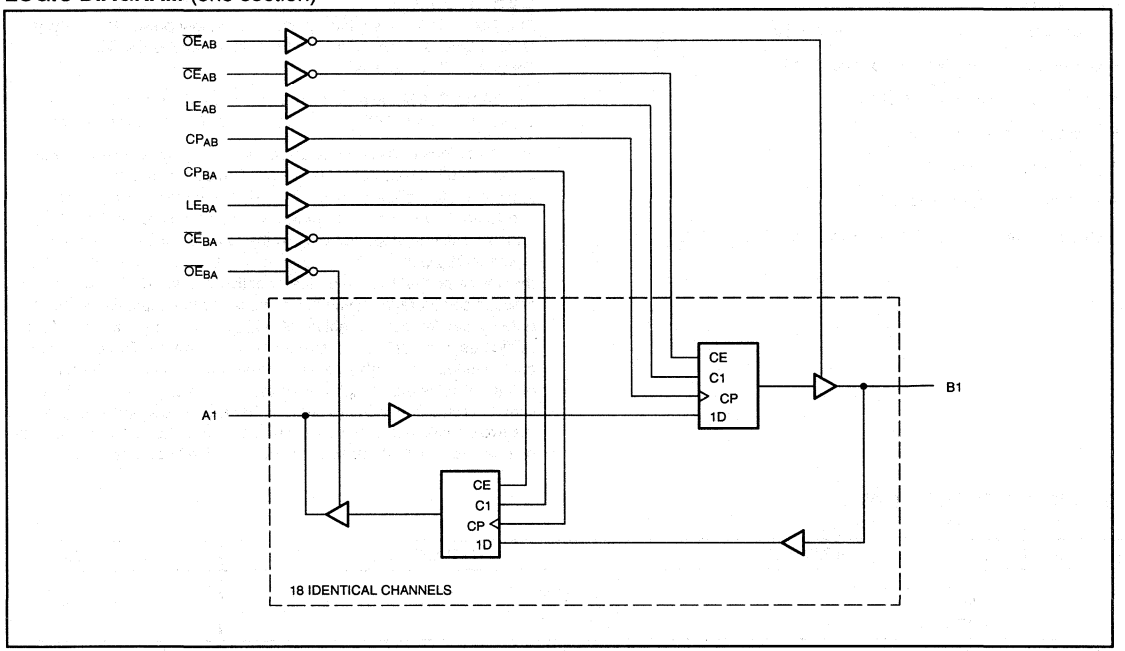
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}_{AB}$	Output enable A-to-B
2	LE_{AB}	Latch enable A-to-B
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0 to A17	A data inputs/outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage
27	$\overline{OE}_{BA}$	Output enable B-to-A
28	LE_{BA}	Latch enable B-to-A
29	$\overline{CE}_{BA}$	Clock enable B-to-A
30	CP_{BA}	Clock input B-to-A, HIGH-to-LOW
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0 to B17	B data inputs/outputs
55	CP_{AB}	Clock input A-to-B, HIGH-to-LOW
56	$\overline{CE}_{AB}$	Clock enable A-to-B

LOGIC DIAGRAM (one section)



FUNCTION TABLE

INPUTS					OUTPUTS	STATUS
$\overline{CE}_{XX}$	$\overline{OE}_{XX}$	LE_{XX}	CP_{XX}	DATA		
X	H	X	X	X	Z	Disabled
X X	L L	H H	X X	H L	H L	Transparent
H H	L L	L L	X X	X X	NC NC1	Hold
L L	L L	L L	↑ ↑	h l	Z Z	Disabled + latch
L L	L L	L L	↑ ↑	h l	H L	Latch + display
L L	L L	L L	L H	X X	NC NC1	Hold

XX = AB for A-to-B direction, BA for B-to-A direction
H = HIGH voltage level
L = LOW voltage level
h = HIGH state must be present one setup time before the LOW-to-HIGH transition of CP_{XX}
l = LOW state must be present one setup time before the LOW-to-HIGH transition of CP_{XX}
X = Don't care
↑ = LOW-to-HIGH level transition
NC = No change
NC1 = No change provided that CP_{XX} was LOW before LE_{XX} went LOW
Z = High impedance "off" state

16-bit transceiver with dual enable; 3-State 74ALVC16623

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8–1A
- CMOS low power consumption
- Multibyte™ pin-out architecture
- Direct interface with TTL levels
- All data inputs have bushold
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74ALVC16623 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74ALVC16623 is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions.

This 16-bit bus transceiver is designed for asynchronous two-way communication between data buses. The control function implementation allows maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the enable inputs (nOE_{AB}, $n\overline{OE}_{BA}$). The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual enable function configuration gives this transceiver the capability to store data by simultaneous enabling of nOE_{AB} and $n\overline{OE}_{BA}$. Each output reinforces its input in this transceiver configuration. Thus, when all control inputs are enabled and all other data sources to the four sets of the bus lines are at high impedance OFF-state, all sets of bus lines will remain at their last states. The 8-bit codes appearing on the two double sets of buses will be complementary. This device can be used as two 8-bit transceivers or one 16-bit transceiver.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Bn; Bn to An	C_L = 50pF V_{CC} = 3.3V	2.7	ns
C_I	Input capacitance		3.0	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1, 2	35	pF

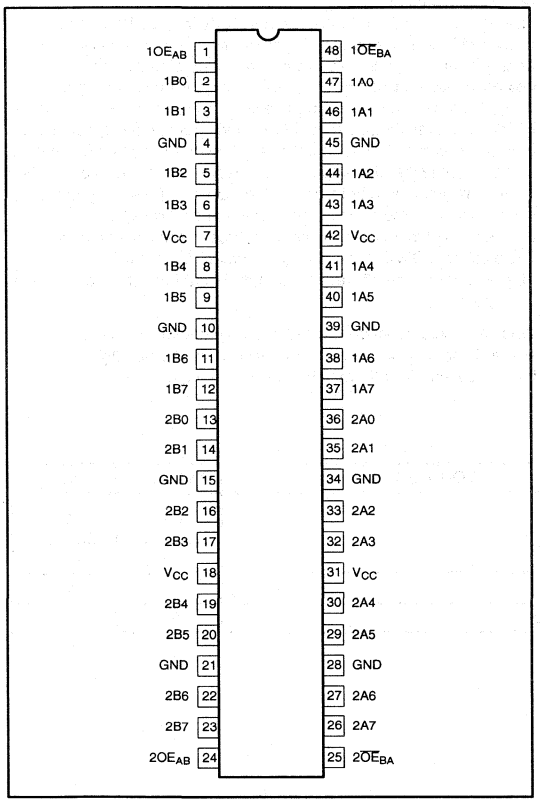
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

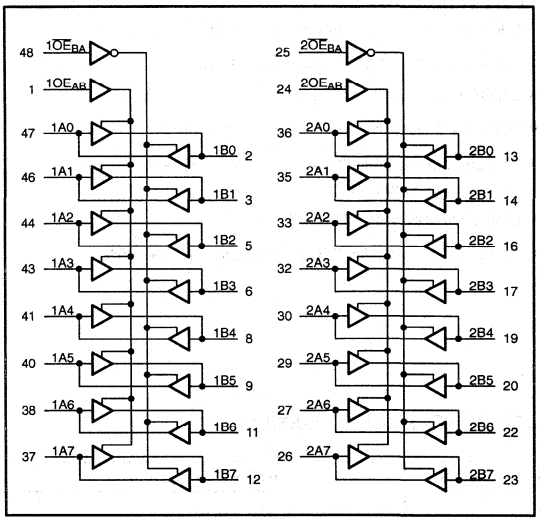
ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16623DL	48	SSOP48	Plastic	SSOP48/SOT370
74ALVC16623DGG	48	TSSOP48	Plastic	TSSOP48/SOT362

PIN CONFIGURATION



LOGIC SYMBOL



FUNCTION TABLE

ENABLE INPUTS		OPERATION
nOE$_{AB}$	n$\overline{OE}_{BA}$	
L	L	B data to A bus
H	H	A data to B bus
L	H	Z
H	L	B data to A bus, A data to B bus

H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	1OE$_{AB}$	'1' output enable input (active HIGH)
2, 3, 5, 6, 8, 9, 11, 12	1B0 to 1B7	1B data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2B0 to 2B7	2B data inputs/outputs
24	2OE$_{AB}$	'2' output enable input (active HIGH)
25	2$\overline{OE}_{BA}$	'2' output enable input (active LOW)
36, 35, 33, 32, 30, 29, 27, 26	2A0 to 2A7	2A data inputs/outputs
47, 46, 44, 43, 41, 40, 38, 37	1A0 to 1A7	1A data inputs/outputs
48	1$\overline{OE}_{BA}$	'1' output enable input (active LOW)

16-bit bus transceiver/register; 3-State 74ALVC16646

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Multibyte™ flow-through pin-out architecture
- Low inductance, multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74ALVC16646 consists of 16 non-inverting bus transceiver circuits with 3-State outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the 'A' or 'B' bus will be clocked in the internal registers, as the appropiate clock (CP_{AB} or CP_{BA}) goes to a HIGH logic level. Output enable ($\overline{OE}$) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the 'A' or 'B' register, or in both. The select source inputs (S_{AB} and S_{BA}) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when $\overline{OE}$ is active (LOW). In the isolation mode ($\overline{OE}$ = HIGH), 'A' data may be stored in the 'B' register and/or 'B' data may be stored in the 'A' register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, 'A' or 'B' may be driven at a time.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.5ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An , Bn to Bn, An	C_L = 50pF V_{CC} = 3.3V	3.2	ns
f_{MAX}	Maximum clock frequency		350	MHz
C_I	Input capacitance		3.0	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	30	pF

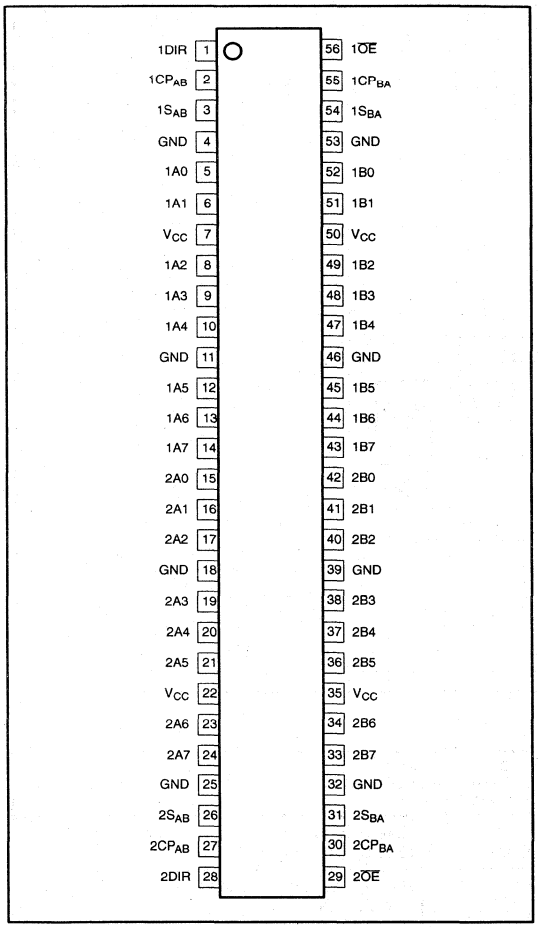
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16646DL	56	SSOP56	Plastic	SSOP56/SOT371
74ALVC16646DGG	56	TSSOP56	Plastic	TSSOP56/SOT364

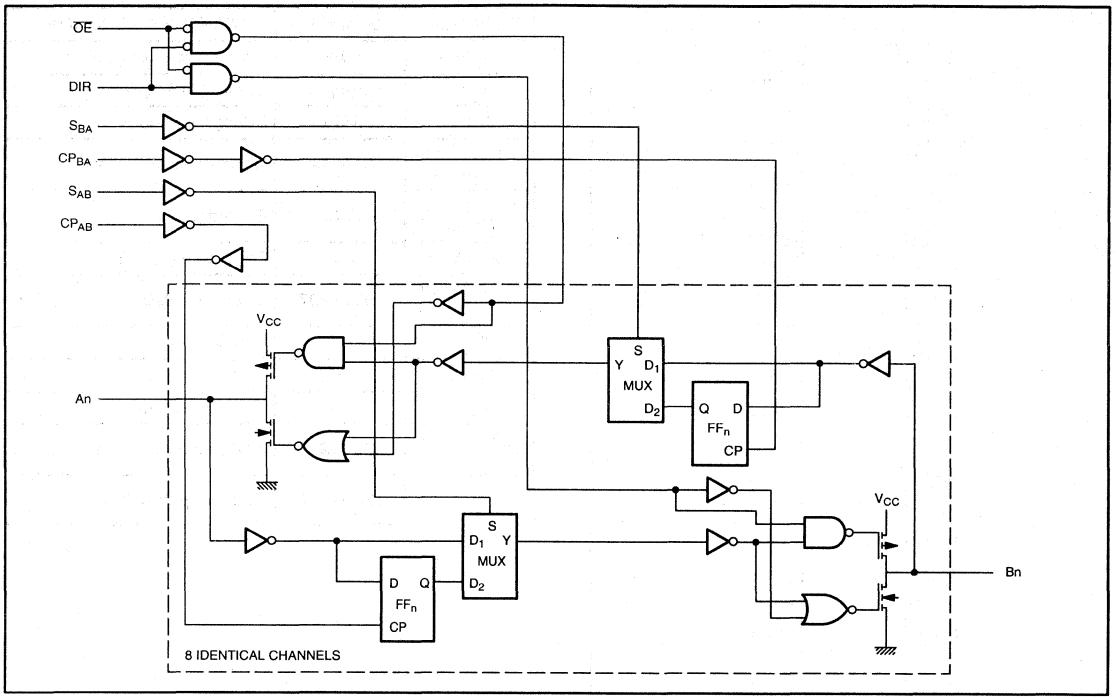
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 28	nDIR	Direction control input
2, 27	nCP_{AB}	Clock input A-to-B
3, 26	nS_{AB}	Select input A-to-B
5, 6, 8, 9, 10, 12, 13, 14	1A0 to 1A7	1A data inputs/outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage
15, 16, 17, 19, 20, 21, 23, 24	2B0 to 2B7	2B data inputs/outputs
29, 56	$n\overline{OE}$	Output enable
30, 55	nCP_{BA}	Clock input B-to-A
31, 54	nS_{BA}	Select input B-to-A
42, 41, 40, 38, 37, 36, 34, 33	2B0 to 2B7	2B data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43	1B0 to 1B7	1B data inputs/oututs

LOGIC SYMBOL



FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A0 to A7	B0 to B7	
X X	X X	↑ X	X ↑	X X	X X	input un*	un* input	store A, B unspecified* store B, A unspecified*
H H	X X	↑ H or L	↑ H or L	X X	X X	input	input	store A and B data, isolation hold storage
L L	L L	X X	X H or L	X X	L H	output	input	real-time B data to A bus stored B data to A bus
L L	H H	X H or L	X X	L H	X X	input	output	real-time A data to B bus stored A data to B bus

* The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

16-bit transceiver/register with dual enable; 3-State 74ALVC16652

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Multibyte™ flow-through pin-out architecture
- Low inductance, multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74ALVC16652 consist of 16 non-inverting bus transceiver circuits with 3-State outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the 'A' or 'B' or both buses, will be stored in the internal registers, at the appropiate clock inputs (CP_{AB} or CP_{BA}) regardless of the select inputs (S_{AB} and S_{BA}) or output enable (OE_{AB} and $\overline{OE}_{BA}$) control inputs. Depending on the select inputs S_{AB} and S_{BA} data can directly go from input to output (real time mode) or data can be controlled by the clock (storage mode), this is when the OE inputs permit this operating mode. The output enable inputs OE_{AB} and $\overline{OE}_{BA}$ determine the operation mode of the transceiver. When OE_{AB} is LOW, no data transmission from An to Bn is possible and when $\overline{OE}_{BA}$ is HIGH, there is no data transmission from Bn to An possible. When S_{AB} and S_{BA} are in the real time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OE_{AB} and $\overline{OE}_{BA}$. In this configuration each output reinforces its input.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An, Bn to Bn, An	C_L = 50pF; V_{CC} = 3.3V	3.2	ns
f_{MAX}	Maximum clock frequency		350	MHz
C_I	Input capacitance		3.0	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	30	pF

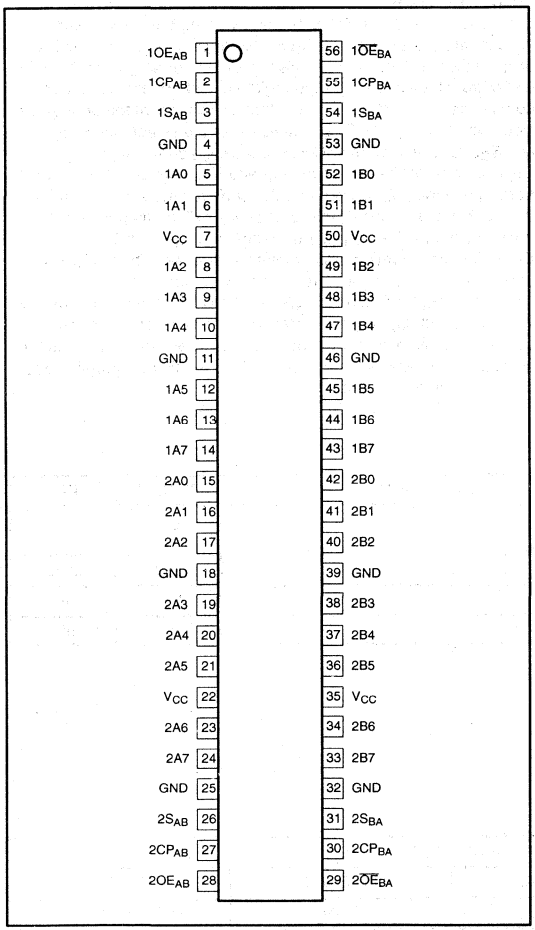
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16652DL	56	SSOP56	Plastic	SSOP56/SOT371
74ALVC16652DGG	56	TSSOP56	Plastic	TSSOP56/SOT364

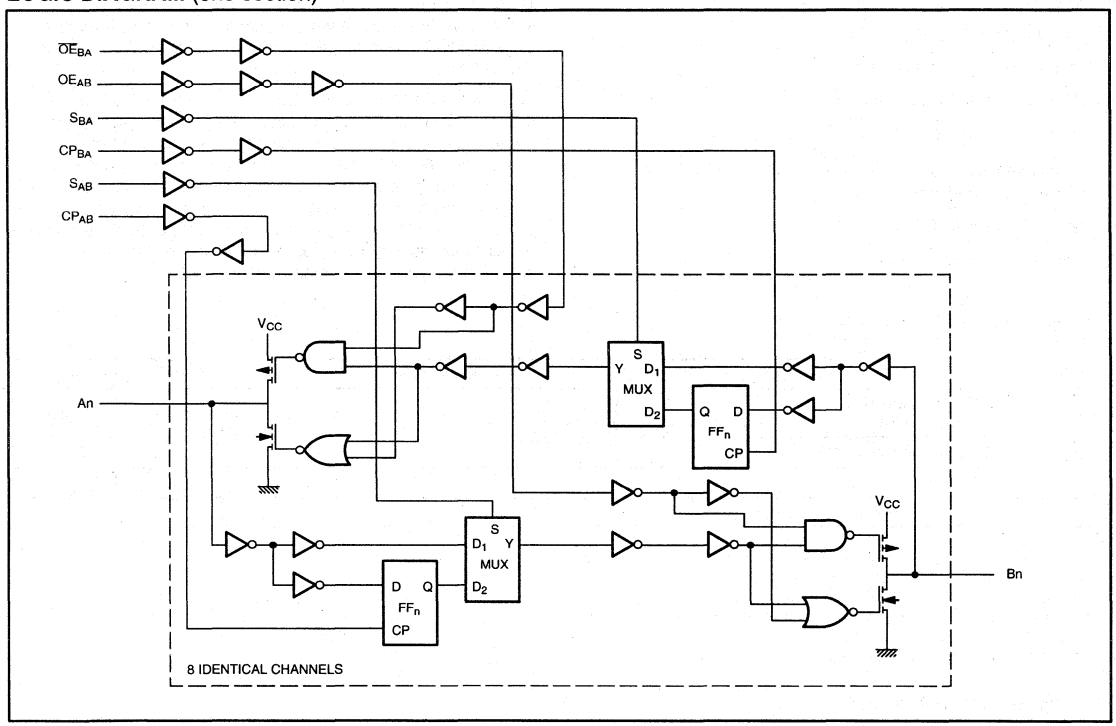
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 28	nOE$_{AB}$	Output enable A-to-B
2, 27	nCP$_{AB}$	Clock input A-to-B
3, 26	nS$_{AB}$	Select input A-to-B
5, 6, 8, 9, 10, 12, 13, 14	1A0 to 1A7	1A data inputs/outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V$_{CC}$	Positive supply voltage
15, 16, 17, 19, 20, 21, 23, 24	2B0 to 2B7	2B data inputs/outputs
29, 56	n$\overline{OE}_{BA}$	Output enable B-to-A
30, 55	nCP$_{BA}$	Clock input B-to-A
31, 54	nS$_{BA}$	Select input B-to-A
42, 41, 40, 38, 37, 36, 34, 33	2B0 to 2B7	2B data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43	1B0 to 1B7	1B data inputs/outputs

LOGIC DIAGRAM (one section)



FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A0 to A7	B0 to B7	
L L	H H	H or L ↑	H or L ↑	X X	X X	input	input	isolation store A and B data
X H	H H	↑ ↑	H or L ↑	X L	X X	input input	un* output	store A, hold B store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X L	un* output	input input	hold A, store B store B in both registers
L L	L L	X X	X H or L	X X	L H	output	input	real time B data to A bus stored B data to A bus
H H	H H	X H or L	X X	L H	X X	input	output	real-time A data to B bus stored A data to B bus
H	L	H or L	H or L	H	H	output	output	stored A data to B bus and stored B data to A bus

* The data output functions may be enabled or disabled by various signals at the OE_{AB} and $\overline{OE}_{BA}$ inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

16-bit registered transceiver; 3-State 74ALVC16952

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Multibyte™ flow-through pin-out architecture
- Low inductance, multiple center power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74ALVC16952 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74ALVC16952 consists of two sections, each containing a dual octal non-inverting registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bi-directional busses. Data applied to the inputs is entered and stored on the rising edge of the clock (CP_{XX}, where X is AB or BA) provided that the clock enable ($\overline{CE}_{XX}$) is LOW. The data is then present at the 3-State output buffers, but is only accessible when the output enable input ($\overline{OE}_{XX}$) is LOW. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.5ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An, Bn to Bn, An	C_L = 50pF; V_{CC} = 3.3V	3.2	ns
f_{MAX}	Maximum clock frequency		350	MHz
C_I	Input capacitance		3.0	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1, 2	30	pF

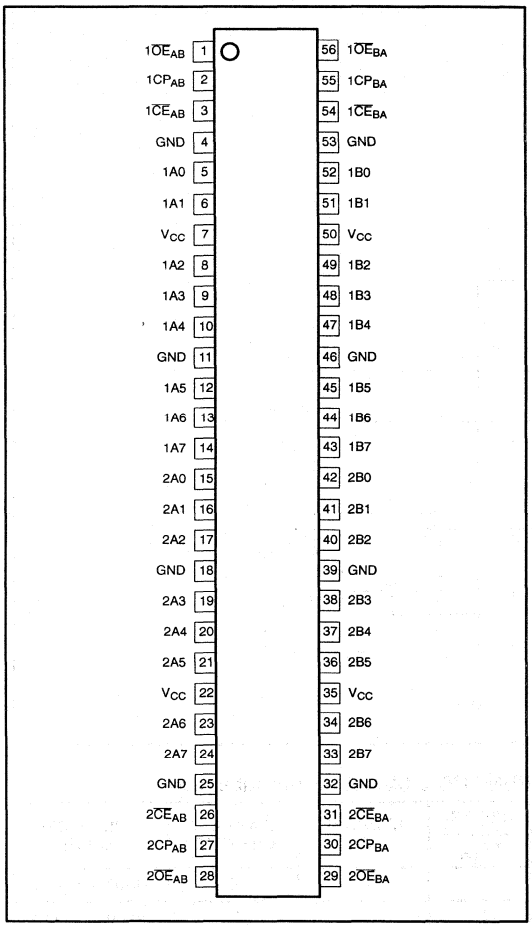
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16952DL	56	SSOP56	Plastic	SSOP56/SOT371
74ALVC16952DGG	56	TSSOP56	Plastic	TSSOP56/SOT364

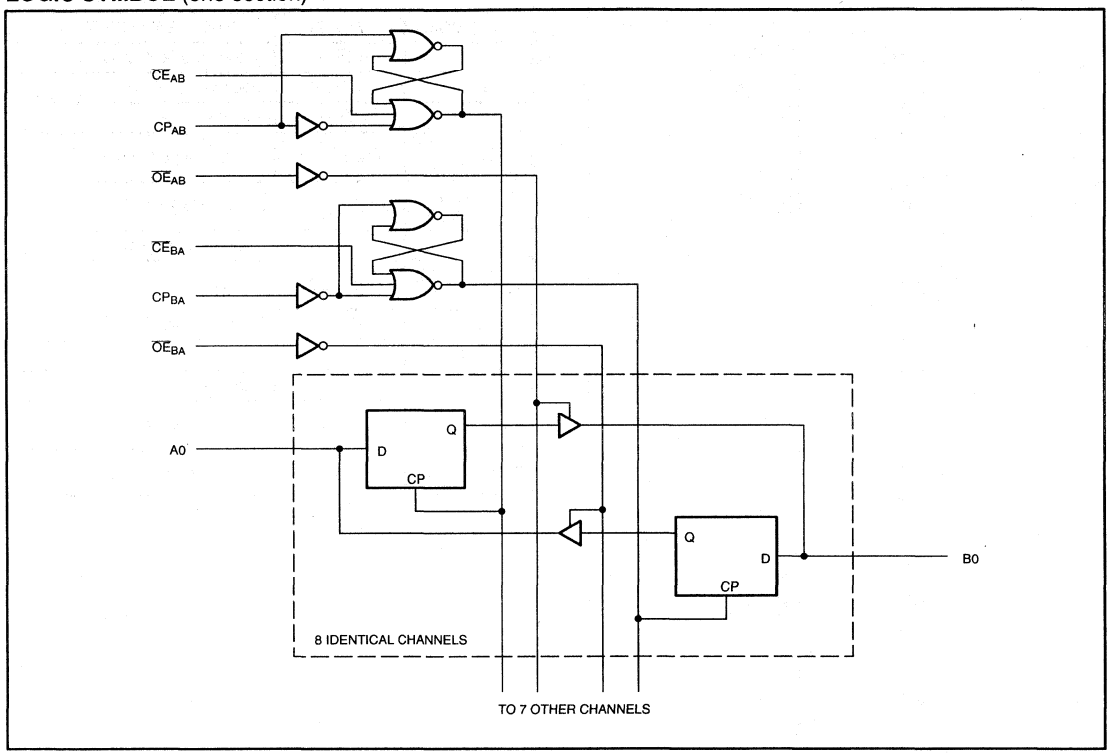
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 28	n$\overline{OE}_{AB}$	Output enable A-to-B
2, 27	nCP_{AB}	Clock input A-to-B
3, 26	n$\overline{CE}_{AB}$	A-to-B enable
5, 6, 8, 9, 10, 12, 13, 14	1A0 to 1A7	1A data inputs/outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage
15, 16, 17, 19, 20, 21, 23, 24	2B0 to 2B7	2B data inputs/outputs
29, 56	n$\overline{OE}_{BA}$	Output enable B-to-A
30, 55	nCP_{BA}	Clock input B-to-A
31, 54	n$\overline{CE}_{BA}$	B-to-A enable
42, 41, 40, 38, 37, 36, 34, 33	2B0 to 2B7	2B data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43	1B0 to 1B7	1B data inputs/outputs

LOGIC SYMBOL (one section)



FUNCTION TABLE for register An or Bn

INPUTS			INTERNAL Q	OPERATING MODE
An or Bn	CP_{XX}	$\overline{CE}_{XX}$		
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	Load data

H = HIGH voltage level
L = LOW voltage level
↑ = LOW-to-HIGH transition

FUNCTION TABLE for output enable

INPUTS	INTERNAL Q	An or Bn OUTPUTS	OPERATING MODE
$\overline{OE}_{nn}$			
H	X	Z	Disable outputs
L	L	L	Enable outputs
L	H	H	Enable outputs

NC = no change
X = don't care
Z = high impedance OFF-state

16-bit dual supply translating transceiver; 3-State 74ALVC164245

FEATURES

- Wide supply voltage range
  - A port: 1.2 to 3.6V
  - B port: 1.2 to 5.5V
- Complies with JEDEC standard no. 8-1A
- Control inputs voltage range from 2.7V to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels

DESCRIPTION

The 74ALVC164245 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74ALVC164245 is a 16-bit (dual-octal) translating transceiver and is designed to interface between a 5V bus and 3V bus in a mixed 3V/5V supply environment. This device can be used as two 8-bit transceivers or one 16-bit transceiver. The direction control inputs (1DIR, 2DIR) determine the direction of the data flow. nDIR (active HIGH) enables data from nA ports to nB ports. nDIR (active LOW) enables data from nB ports to nA ports.The output enable inputs ($1\overline{OE}$, $2\overline{OE}$), when HIGH, disable both nA and nB ports by placing them in a high impedance OFF-state. The nB ports interface with the 5V bus. The nA ports interface with the 3V bus. In suspend mode, when one of the supply voltages is zero, there will be no current flow from the non zero supply towards the zero supply. $V_{CC1} \geq V_{CC2}$ (except in suspend mode).

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA to nB nB to nA	C_L = 50pF V_{CC1} = 5.0V V_{CC2} = 3.3V	 3.7 3.1	ns
C_I	Input capacitance		5	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1, 2	20	pF

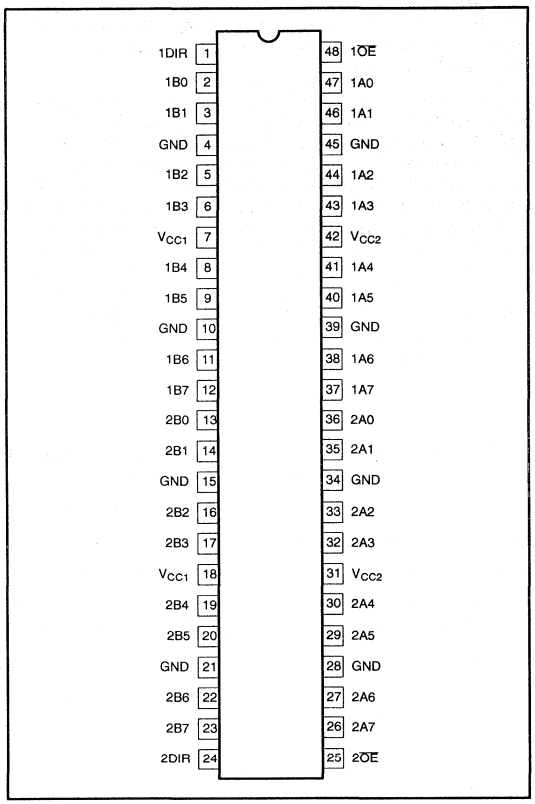
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC164245DL	48	SSOP48	Plastic	SSOP48/SOT370
74ALVC164245DGG	48	TSSOP48	Plastic	TSSOP48/SOT362

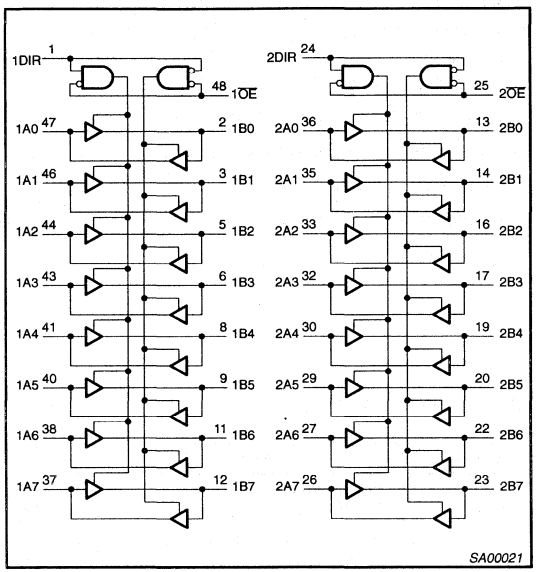
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	1DIR	'1' direction control
2, 3, 5, 6, 8, 9, 11, 12	1B0 to 1B7	1B data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	GND
7, 18	V_{CC1}	Positive supply voltage (5V bus)
13, 14, 16, 17, 19, 20, 22, 23	2B0 to 2B7	2B data inputs/outputs
24	2DIR	2B direction control
25	$2\overline{OE}$	'2' output enable input (active LOW)
26, 27, 29, 30, 32, 33, 35, 36	2A7 to 2A0	2A data inputs/outputs
31, 42	V_{CC2}	Positive supply voltage (3V bus)
37, 38, 40, 41, 43, 44, 46, 47	1A7 to 1A0	1A data inputs/outputs
48	$1\overline{OE}$	'1' output enable input (active LOW)

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS	
$n\overline{OE}$	nDIR	nAn	nBn
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

ALVC Netlists

ALVC SPICE MODELS

```
* ALVC.CIR
* 3 VOLT ADVANCED CMOS LOGIC
* STANDARD LOGIC PRODUCT GROUP
* PHILIPS SEMICONDUCTORS
* 4/11/95
*
* SIMULATION MODULES OF CMOS LOGIC PARTS OF PHILIPS ALVC FAMILY*
*                      BERKELEY SPICE FORMAT                   *
*--------------------------------------------------------------*
* IN ORDER TO SIMULATE A SPECIFIC ALVC DEVICE, GO TO THE END OF*
* FILE UNDER HEADING 'START RUNNING CIRCUIT MODEL' AND REMOVE  *
* THE COMMENT STATEMENT '*' BEFORE THE REQUIRED DEVICE.        *
* ALL OTHER DEVICES MUST HAVE AN '*' COMMENT STATEMENT.        *
* IF YOU LIKE TO SIMULATE WITH FAST OR SLOW PARAMETERS, GO TO  *
* HEADING 'PROCESS MODELS' AND REMOVE THE COMMENT STATEMENT '*'*
* BEFORE THE REQUIRED PROCESS MODEL.                           *
* YOU MAY ONLY SIMULATE ONE DEVICE AT THE TIME.                *
* THE LOAD CIRCUIT AND SIMULATION TIMING SHOULD NORMALLY BE    *
* ADAPTED TO YOUR SPECIFIC SITUATION.                          *
*--------------------------------------------------------------*

*****************************************************************
*                                                               *
* These ALVC models represent only one data input and one output *
* buffer of the device. Devices with a 3-state output buffer,   *
* have also an Output Enable (OE) input. Other control inputs   *
* such as DIR or CLK inputs are not modeled. Circuitry between  *
* the input and output buffers are also omitted, such as gates, *
* registers, latches, mux's and intermediate buffers. One result *
* of this is that ALVC models do not show the exact function of *
* the device. Another result of this is that propagation delays *
* in SPICE will not necessarily match with the published AC     *
* timing specifications in the device datasheet.                *
*                                                               *
*****************************************************************

.OPTIONS  ACCT   LIST  OPTS  ITL5=25000  NOMOD

**************  PROCESS MODELS ***************

* Nominal parameters
.INC c:\spice\alvc\lvcnomi.cir

* Fast parameters
*.INC c:\spice\alvc\lvcfast.cir

* Slow parameters
*.INC c:\spice\alvc\lvcslow.cir

******* START RUNNING CIRCUIT MODEL ********
*XALVC16240  5  2  4  1  0       INVERT3
*XALVC16241  5  2  4  1  0       INVERT3N
XALVC16244   5  2  4  1  0       INVERT3N
*XALVC16245  5  2  4  1  0       INVERT3N
*XALVC16373  5  2  4  1  0       INVERT3N
*XALVC16374  5  2  4  1  0       INVERT3N
*XALVC16540  5  2  4  1  0       INVERT3
*XALVC16541  5  2  4  1  0       INVERT3N
*XALVC16623  5  2  4  1  0       INVERT3N
*XALVC164245 5  2  4  1  0       INVERT3N
```

```
************ EXTERNAL TEST LOAD ************
R1     4    0    250
* Use this resistor only with a 3-state Output

*R1     4    0    500
C2      4    0    50P
*****************************************

VDD     1    0    DC  3.0
VIN1    2    0    PULSE  0  3.0  5N  2.5N  2.5N  40N 70N
VEN     5    0    DC  3.0
.TRAN  1.000n    70.000n  0         2.000n
.PROBE V(4)      V(2)
.PRINT TRAN    V(2)      V(4)
.END
```

LVCNOMI.CIR Subcircuit

```
* ALVC SUBCIRCUIT AND PRIMITIVE ELEMENTS LIBRARY
* LVCNOMI.CIR
* NOMINAL PROCESS CORNER
* STANDARD LOGIC PRODUCT GROUP
* PHILIPS SEMICONDUCTORS
* 4/11/95
************************************************
*          NOMINAL N-CHANNEL TRANSISTOR         *
*             UCB-3 PARAMETER SET               *
*                 24-JUNE-1993                  *
************************************************
.MODEL MNEN NMOS
+LEVEL = 3
+KP    = 114E-6
+VTO   = 0.57
+TOX   = 15E-9
+NSUB  = 7.8E16
+GAMMA = 0.70
+PHI   = 0.65
+VMAX  = 187E3
+RS    = 20
+RD    = 20
+XJ    = 0.26E-6
+LD    = 0.11E-6
+DELTA = 1.89
+THETA = 0.072
+ETA   = 0.043
+KAPPA = 0.0
+WD    = 0.0
* USE PARAMETER WD ONLY IN SPICE MODEL 3
* OTHERWISE MAKE FROM THAT LINE A COMMENT
************************************************
*         NOMINAL P-CHANNEL TRANSISTOR         *
*            UCB-3 PARAMETER SET               *
*                 24-JUNE-1993                  *
************************************************
.MODEL MPEN PMOS
+LEVEL = 3
+KP    = 43.7E-6
+VTO   = -0.67
+TOX   = 15.0E-9
+NSUB  = 6.0E16
+GAMMA = 0.84
+PHI   = 0.65
+VMAX  = 1.0E6
+RS    = 17.5
+RD    = 17.5
+XJ    = 0.30E-6
+LD    = 0.04E-6
+DELTA = 2.88
+THETA = 0.189
+ETA   = 0.091
+KAPPA = 0.0
+WD    = -0.03E-6
* USE PARAMETER WD ONLY IN SPICE MODEL 3
* OTHERWISE MAKE FROM THAT LINE A COMMENT
```

```
*********************************************
*       START OF SUBCIRCUIT DESCRIPTION     *
*                 SEPT. 1994                *
*********************************************

.SUBCKT LVCINPAN   2   3   50   60
* NOMINAL CASE PARAMETERS
* STANDARD LVC INPUT P-CH 150/0.8 N-CH 70/0.8 INCL. ESD STRUCTURE
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MN1 2 60 60 60 MNEN W=400U L=1.0U AD=7390P AS=208P PD=688U PS=420U
R1  4  2  100
MN2 4 60 60 60 MNEN W= 43U L=1.0U AD=176P AS=208P PD= 58U PS= 58U
MP1 3  4 50 50 MPEN W=150U L=0.8U AD=220P AS=400P PD=175U PS=175U
MN3 3  4 60 60 MNEN W= 70U L=0.8U AD= 80P AS=170P PD= 80U PS= 80U
MP2 5  3 50 50 MPEN W= 10U L=0.8U AD= 22P AS= 22P PD= 25U PS= 25U
MN4 5  3 60 60 MNEN W=  4U L=0.8U AD=  9P AS=  9P PD= 12U PS= 12U
MN5 3  5 60 60 MNEN W= 22U L=1.6U AD= 40P AS= 40P PD= 40U PS= 40U
.ENDS


.SUBCKT LVCINVAN   2   3   50   60
* NOMINAL CASE PARAMETERS
* INTERNAL INVERTER P-CH 30/0.8  N-CH 12/0.8
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 3  2 50 50 MPEN W= 30U L=0.8U AD=35P AS=35P PD=35U PS=30U
MN1 3  2 60 60 MNEN W= 12U L=0.8U AD=30P AS=30P PD=20U PS=15U
.ENDS

.SUBCKT LVCINV1N   2   3   50   60
* NOMINAL CASE PARAMETERS
* INTERNAL INVERTER P-CH 22/0.8  N-CH 16/0.8
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 3  2 50 50 MPEN W= 22U L=0.8U AD=50P AS=50P PD=50U PS=50U
MN1 3  2 60 60 MNEN W= 16U L=0.8U AD=25P AS=25P PD=25U PS=25U
.ENDS

.SUBCKT LVCINV2N   2   3   50   60
* FAST CASE PARAMETERS
* INTERNAL INVERTER P-CH 10/0.8  N-CH 4/0.8
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 3  2 50 50 MPEN W= 10U L=0.8U AD=15P AS=15P PD=15U PS=15U
MN1 3  2 60 60 MNEN W=  4U L=0.8U AD=10P AS=10P PD=10U PS=15U
.ENDS

.SUBCKT LVCNANDN  2   3   4   50   60
* NOMINAL CASE PARAMETERS
* INTERNAL NAND 2-INPUT P-CH 150/0.8  N-CH  180/0.8
* IN1 = 2,  IN2 = 3, OUT = 4,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 4  2  50 50 MPEN W=150U L=0.8U AD=200P AS=400P PD=100U PS=200U
MP2 4  3  50 50 MPEN W=150U L=0.8U AD=200P AS=400P PD=100U PS=200U
MN1 4  2   5 60 MNEN W=180U L=0.8U AD=400P AS=400P PD=400U PS=400U
MN2 5  3  60 60 MNEN W=180U L=0.8U AD=400P AS=400P PD=400U PS=400U
.ENDS
```

```
.SUBCKT LVCOUTAN    2   3   4   50   60
* NOMINAL CASE PARAMETERS
* 3-STATE OUTPUT MODULE
* OE = 2, IN = 3,  OUT = 4,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 5  2 50 50 MPEN W=100U L=0.8U AD=200P AS=400P PD=200U PS=200U
MP2 5  3 50 50 MPEN W=175U L=0.8U AD=225P AS=450P PD=225U PS=225U
MN1 5  3  6 60 MNEN W=100U L=0.8U AD=130P AS=130P PD=150U PS=130U
MN2 6  2 60 60 MNEN W=125U L=0.8U AD=175P AS=250P PD=175U PS=175U
MP3 15 2 50 50 MPEN W= 50U L=0.8U AD= 80P AS= 80P PD= 80U PS= 80U
MN3 15 2 60 60 MNEN W= 20U L=0.8U AD= 40P AS= 40P PD= 45U PS= 45U
MP4 7 15  8 50 MPEN W= 80U L=0.8U AD=250P AS=250P PD=250U PS=250U
MP5 8  3 50 50 MPEN W=100U L=0.8U AD=400P AS=400P PD=350U PS=350U
MN4 7 15 60 60 MNEN W= 75U L=0.8U AD=120P AS=160P PD=120U PS=120U
MN5 7  3 60 60 MNEN W= 60U L=0.8U AD= 80P AS=160P PD= 80U PS= 80U
R1  5 16 25
MP6 4 16 50 50 MPEN W=100U L=0.8U AD=125P AS=125P PD=125U PS=100U
R2 16  9 25
MP7 4  9 50 50 MPEN W=250U L=0.8U AD=250P AS=250P PD=275U PS=275U
R3  9 10 10
MP8 4 10 50 50 MPEN W=245U L=0.8U AD=250P AS=250P PD=275U PS=275U
R4 10 11 10
MP9 4 11 50 50 MPEN W=245U L=0.8U AD=250P AS=250P PD=275U PS=275U
R5  7 17 25
MN6 4 17 60 60 MNEN W= 65U L=0.8U AD= 75P AS= 75P PD=100U PS=100U
R6 17 12 10
MN7 4 12 60 60 MNEN W= 65U L=0.8U AD= 75P AS= 75P PD=100U PS=100U
R7 12 13 10
MN8 4 13 60 60 MNEN W= 50U L=0.8U AD= 50P AS= 50P PD=100U PS= 50U
R8 13 14 10
MN9 4 14 60 60 MNEN W= 50U L=0.8U AD= 50P AS= 50P PD=100U PS= 50U
.ENDS

.SUBCKT LVCOUT2N    5   4   50   60
* NOMINAL CASE PARAMETERS
* OUTPUT MODULE
* IN1 = 5, OUT = 4,  VCC = 50,  GND = 60
* 21-SEPTEMBER-1993
R1  5 16 25
MP6 4 16 50 50 MPEN W=250U L=0.8U AD=500P AS=500P PD=400U PS=250U
R2 16  9 25
MP7 4  9 50 50 MPEN W=375U L=0.8U AD=750P AS=750P PD=600U PS=375U
R3  9 10 10
MP8 4 10 50 50 MPEN W=375U L=0.8U AD=750P AS=750P PD=600U PS=375U
R4 10 11 10
MP9 4 11 50 50 MPEN W=375U L=0.8U AD=750P AS=750P PD=600U PS=375U
R5  5 17 25
MN6 4 17 60 60 MNEN W=175U L=0.8U AD=175P AS=175P PD=200U PS=175U
R6 17 12 10
MN7 4 12 60 60 MNEN W=175U L=0.8U AD=175P AS=175P PD=200U PS=175U
R7 12 13 10
MN8 4 13 60 60 MNEN W=450U L=0.8U AD=450P AS=450P PD=500U PS=450U
R8 13 14 10
MN9 4 14 60 60 MNEN W=450U L=0.8U AD=450P AS=450P PD=500U PS=450U
.ENDS
```

```
*******************************************************
*      START OF LVC CIRCUITS DESCRIPTION MODELS       *
*                    SEPT. 1994                       *
*******************************************************

.SUBCKT INVERT3  5  2  4  1  90
* INVERTING BUFFER TYPE; 3-STATE
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
* USE THIS MODEL FOR 74ALVC240 - 544
* OE = 5, IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1   20  30  50  60      LVCINPAN
XINV1  30  35  50  60      LVCINVAN
XINV2  35  36  50  60      LVCINV1N
XOUT    5  36  40  50  60  LVCOUTAN
L4     4   40   5.97NH
C4    40  90   1.5P
L3     2  20   5.97NH
C1    20  90   1.5P
L1     1  50   6.87NH
R1     1  50   0.1
L2    90  60   6.87NH
C2    50  90   1.5P
C3    60  90   1.5P
.ENDS

.SUBCKT INVERT3N  5  2  4  1  90
* NON-INVERTING BUFFER TYPE; 3-STATE
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
* USE THIS MODEL FOR 74ALVC241/244/245/373/374/541/623/4245
* OE = 5, IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1   20  30  50  60      LVCINPAN
XINV   30  35  50  60      LVCINVAN
XOUT    5  35  40  50  60  LVCOUTAN
L4     4  40   5.97NH
C4    40  90   1.5P
L3     2  20   5.97NH
C1    20  90   1.5P
L1     1  50   6.87NH
L2    90  60   6.87NH
C2    50  90   1.5P
C3    60  90   1.5P
.ENDS
```

```
.SUBCKT INVERT  2  4  1  90
* INVERTING BUFFER TYPE;
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
*
* IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1   20  30  50  60      LVCINPAN
XINV1  30  35  50  60      LVCINVAN
XINV2  35  36  50  60      LVCINV1N
XOUT   36  40  50  60      LVCOUT2N
L4     4   40   5.97NH
C4    40  90   1.5P
L3     2  20   5.97NH
C1    20  90   1.5P
L1     1  50   6.87NH
R1     1  50   0.1
L2    90  60   6.87NH
C2    50  90   1.5P
C3    60  90   1.5P
.ENDS

.SUBCKT INVERTN  2  4  1  90
* NON-INVERTING BUFFER TYPE;
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
*
* IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1   20  30  50  60      LVCINPAN
XINV   30  35  50  60      LVCINVAN
XOUT   35  40  50  60      LVCOUT2N
L4     4  40   5.97NH
C4    40  90   1.5P
L3     2  20   5.97NH
C1    20  90   1.5P
L1     1  50   6.87NH
L2    90  60   6.87NH
C2    50  90   1.5P
C3    60  90   1.5P
.ENDS

.SUBCKT NANDINVN  3  2  4  1  90
* NON-INVERTING 2-NAND BUFFER TYPE
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
*
* EN = 3, IN =2, OUT = 4, VCC = 1, GND = 90
* OCTOBER-1994
XIN1   20  25      50  60    LVCINPAN
XIN2   30  35      50  60    LVCINPAN
XNAND1 25  35  36  50  60    LVCNANDN
XOUT1  36  40      50  60    LVCOUT2N
L1      2  20   5.29NH
L2      3  30   4.28NH
L3     40   4   3.78NH
L4     1  50   6.08NH
R1      1  50   0.1
L5    60  90   6.08NH
R2     60  90   0.1
C1     20  90   1.5P
C2     30  90   1.5P
C3     40  90   1.5P
C4     50  90   1.5P
C5     60  90   1.5P
.ENDS
```

LVCFAST.CIR Subcircuit

```
* ALVC SUBCIRCUIT AND PRIMITIVE ELEMENTS LIBRARY
* LVCFAST.CIR
* FAST PROCESS CORNER
* STANDARD LOGIC PRODUCT GROUP
* PHILIPS SEMICONDUCTORS
* 4/11/95
************************************************
*          FAST N-CHANNEL TRANSISTOR           *
*            UCB-3 PARAMETER SET               *
*                24-JUNE-1993                  *
************************************************
.MODEL MNEF NMOS
+LEVEL = 3
+KP    = 134E-6
+VTO   = 0.46
+TOX   = 13.5E-9
+NSUB  = 8.9E16
+GAMMA = 0.54
+PHI   = 0.65
+VMAX  = 160E3
+RS    = 10
+RD    = 10
+XJ    = 0.31E-6
+LD    = 0.18E-6
+DELTA = 1.46
+THETA = 0.070
+ETA   = 0.025
+KAPPA = 0.0
+WD    = -0.05E-6
* USE PARAMETER WD ONLY IN SPICE MODEL 3
* OTHERWISE MAKE FROM THAT LINE A COMMENT
************************************************
*         FAST P-CHANNEL TRANSISTOR            *
*            UCB-3 PARAMETER SET               *
*                24-JUNE-1993                  *
************************************************
.MODEL MPEF PMOS
+LEVEL = 3
+KP    = 47.3E-6
+VTO   = -0.55
+TOX   = 13.5E-9
+NSUB  = 7.9E16
+GAMMA = 0.65
+PHI   = 0.65
+VMAX  = 1.0E6
+RS    = 10
+RD    = 10
+XJ    = 0.28E-6
+LD    = 0.11E-6
+DELTA = 4.80
+THETA = 0.189
+ETA   = 0.055
+KAPPA = 0.0
+WD    = -0.12E-6
* USE PARAMETER WD ONLY IN SPICE MODEL 3
* OTHERWISE MAKE FROM THAT LINE A COMMENT
```

```
*************************************************
*       START OF SUBCIRCUIT DESCRIPTION         *
*                  SEPT. 1994                   *
*************************************************

.SUBCKT LVCINPAF   2   3   50   60
* FAST CASE PARAMETERS
* STANDARD LVC INPUT P-CH 150/0.8 N-CH 70/0.8 INCL. ESD STRUCTURE
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MN1 2 60 60 60 MNEF W=400U L=1.0U AD=7390P AS=208P PD=688U PS=420U
R1  4  2  100
MN2 4 60 60 60 MNEF W= 43U L=1.0U AD=176P AS=208P PD= 58U PS= 58U
MP1 3  4 50 50 MPEF W=150U L=0.8U AD=220P AS=400P PD=175U PS=175U
MN3 3  4 60 60 MNEF W= 70U L=0.8U AD= 80P AS=170P PD= 80U PS= 80U
MP2 5  3 50 50 MPEF W= 10U L=0.8U AD= 22P AS= 22P PD= 25U PS= 25U
MN4 5  3 60 60 MNEF W=  4U L=0.8U AD=  9P AS=  9P PD= 12U PS= 12U
MN5 3  5 60 60 MNEF W= 22U L=1.6U AD= 40P AS= 40P PD= 40U PS= 40U
.ENDS


.SUBCKT LVCINVAF   2   3   50   60
* FAST CASE PARAMETERS
* INTERNAL INVERTER P-CH 30/0.8  N-CH 12/0.8
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 3  2 50 50 MPEF W= 30U L=0.8U AD=35P AS=35P PD=35U PS=30U
MN1 3  2 60 60 MNEF W= 12U L=0.8U AD=30P AS=30P PD=20U PS=15U
.ENDS


.SUBCKT LVCINV1F   2   3   50   60
* FAST CASE PARAMETERS
* INTERNAL INVERTER P-CH 22/0.8  N-CH 16/0.8
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 3  2 50 50 MPEF W= 22U L=0.8U AD=30P AS=30P PD=20U PS=15U
MN1 3  2 60 60 MNEF W= 16U L=0.8U AD=35P AS=35P PD=35U PS=30U
.ENDS

.SUBCKT LVCINV2F   2   3   50   60
* FAST CASE PARAMETERS
* INTERNAL INVERTER P-CH 10/0.8  N-CH 4/0.8
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 3  2 50 50 MPEN W= 10U L=0.8U AD=15P AS=15P PD=15U PS=15U
MN1 3  2 60 60 MNEN W=  4U L=0.8U AD=10P AS=10P PD=10U PS=15U
.ENDS

.SUBCKT LVCNANDF  2   3   4   50   60
* FAST CASE PARAMETERS
* INTERNAL NAND 2-INPUT P-CH 150/0.8  N-CH  180/0.8
* IN1 = 2,  IN2 = 3, OUT = 4,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 4  2  50 50 MPEF W=150U L=0.8U AD=200P AS=400P PD=100U PS=200U
MP2 4  3  50 50 MPEF W=150U L=0.8U AD=200P AS=400P PD=100U PS=200U
MN1 4  2   5 60 MNEF W=180U L=0.8U AD=400P AS=400P PD=400U PS=400U
MN2 5  3  60 60 MNEF W=180U L=0.8U AD=400P AS=400P PD=400U PS=400U
.ENDS
```

```
.SUBCKT LVCOUTAF    2   3   4   50   60
* FAST CASE PARAMETERS
* 3-STATE OUTPUT MODULE
* OE = 2, IN = 3,  OUT = 4,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 5   2 50 50 MPEF W=100U L=0.8U AD=200P AS=400P PD=200U PS=200U
MP2 5   3 50 50 MPEF W=175U L=0.8U AD=225P AS=450P PD=225U PS=225U
MN1 5   3  6 60 MNEF W=100U L=0.8U AD=130P AS=130P PD=150U PS=130U
MN2 6   2 60 60 MNEF W=125U L=0.8U AD=175P AS=250P PD=175U PS=175U
MP3 15  2 50 50 MPEF W= 50U L=0.8U AD= 80P AS= 80P PD= 80U PS= 80U
MN3 15  2 60 60 MNEF W= 20U L=0.8U AD= 40P AS= 40P PD= 45U PS= 45U
MP4 7  15  8 50 MPEF W= 80U L=0.8U AD=250P AS=250P PD=250U PS=250U
MP5 8   3 50 50 MPEF W=100U L=0.8U AD=400P AS=400P PD=350U PS=350U
MN4 7  15 60 60 MNEF W= 75U L=0.8U AD=120P AS=160P PD=120U PS=120U
MN5 7   3 60 60 MNEF W= 60U L=0.8U AD= 80P AS=160P PD= 80U PS= 80U
R1  5  16 25
MP6 4  16 50 50 MPEF W=100U L=0.8U AD=125P AS=125P PD=125U PS=100U
R2 16   9 25
MP7 4   9 50 50 MPEF W=250U L=0.8U AD=250P AS=250P PD=275U PS=275U
R3  9  10 10
MP8 4  10 50 50 MPEF W=245U L=0.8U AD=250P AS=250P PD=275U PS=275U
R4 10  11 10
MP9 4  11 50 50 MPEF W=245U L=0.8U AD=250P AS=250P PD=275U PS=275U
R5  7  17 25
MN6 4  17 60 60 MNEF W= 65U L=0.8U AD= 75P AS= 75P PD=100U PS=100U
R6 17  12 10
MN7 4  12 60 60 MNEF W= 65U L=0.8U AD= 75P AS= 75P PD=100U PS=100U
R7 12  13 10
MN8 4  13 60 60 MNEF W= 50U L=0.8U AD= 50P AS= 50P PD=100U PS= 50U
R8 13  14 10
MN9 4  14 60 60 MNEF W= 50U L=0.8U AD= 50P AS= 50P PD=100U PS= 50U
.ENDS

.SUBCKT LVCOUT2F    5   4   50   60
* FAST CASE PARAMETERS
* OUTPUT MODULE
* IN1 = 5, OUT = 4,  VCC = 50,  GND = 60
* 21-SEPTEMBER-1993
R1  5  16 25
MP6 4  16 50 50 MPEF W=250U L=0.8U AD=500P AS=500P PD=400U PS=250U
R2 16   9 25
MP7 4   9 50 50 MPEF W=375U L=0.8U AD=750P AS=750P PD=600U PS=375U
R3  9  10 10
MP8 4  10 50 50 MPEF W=375U L=0.8U AD=750P AS=750P PD=600U PS=375U
R4 10  11 10
MP9 4  11 50 50 MPEF W=375U L=0.8U AD=750P AS=750P PD=600U PS=375U
R5  5  17 25
MN6 4  17 60 60 MNEF W=175U L=0.8U AD=175P AS=175P PD=200U PS=175U
R6 17  12 10
MN7 4  12 60 60 MNEF W=175U L=0.8U AD=175P AS=175P PD=200U PS=175U
R7 12  13 10
MN8 4  13 60 60 MNEF W=450U L=0.8U AD=450P AS=450P PD=500U PS=450U
R8 13  14 10
MN9 4  14 60 60 MNEF W=450U L=0.8U AD=450P AS=450P PD=500U PS=450U
.ENDS
```

```
**********************************************************
*      START OF LVC CIRCUITS DESCRIPTION MODELS          *
*                    SEPT. 1994                          *
**********************************************************

.SUBCKT INVERT3  5  2  4  1  90
* INVERTING BUFFER TYPE; 3-STATE
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
* USE THIS MODEL FOR 74ALVC240 - 544
* OE = 5, IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1   20  30  50  60      LVCINPAF
XINV1  30  35  50  60      LVCINVAF
XINV2  35  36  50  60      LVCINV1F
XOUT    5  36  40  50  60  LVCOUTAF
L4     4   40   5.97NH
C4    40  90   1.5P
L3     2  20   5.97NH
C1    20  90   1.5P
L1     1  50   6.87NH
R1     1  50   0.1
L2    90  60   6.87NH
C2    50  90   1.5P
C3    60  90   1.5P
.ENDS

.SUBCKT INVERT3N  5  2  4  1  90
* NON-INVERTING BUFFER TYPE; 3-STATE
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
* USE THIS MODEL FOR 74ALVC241/244/245/373/374/541/623/4245
* OE = 5, IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1   20  30  50  60      LVCINPAF
XINV   30  35  50  60      LVCINVAF
XOUT    5  35  40  50  60  LVCOUTAF
L4     4  40   5.97NH
C4    40  90   1.5P
L3     2  20   5.97NH
C1    20  90   1.5P
L1     1  50   6.87NH
L2    90  60   6.87NH
C2    50  90   1.5P
C3    60  90   1.5P
.ENDS
```

```
.SUBCKT INVERT  2  4  1  90
* INVERTING BUFFER TYPE;
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
*
* IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1   20  30  50  60      LVCINPAF
XINV1  30  35  50  60      LVCINVAF
XINV2  35  36  50  60      LVCINV1F
XOUT   36  40  50  60      LVCOUT2F
L4     4   40   5.97NH
C4    40  90   1.5P
L3     2  20   5.97NH
C1    20  90   1.5P
L1     1  50   6.87NH
R1     1  50   0.1
L2    90  60   6.87NH
C2    50  90   1.5P
C3    60  90   1.5P
.ENDS

.SUBCKT INVERTN  2  4  1  90
* NON-INVERTING BUFFER TYPE;
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
*
* IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1   20  30  50  60      LVCINPAF
XINV   30  35  50  60      LVCINVAF
XOUT   35  40  50  60      LVCOUT2F
L4     4  40   5.97NH
C4    40  90   1.5P
L3     2  20   5.97NH
C1    20  90   1.5P
L1     1  50   6.87NH
L2    90  60   6.87NH
C2    50  90   1.5P
C3    60  90   1.5P
.ENDS

.SUBCKT NANDINVN  3  2  4  1  90
* NON-INVERTING 2-NAND BUFFER TYPE
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
*
* EN = 3, IN =2, OUT = 4, VCC = 1, GND = 90
* OCTOBER-1994
XIN1   20  25      50  60    LVCINPAF
XIN2   30  35      50  60    LVCINPAF
XNAND1 25  35  36  50  60    LVCNANDF
XOUT1  36  40      50  60    LVCOUT2F
L1      2  20   5.29NH
L2      3  30   4.28NH
L3     40   4   3.78NH
L4     1  50   6.08NH
R1      1  50   0.1
L5    60  90   6.08NH
R2     60  90   0.1
C1     20  90   1.5P
C2     30  90   1.5P
C3     40  90   1.5P
C4     50  90   1.5P
C5     60  90   1.5P
.ENDS
```

LVCSLOW.CIR Subcircuit

```
* ALVC SUBCIRCUIT AND PRIMITIVE ELEMENTS LIBRARY
* LVCSLOW.CIR
* SLOW PROCESS CORNER
* STANDARD LOGIC PRODUCT GROUP
* PHILIPS SEMICONDUCTORS
* 4/11/95
************************************************
*          SLOW N-CHANNEL TRANSISTOR           *
*            UCB-3 PARAMETER SET               *
*                24-JUNE-1993                  *
************************************************
.MODEL MNES NMOS
+LEVEL = 3
+KP    = 96E-6
+VTO   = 0.66
+TOX   = 16.5E-9
+NSUB  = 3.4E15
+GAMMA = 0.72
+PHI   = 0.65
+VMAX  = 199E3
+RS    = 30
+RD    = 30
+XJ    = 0.06E-6
+LD    = 0.04E-6
+DELTA = 1.79
+THETA = 0.075
+ETA   = 0.047
+KAPPA = 0.0
+WD    = 0.06E-6
* USE PARAMETER WD ONLY IN SPICE MODEL 3
* OTHERWISE MAKE FROM THAT LINE A COMMENT
************************************************
*         SLOW P-CHANNEL TRANSISTOR            *
*            UCB-3 PARAMETER SET               *
*                24-JUNE-1993                  *
************************************************
.MODEL MPES PMOS
+LEVEL = 3
+KP    = 38.4E-6
+VTO   = -0.75
+TOX   = 16.5E-9
+NSUB  = 2.0E17
+GAMMA = 0.81
+PHI   = 0.65
+VMAX  = 1.0E6
+RS    = 25
+RD    = 25
+XJ    = 0.15E-6
+LD    = 0.0
+DELTA = 3.15
+THETA = 0.190
+ETA   = 0.102
+KAPPA = 0.0
+WD    = 0.03E-6
* USE PARAMETER WD ONLY IN SPICE MODEL 3
* OTHERWISE MAKE FROM THAT LINE A COMMENT
```

```
*********************************************
*       START OF SUBCIRCUIT DESCRIPTION     *
*                  SEPT. 1994               *
*********************************************


.SUBCKT LVCINPAS   2   3   50   60
* SLOW CASE PARAMETERS
* STANDARD LVC INPUT P-CH 150/0.8 N-CH 70/0.8 INCL. ESD STRUCTURE
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MN1 2 60 60 60 MNES W=400U L=1.0U AD=7390P AS=208P PD=688U PS=420U
R1  4  2  100
MN2 4 60 60 60 MNES W= 43U L=1.0U AD=176P AS=208P PD= 58U PS= 58U
MP1 3  4 50 50 MPES W=150U L=0.8U AD=220P AS=400P PD=175U PS=175U
MN3 3  4 60 60 MNES W= 70U L=0.8U AD= 80P AS=170P PD= 80U PS= 80U
MP2 5  3 50 50 MPES W= 10U L=0.8U AD= 22P AS= 22P PD= 25U PS= 25U
MN4 5  3 60 60 MNES W=  4U L=0.8U AD=  9P AS=  9P PD= 12U PS= 12U
MN5 3  5 60 60 MNES W= 22U L=1.6U AD= 40P AS= 40P PD= 40U PS= 40U
.ENDS

.SUBCKT LVCINVAS   2   3   50   60
* SLOW CASE PARAMETERS
* INTERNAL INVERTER P-CH 30/0.8  N-CH 12/0.8
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 3  2 50 50 MPES W= 30U L=0.8U AD=35P AS=35P PD=35U PS=30U
MN1 3  2 60 60 MNES W= 12U L=0.8U AD=30P AS=30P PD=20U PS=15U
.ENDS

.SUBCKT LVCINV1S  2   3   50   60
* SLOW CASE PARAMETERS
* INTERNAL INVERTER P-CH 22/0.8  N-CH 16/0.8
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 3  2 50 50 MPES W= 22U L=0.8U AD=30P AS=30P PD=20U PS=15U
MN1 3  2 60 60 MNES W= 16U L=0.8U AD=35P AS=35P PD=35U PS=30U
.ENDS

.SUBCKT LVCINV2S   2   3   50   60
* FAST CASE PARAMETERS
* INTERNAL INVERTER P-CH 10/0.8  N-CH 4/0.8
* IN = 2,  OUT = 3,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 3  2 50 50 MPEN W= 10U L=0.8U AD=15P AS=15P PD=15U PS=15U
MN1 3  2 60 60 MNEN W=  4U L=0.8U AD=10P AS=10P PD=10U PS=15U
.ENDS

.SUBCKT LVCNANDS  2   3   7   4   50   60
* SLOW CASE PARAMETERS
* INTERNAL NAND 2-INPUT P-CH 150/0.8  N-CH  180/0.8
* IN1 = 2,  IN2 = 3, OUT = 4, VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 4  2  50 50 MPES W=150U L=0.8U AD=200P AS=400P PD=100U PS=200U
MP2 4  3  50 50 MPES W=150U L=0.8U AD=200P AS=400P PD=100U PS=200U
MN1 4  2   5 60 MNES W=180U L=0.8U AD=400P AS=400P PD=400U PS=400U
MN2 5  3  60 60 MNES W=180U L=0.8U AD=400P AS=400P PD=400U PS=400U
.ENDS
```

```
.SUBCKT LVCOUTAS    2   3   4   50   60
* NOMINAL CASE PARAMETERS
* 3-STATE OUTPUT MODULE
* OE = 2, IN = 3,  OUT = 4,  VCC = 50,  GND = 60
* SEPTEMBER-1994
MP1 5  2 50 50 MPES W=100U L=0.8U AD=200P AS=400P PD=200U PS=200U
MP2 5  3 50 50 MPES W=175U L=0.8U AD=225P AS=450P PD=225U PS=225U
MN1 5  3  6 60 MNES W=100U L=0.8U AD=130P AS=130P PD=150U PS=130U
MN2 6  2 60 60 MNES W=125U L=0.8U AD=175P AS=250P PD=175U PS=175U
MP3 15 2 50 50 MPES W= 50U L=0.8U AD= 80P AS= 80P PD= 80U PS= 80U
MN3 15 2 60 60 MNES W= 20U L=0.8U AD= 40P AS= 40P PD= 45U PS= 45U
MP4 7 15  8 50 MPES W= 80U L=0.8U AD=250P AS=250P PD=250U PS=250U
MP5 8  3 50 50 MPES W=100U L=0.8U AD=400P AS=400P PD=350U PS=350U
MN4 7 15 60 60 MNES W= 75U L=0.8U AD=120P AS=160P PD=120U PS=120U
MN5 7  3 60 60 MNES W= 60U L=0.8U AD= 80P AS=160P PD= 80U PS= 80U
R1  5 16 25
MP6 4 16 50 50 MPES W=100U L=0.8U AD=125P AS=125P PD=125U PS=100U
R2 16  9 25
MP7 4  9 50 50 MPES W=250U L=0.8U AD=250P AS=250P PD=275U PS=275U
R3  9 10 10
MP8 4 10 50 50 MPES W=245U L=0.8U AD=250P AS=250P PD=275U PS=275U
R4 10 11 10
MP9 4 11 50 50 MPES W=245U L=0.8U AD=250P AS=250P PD=275U PS=275U
R5  7 17 25
MN6 4 17 60 60 MNES W= 65U L=0.8U AD= 75P AS= 75P PD=100U PS=100U
R6 17 12 10
MN7 4 12 60 60 MNES W= 65U L=0.8U AD= 75P AS= 75P PD=100U PS=100U
R7 12 13 10
MN8 4 13 60 60 MNES W= 50U L=0.8U AD= 50P AS= 50P PD=100U PS= 50U
R8 13 14 10
MN9 4 14 60 60 MNES W= 50U L=0.8U AD= 50P AS= 50P PD=100U PS= 50U
.ENDS

.SUBCKT LVCOUT2S    5   4   50   60
* NOMINAL CASE PARAMETERS
* OUTPUT MODULE
* IN1 = 5, OUT = 4,  VCC = 50,  GND = 60
* 21-SEPTEMBER-1993
R1  5 16 25
MP6 4 16 50 50 MPES W=250U L=0.8U AD=500P AS=500P PD=400U PS=250U
R2 16  9 25
MP7 4  9 50 50 MPES W=375U L=0.8U AD=750P AS=750P PD=600U PS=375U
R3  9 10 10
MP8 4 10 50 50 MPES W=375U L=0.8U AD=750P AS=750P PD=600U PS=375U
R4 10 11 10
MP9 4 11 50 50 MPES W=375U L=0.8U AD=750P AS=750P PD=600U PS=375U
R5  5 17 25
MN6 4 17 60 60 MNES W=175U L=0.8U AD=175P AS=175P PD=200U PS=175U
R6 17 12 10
MN7 4 12 60 60 MNES W=175U L=0.8U AD=175P AS=175P PD=200U PS=175U
R7 12 13 10
MN8 4 13 60 60 MNES W=450U L=0.8U AD=450P AS=450P PD=500U PS=450U
R8 13 14 10
MN9 4 14 60 60 MNES W=450U L=0.8U AD=450P AS=450P PD=500U PS=450U
.ENDS
```

```
*******************************************************
*      START OF LVC CIRCUITS DESCRIPTION MODELS       *
*                    SEPT. 1994                       *
*******************************************************

.SUBCKT INVERT3  5  2  4  1  90
* INVERTING BUFFER TYPE; 3-STATE
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
* USE THIS MODEL FOR 74ALVC240 - 544
* OE = 5, IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1   20  30  50  60      LVCINPAS
XINV1  30  35  50  60      LVCINVAS
XINV2  35  36  50  60      LVCINV1S
XOUT    5  36  40  50  60  LVCOUTAS
L4     4   40   5.97NH
C4    40  90   1.5P
L3     2  20   5.97NH
C1    20  90   1.5P
L1     1  50   6.87NH
R1     1  50   0.1
L2    90  60   6.87NH
C2    50  90   1.5P
C3    60  90   1.5P
.ENDS

.SUBCKT INVERT3N  5  2  4  1  90
* NON-INVERTING BUFFER TYPE; 3-STATE
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
* USE THIS MODEL FOR 74ALVC241/244/245/373/374/541/623/4245
* OE = 5, IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1   20  30  50  60      LVCINPAS
XINV   30  35  50  60      LVCINVAS
XOUT    5  35  40  50  60  LVCOUTAS
L4     4  40   5.97NH
C4    40  90   1.5P
L3     2  20   5.97NH
C1    20  90   1.5P
L1     1  50   6.87NH
L2    90  60   6.87NH
C2    50  90   1.5P
C3    60  90   1.5P
.ENDS
```

```
.SUBCKT INVERT  2  4  1  90
* INVERTING BUFFER TYPE;
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
*
* IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1   20  30  50  60      LVCINPAS
XINV1  30  35  50  60      LVCINVAS
XINV2  35  36  50  60      LVCINV1S
XOUT   36  40  50  60      LVCOUT2S
L4     4   40   5.97NH
C4    40  90   1.5P
L3     2  20   5.97NH
C1    20  90   1.5P
L1     1  50   6.87NH
R1     1  50   0.1
L2    90  60   6.87NH
C2    50  90   1.5P
C3    60  90   1.5P
.ENDS

.SUBCKT INVERTN  2  4  1  90
* NON-INVERTING BUFFER TYPE;
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
*
* IN = 2,  OUT = 4,  VCC = 1,  GND = 90
* OCTOBER-1994
XIN1   20  30  50  60      LVCINPAS
XINV   30  35  50  60      LVCINVAS
XOUT1  35  40  50  60      LVCOUT2S
L4     4  40   5.97NH
C4    40  90   1.5P
L3     2  20   5.97NH
C1    20  90   1.5P
L1     1  50   6.87NH
L2    90  60   6.87NH
C2    50  90   1.5P
C3    60  90   1.5P
.ENDS

.SUBCKT NANDINVN  3  2  4  1  90
* NON-INVERTING 2-NAND BUFFER TYPE
* EQUIVALENT REFERENCE SIMULATION MODEL NOMINAL CASE
*
* EN = 3, IN =2, OUT = 4, VCC = 1, GND = 90
* OCTOBER-1994
XIN1   20  25      50  60    LVCINPAS
XIN2   30  35      50  60    LVCINPAS
XNAND1 25  35  36  50  60    LVCNANDS
XOUT1  36  40      50  60    LVCOUT2S
L1      2  20   5.29NH
L2      3  30   4.28NH
L3     40   4   3.78NH
L4     1  50   6.08NH
R1      1  50   0.1
L5    60  90   6.08NH
R2     60  90   0.1
C1     20  90   1.5P
C2     30  90   1.5P
C3     40  90   1.5P
C4     50  90   1.5P
C5     60  90   1.5P
.ENDS
```

Section 9
LV

SPICE

CONTENTS

Each LV device requires some combination of one or two input stages, an output stage, possibly one or two inverting stages, possibly a NAND stage, and some package parasitics. Switch part types have an input stage, possibly a level converter, and an analog switch. Table 9-1 shows LV model combinations that correlate the various subcircuit structures for each part type. Dashes indicate that a particular stage is not needed.

Table 9-1. LV Model Combinations

LV	Input Circuit	Inverter Circuit	NAND Circuit	Output Circuit	Level Converter	Analog Switch	Subcircuit Name
00	INP2	INV	–	OUTP	–	–	INV2
04	INP0	–	–	OUTP	–	–	INV0
14	SMT1	INV	–	OUTP	–	–	INVSMT
32	INP1	INV/INV	–	OUTP	–	–	NINV1
74	INP1	INV	–	OUTP	–	–	INV1
123	INP1	INV	–	OUTP	–	–	INV1
132	INP1	INV	–	OUTP	–	–	INV1
138	INP2/INP2	–	NAND	OUTP	–	–	NANDINV
161	INP2	INV	–	OUTP	–	–	INV2
163	INP2	INV	–	OUTP	–	–	INV2
244	INP2	INV	–	BUSOUTP	–	–	NINV3
245	INP2	INV	–	BUSOUTP	–	–	NINV3
273	INP1	INV/INV		OUTP	–	–	NINV1
373	INP2	INV	–	BUSOUTP	–	–	NINV3
374	INP2	INV	–	BUSOUTP	–	–	NINV3
595	INP2	INV	–	BUSOUTP	–	–	NINV3
4040	INP1	INV/INV	–	OUTP	–	–	NINV1
4051	INP2	–	–	–	LLC	SWITCH1	SWI1
4052	INP2	–	–	–	LLC	SWITCH1	SWI1
4053	INP2	–	–	–	LLC	SWITCH1	SWI1
4066	INP2	–	–	–	–	SWITCH2	SWI2
4316	INP1	–	–	–	LLC	SWITCH3	SWI3
4538	INP1	INV	–	OUTP	–	–	INV1

The data sheet section provides information on the part types if needed. Each data sheet contains a part description, part features, quick reference data, ordering information, pin configuration, logic symbol, and function table.

To do simulations on a particular part type, refer to the LV Netlists section of the book. That section contains a file called "LV.CIR" that contains simulation test circuits for individual device types. The file is also in the LV directory in the attached diskette, and it is written in the Berkeley SPICE format only. Figures 9-1 through 9-7 show examples of how the test circuits are assembled.

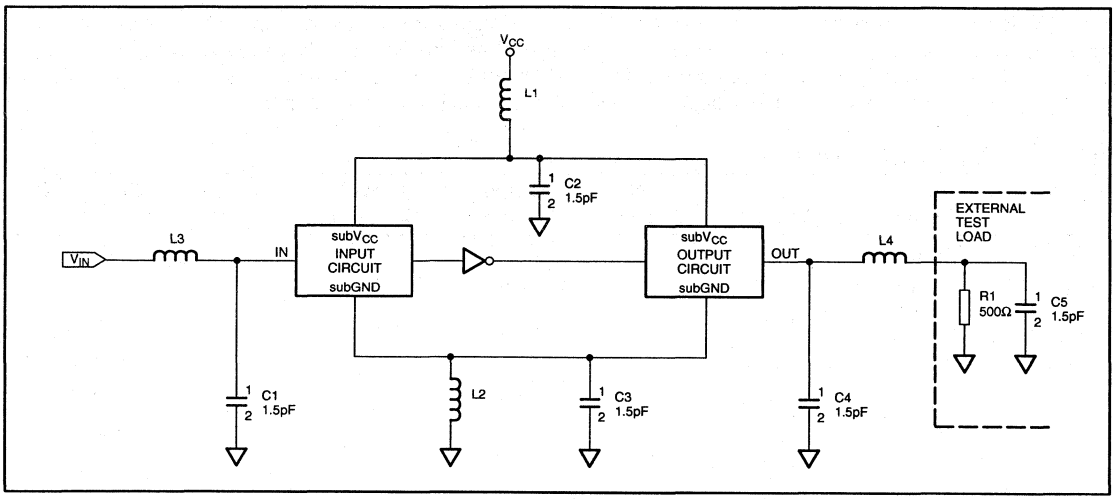


Figure 9-1. Test Circuit for LV00/14/74/123/132/161/163/4538

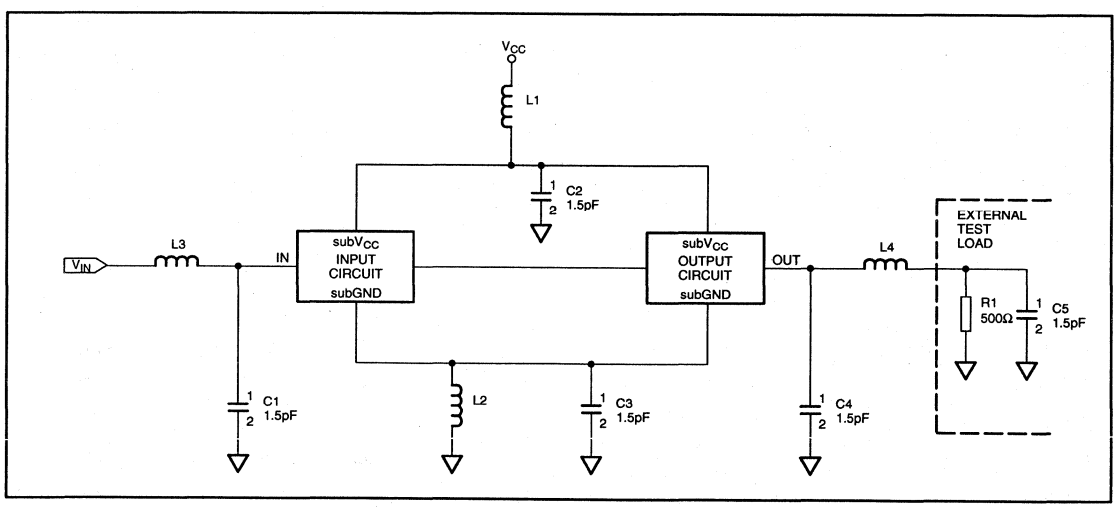


Figure 9-2. Test Circuit for LV04

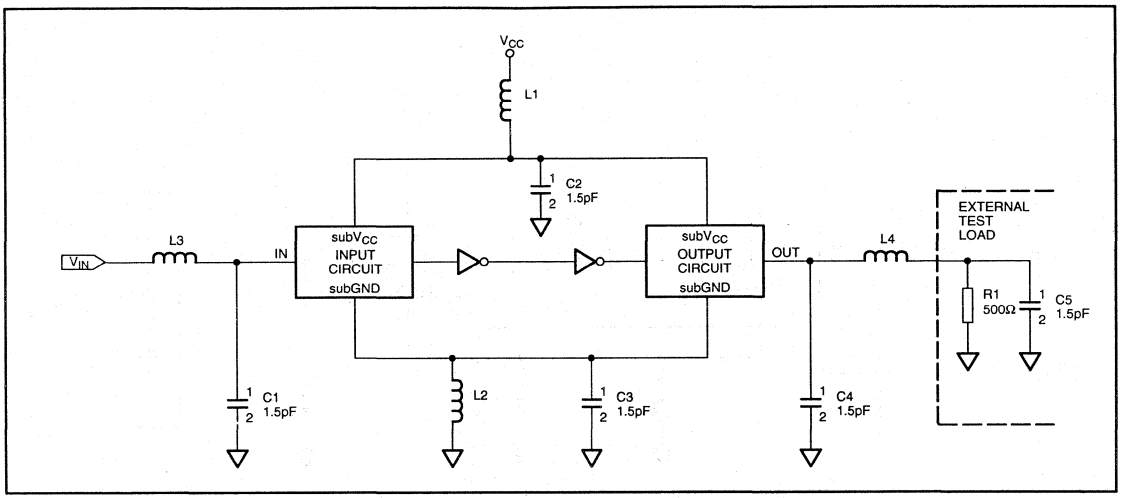


Figure 9-3. Test Circuit for LV32/273/4040

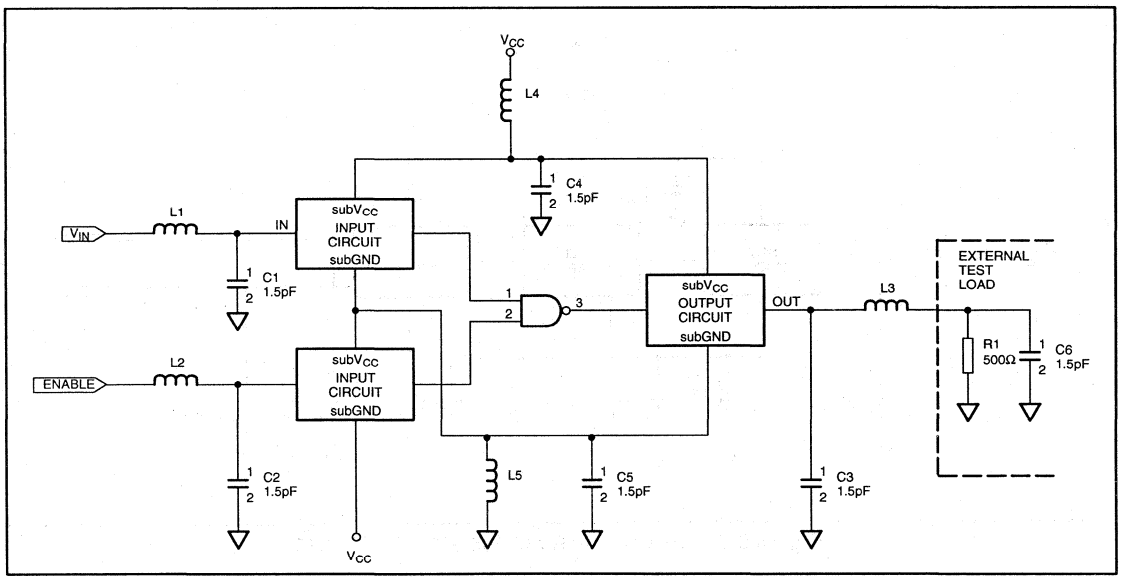


Figure 9-4. Test Circuit for LV138

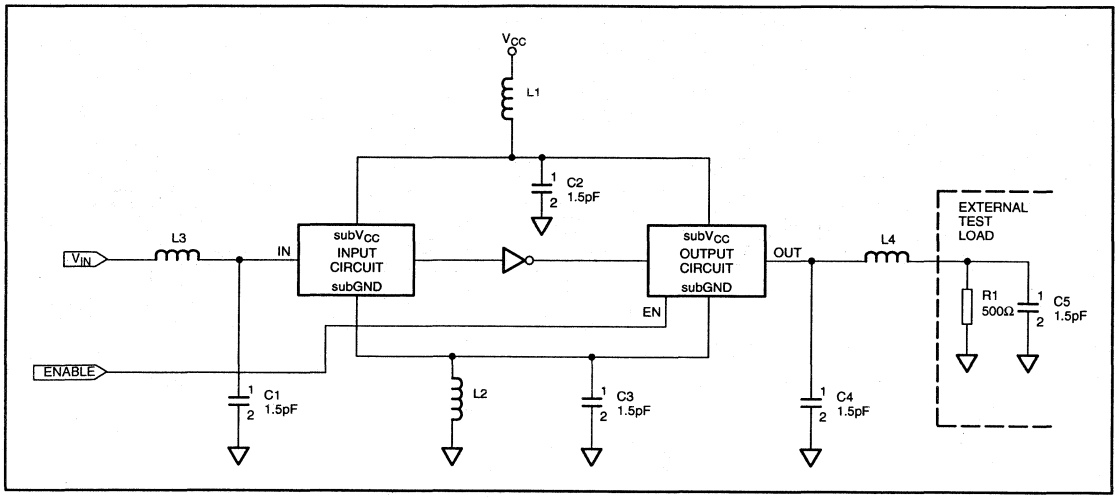


Figure 9-5. Test Circuit for LV244/245/373/374/595

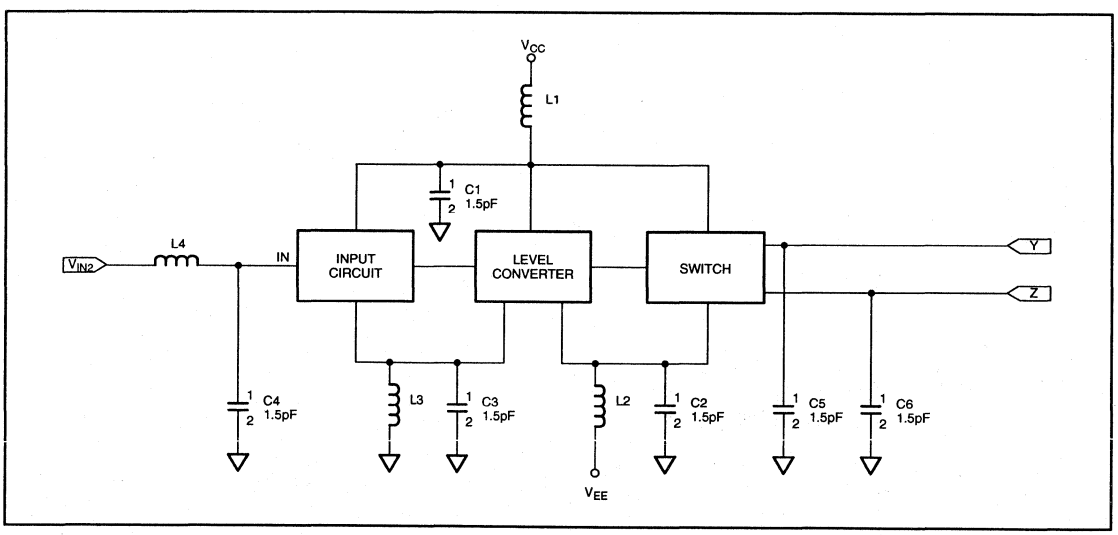


Figure 9-6. Test Circuit for LV4051/4052/4053/4316

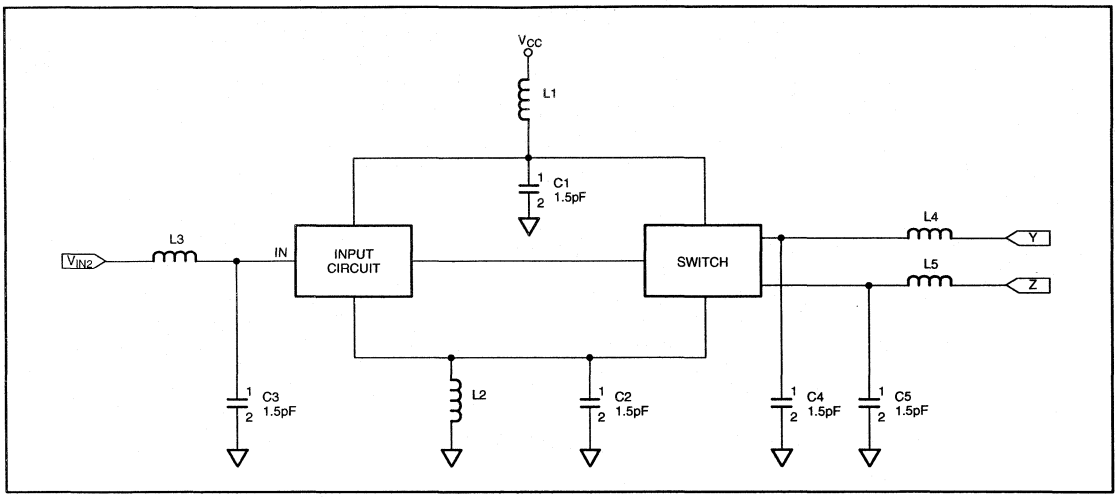


Figure 9-7. Test Circuit for LV4066

Also in the LV Netlists section of the book and in the LV directory of the diskette are files for subcircuits and primitive elements, such as transistors, diodes, and resistors. These files are called LVXXXX.CIR, the "XXXX" standing for NOMI, FAST, and SLOW, representing the nominal, fast, and slow process corners. The files contain the subcircuit elements, and they also have package parasitics connected to simulate a device in a package. Package parasitic values can be changed to suit the application. See the Packaging section of the book for values.

For clarification, the following illustration shows how the two programs interact with each other:

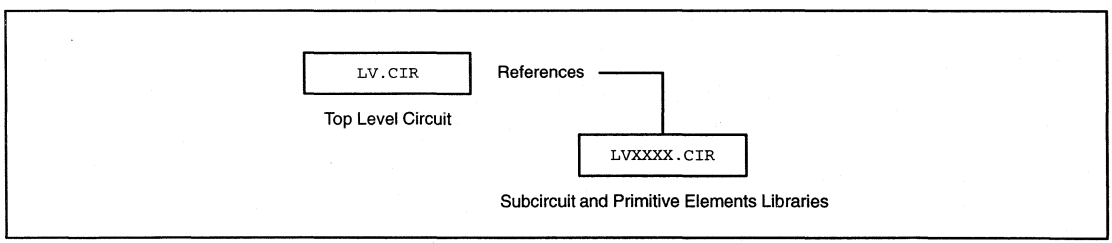


Figure 9-8. LV SPICE Program Hierarchy

The top level program, LV.CIR, uses an AC test set-up with a 3V square wave input, 5ns delay, 2.5ns rise and fall times, 30ns pulse width, 100ns period, 3V V_{CC}, 0V applied to the output enable, and a 1kΩ, 50pF load. These conditions may be modified to suit the application. Pay particular attention to the commented commands in the program when changing simulations from logic devices to the analog switches. Some of the previous commands for the logic devices will have to be commented out. Also, the ".INC" command that specifies the path to reference the other program should be modified to reflect your disk directory structure.

LV Short-form Datasheets

Quad 2-input NAND gate — 74LV00

FEATURES

- Optimized for Low Voltage applications: 1.0V to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (V_{OH} undershoot) > 2V at V_{CC} = 3.3V, T_{amb} = 25°C
- Output capability: standard
- I_{CC} category: SSI

DESCRIPTION

The 74LV00 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT00.

The 74LV00 provides the 2-input NAND function.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL} t_{PLH}	Propagation delay nA, nB to nY	C_L = 15pF; V_{CC} = 3.3V	7	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1, 2	22	pF

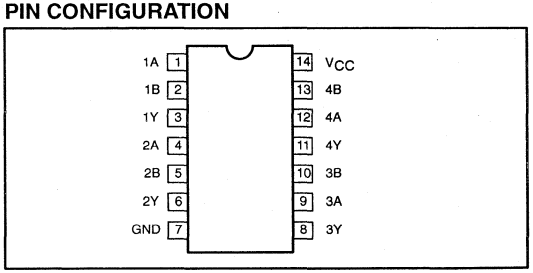
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV00N	14	DIL	Plastic	DIL14/SOT27
74LV00D	14	SO	Plastic	SO14/SOT108A
74LV00DB	14	SSOP	Plastic	SSOP14/SOT337
74LV00PW	14	TSSOP	Plastic	TSSOP14/SOT402

PIN CONFIGURATION

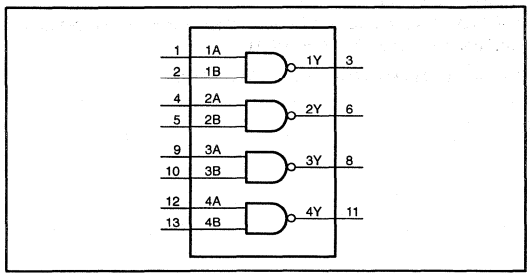


PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A – 4A	Data inputs
2, 5, 10, 13	1B – 4B	Data inputs
3, 6, 8, 11	1Y – 4Y	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

Quad 2-input NAND gate 74LV00

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

Hex inverter | 74LV04

FEATURES

- Optimized for Low Voltage applications: 1.0V to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V at V_{CC} = 3.3V, T_{amb} = 25°C
- Output capability: standard
- I_{CC} category: SSI

DESCRIPTION

The 74LV04 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT04.

The 74LV04 provides the 2-input NAND function.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL} t_{PLH}	Propagation delay nA to nY	C_L = 15pF; V_{CC} = 3.3V	6	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1, 2	21	pF

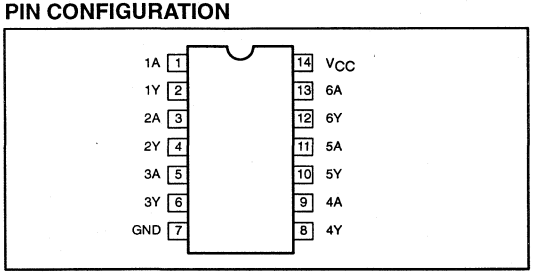
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV04N	14	DIL	Plastic	DIL14/SOT27
74LV04D	14	SO	Plastic	SO14/SOT108A
74LV04DB	14	SSOP	Plastic	SSOP14/SOT337
74LV04PW	14	TSSOP	Plastic	TSSOP14/SOT402

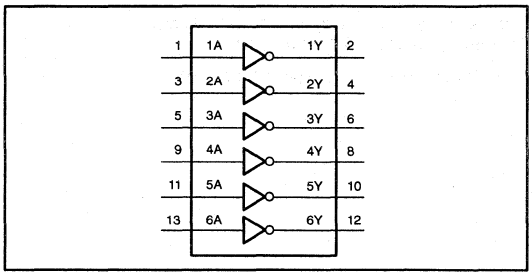
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A – 6A	Data inputs
2, 4, 6, 8, 10, 12	1Y – 6Y	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUT	OUTPUT
nA	**nY**
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

Hex inverting Schmitt-trigger | 74LV14

FEATURES

- Optimized for Low Voltage applications: 1.0V to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V at V_{CC} = 3.3V, T_{amb} = 25°C
- Output capability: standard
- I_{CC} category: SSI

APPLICATIONS

- Wave and pulse shapers for highly noisy environments

DESCRIPTION

The 74LV14 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT14.

The 74LV14 provides six inverting buffers with Schmitt-trigger action. It is capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL} t_{PLH}	Propagation delay nA to nY	C_L = 15pF; V_{CC} = 3.3V	13	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1, 2	15	pF

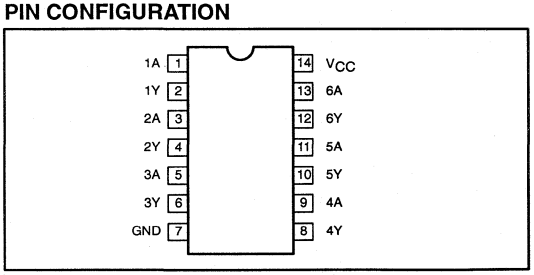
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV14N	14	DIL	Plastic	DIL14/SOT27
74LV14D	14	SO	Plastic	SO14/SOT108A
74LV14DB	14	SSOP	Plastic	SSOP14/SOT337
74LV14PW	14	TSSOP	Plastic	TSSOP14/SOT402

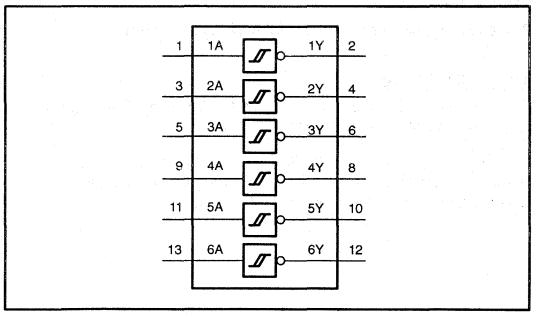
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A – 6A	Data inputs
2, 4, 6, 8, 10, 12	1Y – 6Y	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

Quad 2-input OR gate | 74LV32

FEATURES

- Optimized for Low Voltage applications: 1.0V to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V at V_{CC} = 3.3V, T_{amb} = 25°C
- Output capability: standard
- I_{CC} category: SSI

DESCRIPTION

The 74LV32 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT32.

The 74LV32 provides the 2-input OR function.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL} t_{PLH}	Propagation delay nA, nB to nY	C_L = 15pF; V_{CC} = 3.3V	6	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1, 2	16	pF

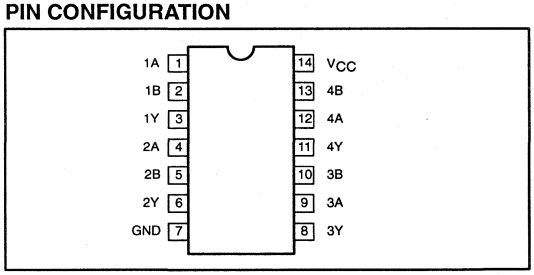
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV32N	14	DIL	Plastic	DIL14/SOT27
74LV32D	14	SO	Plastic	SO14/SOT108A
74LV32DB	14	SSOP	Plastic	SSOP14/SOT337
74LV32PW	14	TSSOP	Plastic	TSSOP14/SOT402

PIN CONFIGURATION

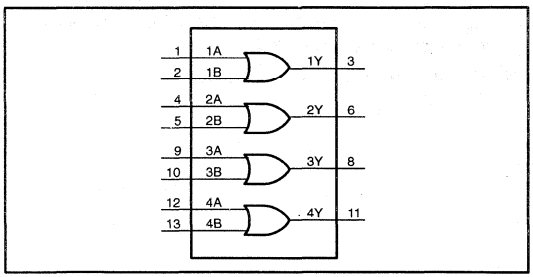


PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A – 4A	Data inputs
2, 5, 10, 13	1B – 4B	Data inputs
3, 6, 8, 11	1Y – 4Y	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

Quad 2-input OR gate 74LV32

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH voltage level
L = LOW voltage level

Dual D-type flip-flop with set and reset; positive-edge trigger

74LV74

FEATURES

- Optimized for Low Voltage applications: 1.0V to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V at V_{CC} = 3.3V, T_{amb} = 25°C
- Output capability: standard
- I_{CC} category: flip-flops

DESCRIPTION

The 74LV74 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT74.

The 74LV74 is a dual positive edge triggered, D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set ($\overline{S}_D$) and ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nCP to nQ, n$\overline{Q}$ n$\overline{S}_D$ to nQ, n$\overline{Q}$ n$\overline{R}_D$ to nQ, n$\overline{Q}$	C_L = 15pF V_{CC} = 3.3V	 11 14 14	ns
f_{max}	Maximum clock frequency		76	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1, 2	24	pF

NOTES:

C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; C_L = output load capacity in pF;
f_o = output frequency in MHz; V_{CC} = supply voltage in V;
$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
The condition is V_I = GND to V_{CC}.

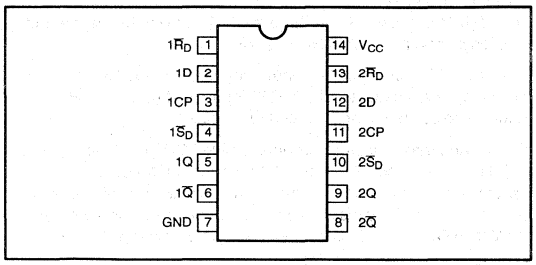
ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV74N	14	DIL	PLASTIC	DIL14/SOT27
74LV74D	14	SO	PLASTIC	SO14/SOT108A
74LV74DB	14	SSOP	PLASTIC	SSOP14/SOT337
74LV74PW	14	TSSOP	PLASTIC	TSSOP14/SOT402

Dual D-type flip-flop with set and reset; positive-edge trigger

74LV74

PIN CONFIGURATION

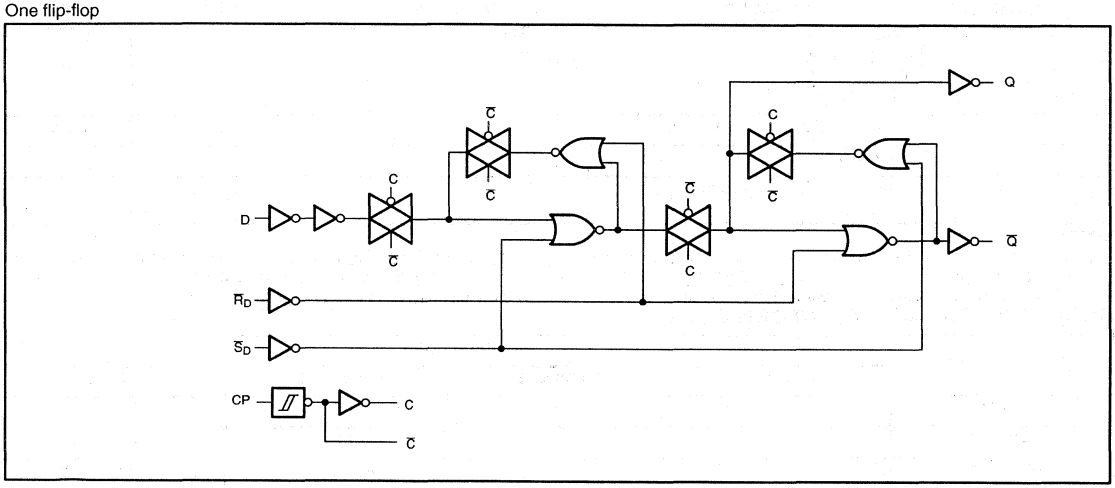


PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 13	1$\overline{R}_D$, 2$\overline{R}_D$	Asynchronous reset-direct input (active LOW)
2, 12	1D, 2D	Data inputs
3, 11	1CP, 2CP	Clock input (LOW-to-HIGH, edge-triggered)
4, 10	1$\overline{S}_D$, 2$\overline{S}_D$	Asynchronous set-direct input (active LOW)
5, 9	1Q, 2Q	True flip-flop outputs
6, 8	1$\overline{Q}$, 2$\overline{Q}$	Complement flip-flop outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC DIAGRAM

One flip-flop



FUNCTION TABLES

INPUTS				OUTPUTS	
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

INPUTS				OUTPUTS	
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH CP transition
Q_{n+1} = State after the next LOW-to-HIGH CP transition

Dual retriggerable monostable multivibrator with reset

74LV123

FEATURES

- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V @ V_{CC} = 3.3V, T_{amb} = 25°C
- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100% duty factor
- Direct reset terminates output pulses
- Schmitt-trigger action on all inputs except for the reset input
- Output capability: standard (except for nR_{EXT}/C_{EXT})
- I_{CC} category: MSI

DESCRIPTION

The 74LV123 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC/HCT123.

The 74LV123 is a dual retriggerable monostable multivibrator with output pulse width control by three methods. The basic pulse time is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}). Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ($n\overline{A}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period (nQ = HIGH, $n\overline{Q}$ = LOW) can be made as long as desired. Alternatively, an output delay can be terminated at any time by a LOW-going edge on input $n\overline{R}_D$, which also inhibits the triggering. An internal connection from $n\overline{R}_D$ to the input gates makes it possible to trigger the circuit by a positive-going signal at input $n\overline{R}_D$. The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT}.

When C_{EXT} > 10,000pF, the typical output pulse width is defined as: $t_W = 0.45 \times R_{EXT} \times C_{EXT}$ (typ.), where t_W = pulse width in ns; R_{EXT} = external resistor in KΩ; and C_{EXT} = external capacitor in pF. Schmitt-trigger action in the $n\overline{A}$ and nB inputs makes the circuit highly tolerant of slower input rise and fall times.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay $n\overline{A}$, nB to nQ, $n\overline{Q}$ $n\overline{R}_D$ to nQ, $n\overline{Q}$	C_L = 15pF V_{CC} = 3.3V R_{EXT} = 5KΩ C_{EXT} = 0pF	 16 13	 ns ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per flip-flop	V_{CC} = 3.3V Notes 1, 2	17	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

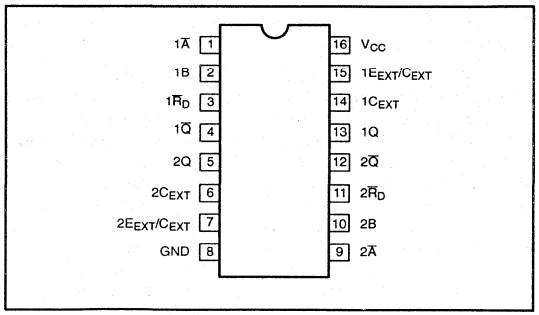
ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV123N	16	DIL	Plastic	DIL16/SOT38Z
74LV123D	16	SO	Plastic	SO16/SOT109A
74LV123DB	16	SSOP	Plastic	SOP16/SOT338
74LV123PW	16	TSSOP	Plastic	TSSOP16/SOT403

Dual retriggerable monostable multivibrator with reset

74LV123

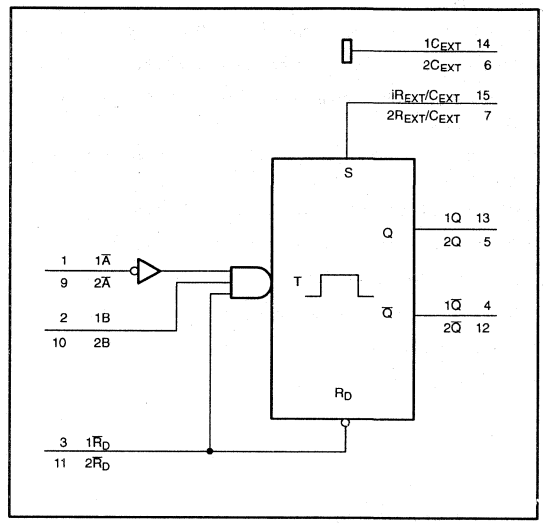
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1,9	1$\overline{A}$, 2$\overline{A}$	Trigger inputs (negative-edge triggered)
2,10	1B, 2B	Trigger inputs (positive-edge triggered)
3,11	1$\overline{R}_D$, 2$\overline{R}_D$	Direct reset LOW and trigger action at positive edge
4, 12	1$\overline{Q}$, 2$\overline{Q}$	Outputs (active LOW)
7	2R_{EXT}/C_{EXT}	External resistor/capacitor connection
8	GND	Ground (0V)
13, 5	1Q, 2Q	Outputs (active HIGH)
14, 6	1C_{EXT}, 2C_{EXT}	External capacitor connection
15	1R_{EXT}/C_{EXT}	External resistor/capacitor connection
16	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUTS			OUTPUTS	
n$\overline{R}_D$	n$\overline{A}$	nB	nQ	n$\overline{Q}$
L	X	X	L	H
X	H	X	L *	H *
X	X	L	L *	H *
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
⎍ = one HIGH level output pulse
⎍ = one LOW level output pulse

Quad 2-input NAND Schmitt trigger 74LV132

FEATURES

- Optimized for Low Voltage applications: 1.0V to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V at V_{CC} = 3.3V, T_{amb} = 25°C
- Output capability: standard
- I_{CC} category: SSI

APPLICATIONS

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators

GENERAL DESCRIPTION

The 74LV132 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT132.

The 74LV132 contain four 2-input NAND gates which accept standard input signals. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

The gate switches at different points for positive and negative-going signals. The difference between the positive voltage V_{T+} and the negative voltage V_{T-} is defined as the hysteresis voltage V_H.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.5ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/ t_{PLH}	Propagation delay nA, nB to nY	C_L = 15pF; V_{CC} = 3.3V	10	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1 and 2	24	pF

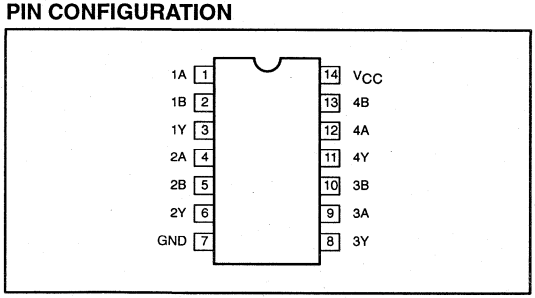
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV132N	14	DIL	Plastic	DIL14/SOT27
74LV132D	14	SO	Plastic	SO14/SOT108A
74LV132DB	14	SSOP	Plastic	SSOP14/SOT337
74LV132PW	14	TSSOP	Plastic	TSSOP14/SOT402

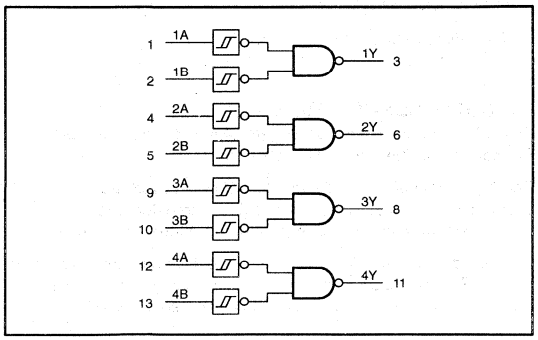
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data inputs
2, 5, 10, 13	1B to 4B	Data inputs
3, 6, 8, 11	1Y to 4Y	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

3-to-8 line decoder/demultiplexer; inverting | 74LV138

FEATURES

- Optimized for Low Voltage applications: 1.0V to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V at V_{CC} = 3.3V, T_{amb} = 25°C
- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV138 is a low-voltage, low-power, high-performance Si-gate CMOS device and is pin and function compatible with 74HC/HCT138.

The 74LV138 accepts three binary weighted address inputs (A_0, A_1, A_2) and when enabled, provide 8 mutually exclusive active LOW outputs ($\overline{Y}_0$ to $\overline{Y}_7$).

The 74LV138 features three enable inputs: two active LOW ($\overline{E}_1$ and $\overline{E}_2$ and one active HIGH (E_3). Every output will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH.

This multiple enable function allows easy parallel expansion of the 74LV138 to a 1-of-32 (5 lines to 32 lines) decoder with just four 74LV138 ICs and one inverter. The 74LV138 can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

The 74LV138 is identical to the 74LV238 but has non-inverting (true) outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL} t_{PLH}	Propagation delay An to $\overline{Y}$n; E3 to $\overline{Y}$n, $\overline{E}$n to $\overline{Y}$n	C_L = 15pF; V_{CC} = 3.3V	12 14	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per package	V_{CC} = 3.3V Notes 1, 2	45	pF

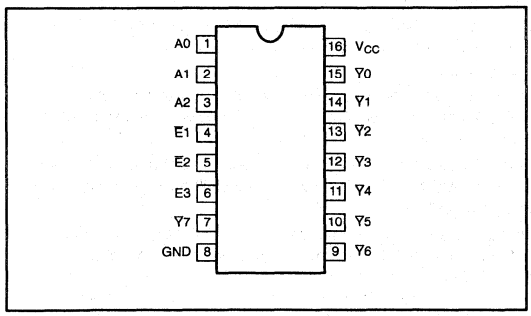
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

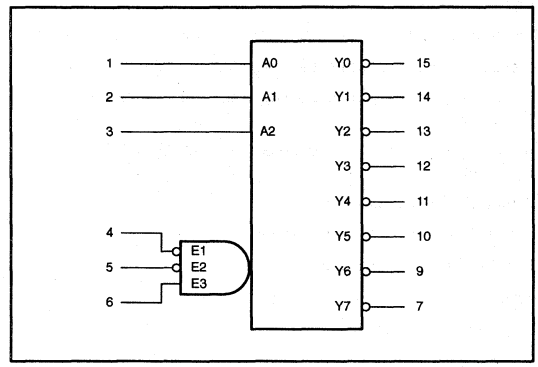
ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV138N	14	DIL	Plastic	DIL14/SOT27
74LV138D	14	SO	Plastic	SO14/SOT108A
74LV138DB	14	SSOP	Plastic	SSOP14/SOT337
74LV138PW	14	TSSOP	Plastic	TSSOP14/SOT402

PIN CONFIGURATION



LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 3	A0 – A2	Address inputs
4, 5	$\overline{E1}$ – $\overline{E2}$	Enable inputs (active LOW)
6	E3	Enable inputs (active HIGH)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y0}$ – $\overline{Y7}$	Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive power supply

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E1}$	$\overline{E2}$	E3	A0	A1	A2	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	Y6	$\overline{Y7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

Presettable synchronous 4-bit binary counter; asynchronous reset

74LV161

FEATURES

- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC} 3.3V, T_{amb} = 25°C
- Typcial V_{OHV} (output V_{OH} undershoot) > 2V at V_{CC} = 3.3V, T_{amb} = 25°C
- Asynchronous reset
- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV161 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT161.

The 74LV161 is a synchronous presettable binary counter which features an internal look-ahead carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP). The outputs (Q0 to Q3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D0 to D3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET). A low level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q0 to Q3) to LOW level regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q0. This pulse can be used to enable the next cascaded stage. The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{MAX} = \frac{1}{t_{P(MAX)}\ (\text{CP to TC}) + t_{SU}\ (\text{CEP to CP})}$$

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Qn CP to TC $\overline{MR}$ to Qn $\overline{MR}$ to TC CET to TC	C_L = 15pF; V_{CC} = 3.3V	 15 18 15 17 9	 ns ns ns ns ns
f_{MAX}	Maximum clock frequency		77	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1 and 2	25	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\ (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; f_o = output frequency in MHz
   C_L = output load capacitance in pF; V_{CC} = supply voltage in V
   $\Sigma\ (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

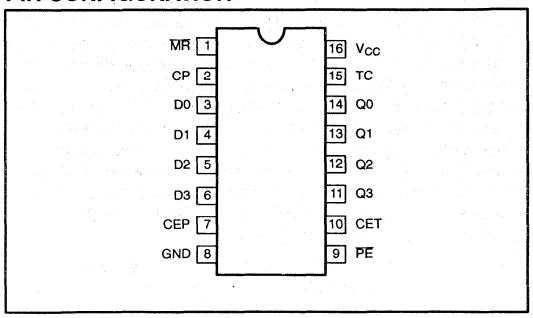
ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV161N	16	DIL	Plastic	DIL16/SOT38-1
74LV161D	16	SO	Plastic	SO16/SOT109-1
74LV161DB	16	SSOP	Plastic	SSOP16/SOT338-1
74LV161PW	16	TSSOP	Plastic	TSSOP16/SOT403-1

Presettable synchronous 4-bit binary counter; asynchronous reset

74LV161

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	Asynchronous master reset (active LOW)
2	CP	Clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	D0 to D3	Data inputs
7	CEP	Count enable input
8	GND	Ground (0V)
9	$\overline{PE}$	Parallel enable input (active LOW)
10	CET	Count enable carry input
14, 13, 12, 11	Q0 to Q3	Flip-flop outputs
15	TC	Terminal count output
16	V_{CC}	Positive supply voltage

FUNCTION TABLE

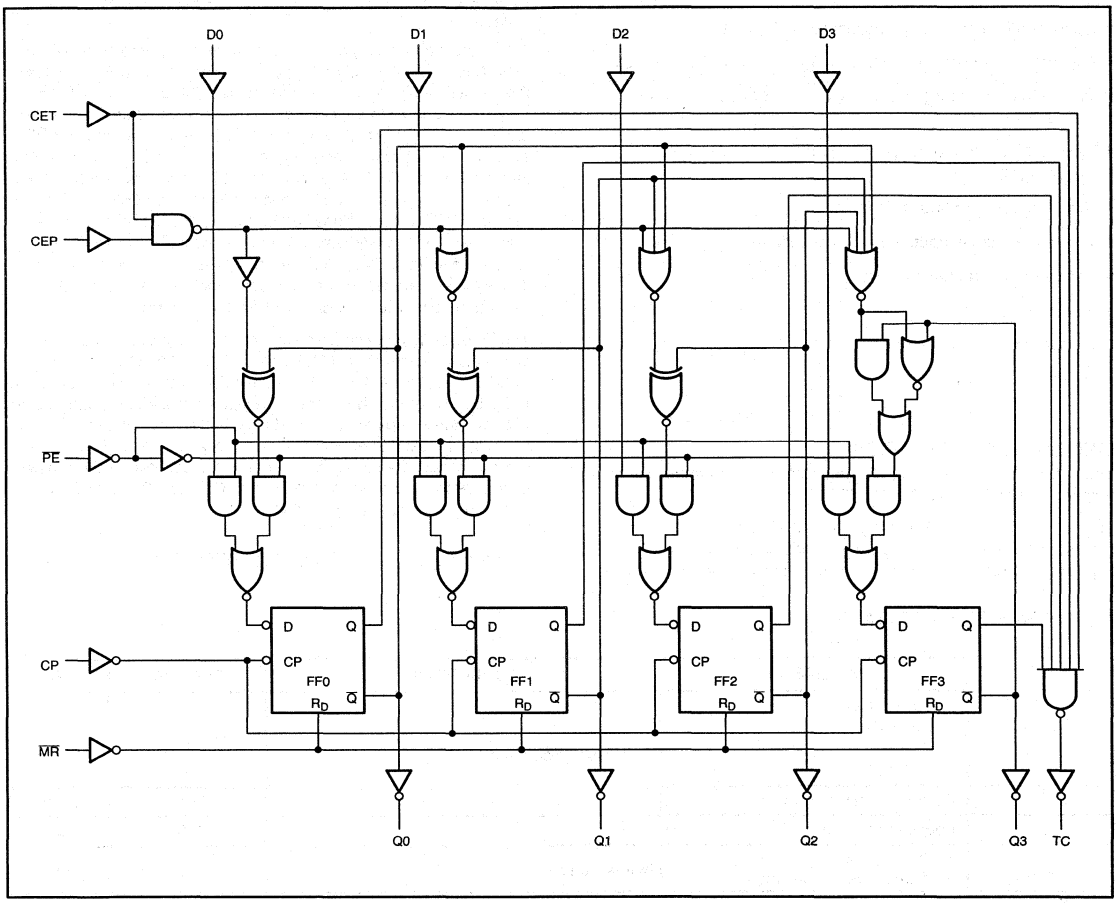
OPERATIONG MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	Dn	Qn	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H H	↑ ↑	X X	X X	l l	l h	L H	L *
Count	H	↑	h	h	h	X	count	*
Hold (do nothing)	H H	X X	l X	X l	h h	X X	qn qn	* L

NOTE:

* The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH).

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
q = Lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition
X = Don't care
↑ = LOW-to-HIGH clock transition

LOGIC DIAGRAM



Presettable synchronous 4-bit binary counter; synchronous reset

74LV163

FEATURES

- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V at V_{CC} = 3.3V, T_{amb} = 25°C
- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Synchronous reset
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74LV163 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT163.

The 74LV163 is a synchronous presettable binary counter that features an internal look-ahead carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).

The outputs (Q0 to Q3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D0 to D3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET). A LOW level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q0 to Q3) to LOW level after the next positive-going transition on the clock (CP) input (provided that the set-up and hold time requirements for $\overline{MR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET and CEP inputs. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q0. This pulse can be used to enable the next cascaded stage. The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{MAX} = \frac{1}{t_{P(MAX)}\ (\text{CP to TC}) + t_{SU}\ (\text{CEP to CP})}$$

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Qn CP to TC CET to TC	C_L = 15pF; V_{CC} = 3.3V	 15 18 9	 ns ns ns
f_{MAX}	Maximum clock frequency		77	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per package	Notes 1 and 2	25	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\ (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; f_o = output frequency in MHz
   C_L = output load capacitance in pF; V_{CC} = supply voltage in V
   $\Sigma\ (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs
2. The condition is V_I = GND to V_{CC}.

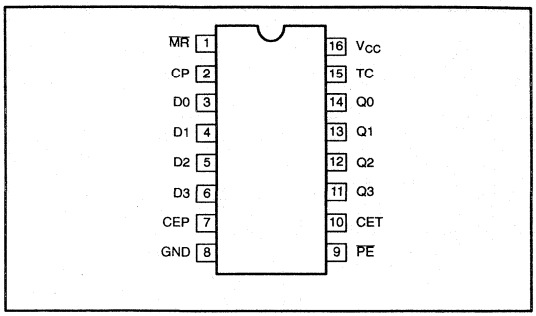
ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV163N	16	DIL	Plastic	DIL16/SOT38-1
74LV163D	16	SO	Plastic	SO16/SOT109-1
74LV163DB	16	SSOP	Plastic	SSOP16/SOT338-1
74LV163PW	16	TSSOP	Plastic	TSSOP16/SOT403-1

Presettable synchronous 4-bit binary counter; synchronous reset

74LV163

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	Synchronous master reset (active LOW)
2	CP	Clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	D0 to D3	Data inputs
7	CEP	Count enable input
8	GND	Ground (0V)
9	$\overline{PE}$	Parallel enable input (active LOW)
10	CET	Count enable carry input
14, 13, 12, 11	Q0 to Q3	Flip-flop outputs
15	TC	Terminal count output
16	V_{CC}	Positive supply voltage

FUNCTION TABLE

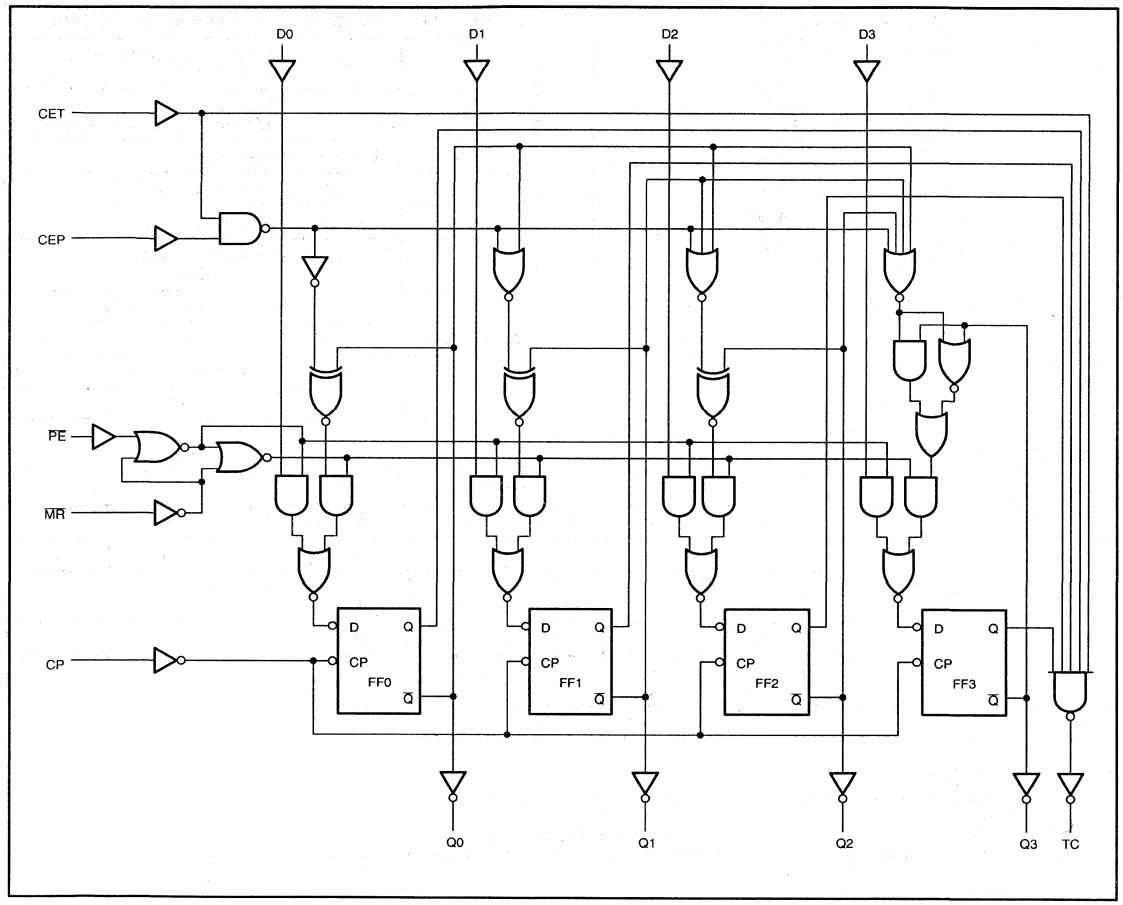
OPERATIONG MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	Dn	Qn	TC
Reset (clear)	l	↑	X	X	X	X	L	L
Parallel load	h h	↑ ↑	X X	X X	l l	l h	L H	L *
Count	h	↑	h	h	h	X	count	*
Hold (do nothing)	h h	X X	l X	X l	h h	X X	qn qn	* L

NOTE:

* The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH).

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
q = Lower case letters indicate the state of the reference output one set-up time prior to the LOW-to-HIGH clock transition
X = Don't care
↑ = LOW-to-HIGH clock transition

LOGIC DIAGRAM



Octal buffer/line driver; 3-State | 74LV244

FEATURES

- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Output capability: bus driver
- I_{CC} category: MSI

DESCRIPTION

The 74LV244 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC/HCT244.

The 74LV244 is an octal non-inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs 1OE and 2OE. A HIGH on nOE causes the outputs to assume a high impedance OFF-state. The 74LV244 is identical to the 74LV240 but has non-inverting outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay 1An to 1Yn; 2An to 2Yn	C_L = 15pF V_{CC} = 3.3V	8	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1, 2	35	pF

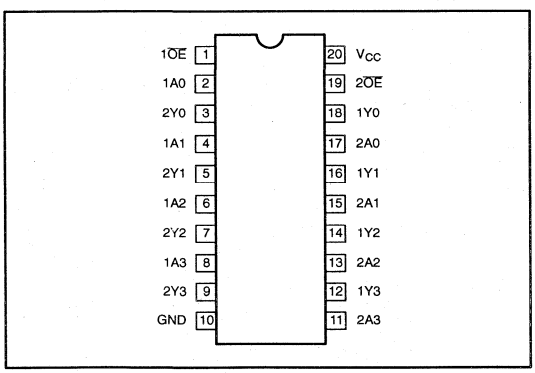
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV244N	20	DIL	Plastic	DIL20/SOT146
74LV244D	20	SO	Plastic	SO20/SOT163A
74LV244DB	20	SSOP	Plastic	SSOP20/SOT339
74LV244PW	20	TSSOP	Plastic	TSSOP20/SOT360

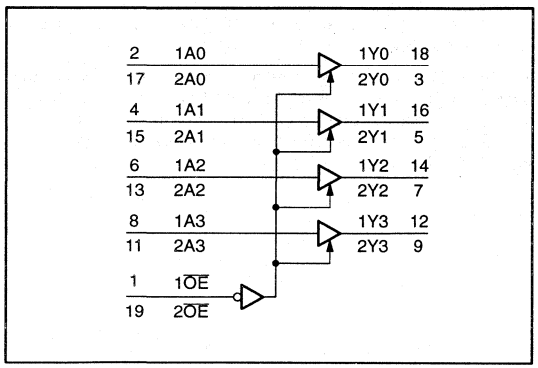
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{1OE}$	Output enable (active LOW)
2, 4, 6, 8	1A0 – 1A3	Data inputs
3, 5, 7, 9	2Y0 – 2Y3	Bus outputs
10	GND	Ground (0V)
17, 15, 13, 11	2A0 – 2A3	Data inputs
18, 16, 14, 12	1Y0 – 1Y3	Bus outputs
19	$\overline{2OE}$	Output enable input (active LOW)
20	V_{CC}	Positive power supply

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUT
n$\overline{OE}$	nAn	nYn
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF-state

Octal bus transceiver; 3-State 74LV245

FEATURES

- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Output capability: bus driver
- I_{CC} category: MSI

DESCRIPTION

The 74LV245 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC/HCT245.

The 74LV245 is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The 74LV245 features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) input for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Bn; Bn to An	C_L = 15pF V_{CC} = 3.3V	7	ns
C_I	Input capacitance		3.5	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1, 2	40	pF

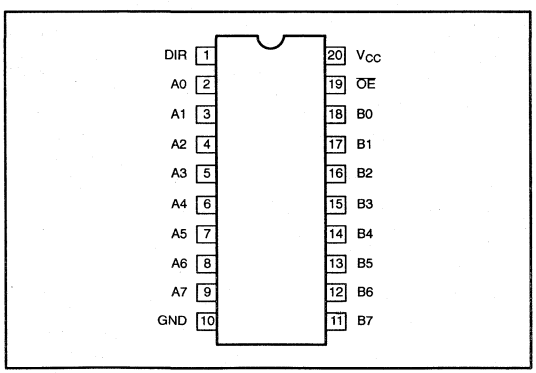
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV245N	20	DIL	Plastic	DIL20/SOT146
74LV245D	20	SO	Plastic	SO20/SOT163A
74LV245DB	20	SSOP	Plastic	SSOP20/SOT339
74LV245PW	20	TSSOP	Plastic	TSSOP20/SOT360

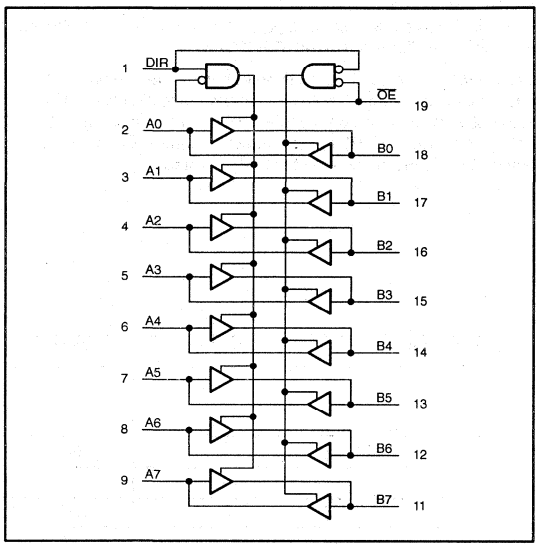
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	DIR	Direction control
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs/outputs
10	GND	Ground (0V)
18, 17, 16, 15, 14, 13, 12, 11	B0 – B7	Data inputs/outputs
19	$\overline{OE}$	Output enable input (active LOW)
20	V_{CC}	Positive power supply

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		INPUTS/OUTPUT	
$\overline{OE}$	DIR	An	Bn
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF-state

Octal D-type flip-flop with reset; positive-edge trigger 74LV273

FEATURES

- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (V_{OH} undershoot) > 2V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Ideal buffer for MOS microprocessor or memory
- Common clock and master reset
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV273 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC/HCT273.

The 74LV273 has eight edge-triggered , D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously. The state of each D input, one set-up time brfore the LOW-to-HIGH clock transition, is transferred to the corresponding output (Qn) of the flip-flop.

All outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the $\overline{MR}$ input.

The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Qn; $\overline{MR}$ to Qn	C_L = 15pF V_{CC} = 3.3V	12 13	ns
f_{max}	Maximum clock frequency		110	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1, 2	20	pF

NOTES:

1 C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; C_L = output load capacity in pF;
f_o = output frequency in MHz; V_{CC} = supply voltage in V;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

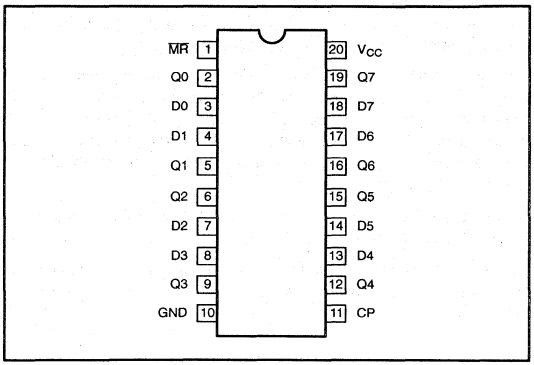
2 The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

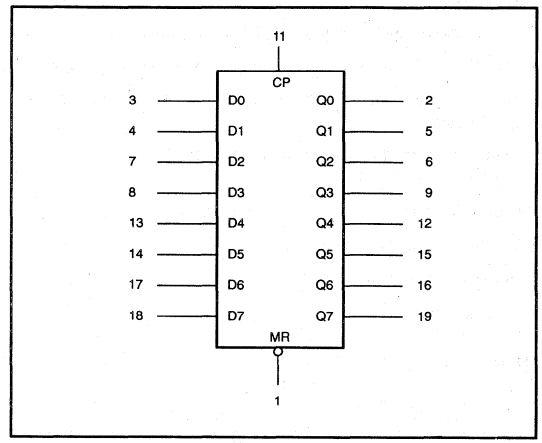
TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV273N	20	DIL	Plastic	DIL20/SOT146
74LV273D	20	SO	Plastic	SO20/SOT163A
74LV273DB	20	SSOP	Plastic	SSOP20/SOT339
74LV273PW	20	TSSOP	Plastic	TSSOP20/SOT360

Octal D-type flip-flop with reset; positive-edge trigger 74LV273

PIN CONFIGURATION



LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{MR}$	Master reset input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 – Q7	Flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 – D7	Data inputs
10	GND	Ground (0V)
19	CP	Clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	Positive power supply

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUT
	$\overline{MR}$	CP	Dn	Q0 – Q7
Reset (clear)	L	L	X	L
Load '1'	H	↑	h	H
Load '0'	H	↑	l	L

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition
↑ = LOW-to-HIGH transition
X = Don't care

Octal D-type transparent latch; 3-State 74LV373

FEATURES

- Optimized for Low Voltage applications: 1.0V to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V at V_{CC} = 3.3V, T_{amb} = 25°C
- Common 3-State output enable input
- Output capability: bus driver
- I_{CC} category: MSI

DESCRIPTION

The 74LV373 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT373.

The 74LV373 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all internal latches.

The 74LV373 consists of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The 74LV373 is functionally identical to the 74LV573, but the 74LV573 has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay D_n to Q_n LE to Q_n	C_L = 15pF V_{CC} = 3.3V	 10 12	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	22	pF

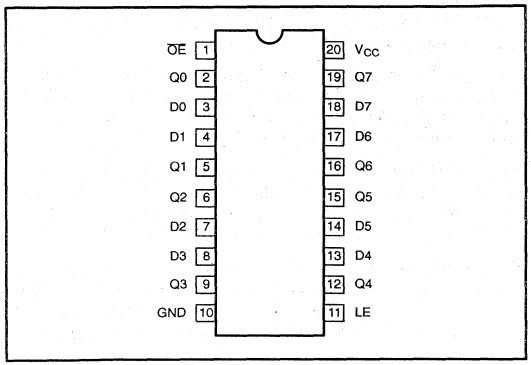
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV373N	20	DIL	Plastic	DIL20/SOT146
74LV373D	20	SO	Plastic	SO20/SOT163A
74LV373DB	20	SSOP	Plastic	SSOP20/SOT339
74LV373PW	20	TSSOP	Plastic	TSSOP20/SOT360

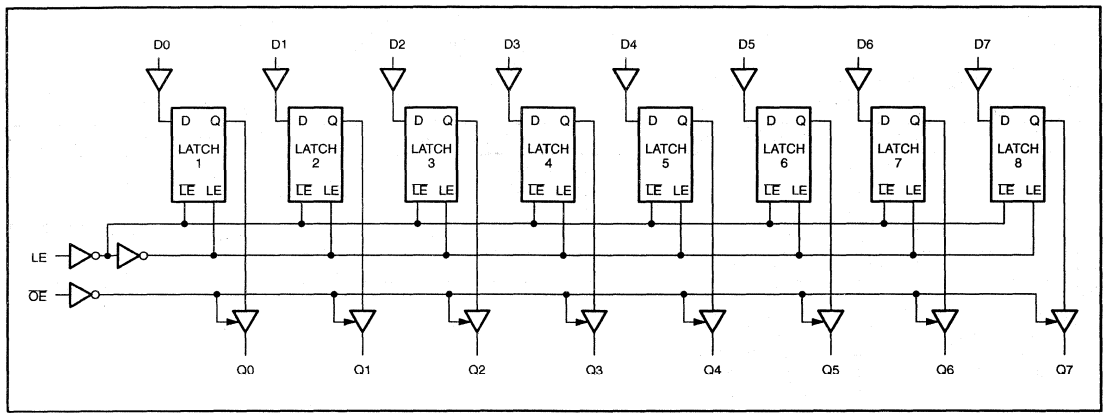
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enabled input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0–Q7	3-State latch outputs
3, 4, 7, 8, 13, 14, 17, 18	D0–D7	Data inputs
10	GND	Ground (0V)
11	LE	Latch enable input (active HIGH)
20	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	Dn		Q0 to Q7
Enable and read register (transparent mode)	L L	H H	L H	L H	L H
Latch and read register	L L	l l	l h	L H	L H
Latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW transition
X = Don't care
Z = High impedance OFF-state

Octal D-type flip-flop; positive edge-trigger; 3-State 74LV374

FEATURES

- Optimized for Low Voltage applications: 1.0V to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V at V_{CC} = 3.3V, T_{amb} = 25°C
- Common 3-State output enable input
- Output capability: bus driver
- I_{CC} category: MSI

DESCRIPTION

The 74LV374 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT374.

The 74LV374 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-State outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The eight flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the eight flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Qn	C_L = 15pF V_{CC}= 3.3V	13	ns
f_{max}	Maximum clock frequency		77	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1, 2	25	pF

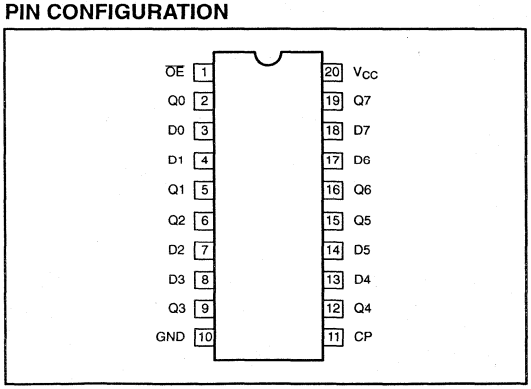
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV374N	20	DIL	Plastic	DIL20/SOT146
74LV374D	20	SO	Plastic	SO20/SOT163A
74LV374DB	20	SSOP	Plastic	SSOP20/SOT339
74LV374PW	20	TSSOP	Plastic	TSSOP20/SOT360

PIN CONFIGURATION

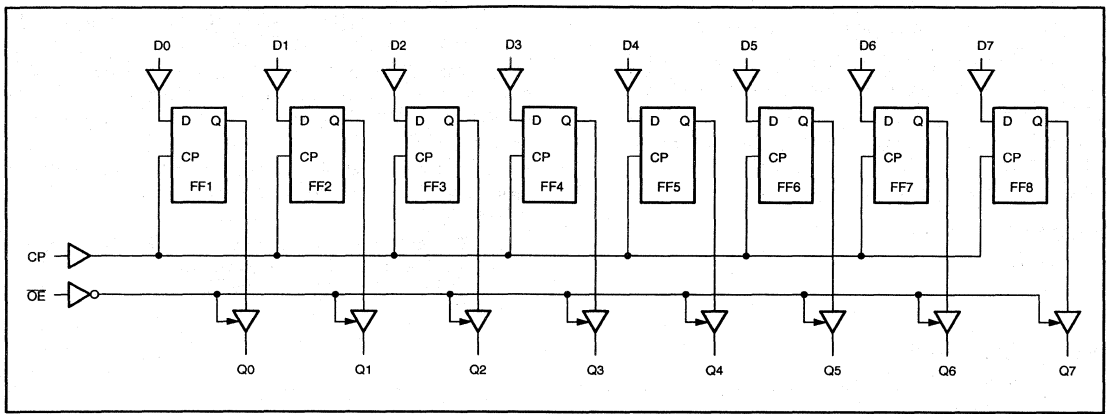


PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0–Q7	3-State flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D0–D7	Data inputs
10	GND	Ground (0V)
11	CP	Clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	Positive supply voltage

Octal D-type flip-flop; positive edge-trigger; 3-State 74LV374

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	Dn		Q0–Q7
Load and read register	L L	↑ ↑	l h	L H	L H
Load register and disable outputs	H H	↑ ↑	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = High impedance OFF-state
↑ = LOW-to-HIGH clock transition

8-bit serial-in/serial or parallel-out shift register with output latches; 3-State

74LV595

FEATURES

- Optimized for Low Voltage applications: 1.0V to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V at V_{CC} = 3.3V, T_{amb} = 25°C
- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-State outputs
- Shift register with direct clear
- Output capability:
  - parallel outputs; bus driver
  - serial output; standard
- I_{CC} category: MSI

APPLICATIONS

- Serial-to-parrallel data conversion
- Remote control holding register

DESCRIPTION

The 74LV595 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT595.

The74LV595 is an 8-stage serial shift register with a storage register and 3-State outputs. The shift register and storage register have separate clocks.

Data is shifted on the positive-going transitions of the SH_{CP} input. The data in each register is transferred to the storage register on a positive-going transition of the ST_{CP} input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register.

The shift register has a serial input (D_S) and a serial standard output (Q_7') all for cascading. It is also provided with asynchronous reset (active LOW) for all 8 shift register stages. The storage register has 8 parallel 3-State bus driver outputs. Data in the storage register appears at the output whenever the output enable input ($\overline{OE}$) is LOW.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay SH_{CP} to Q_7' ST_{CP} to Q_7' $\overline{MR}$ to Q_7'	C_L = 15pF V_{CC}= 3.3V	 15 16 17	ns
f_{max}	Maximum clock frequency SH_{CP}, ST_{CP}		77	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	V_{CC} = 3.3V Notes 1, 2	115	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

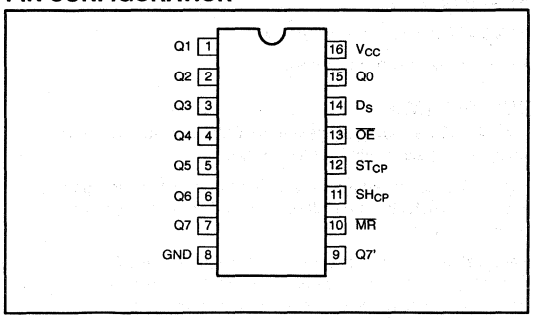
ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV595N	16	DIL	Plastic	DIL16/SOT38Z
74LV595D	16	SO	Plastic	SO16/SOT109A
74LV595DB	16	SSOP	Plastic	SSOP16/SOT338
74LV595PW	16	TSSOP	Plastic	TSSOP16/SOT403

8-bit serial-in/serial or parallel-out shift register with output latches; 3-State

74LV595

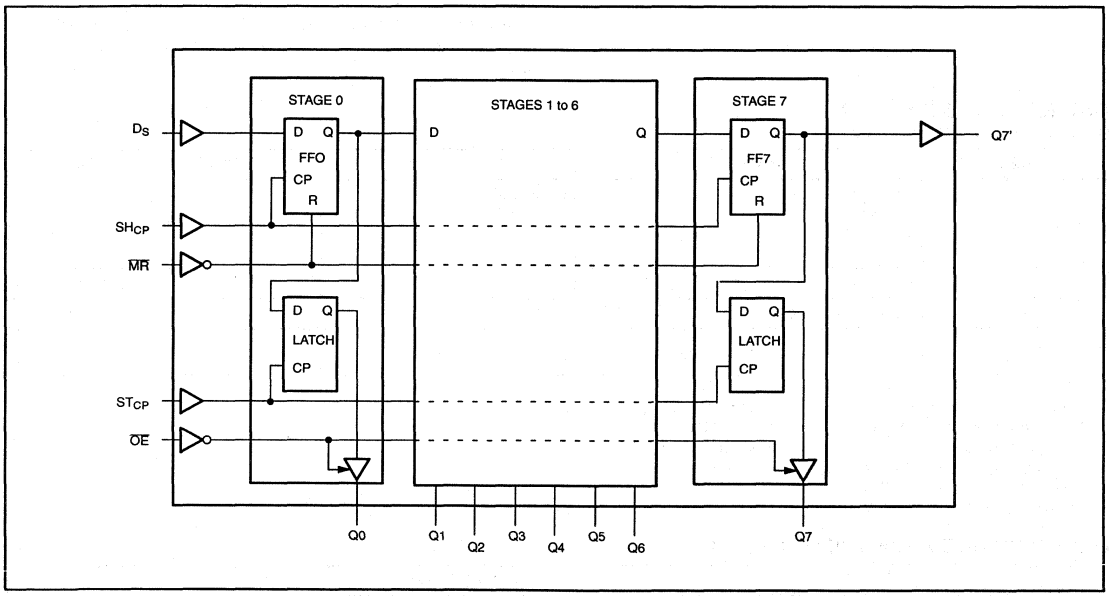
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
15, 1, 2, 3, 4, 5, 6, 7	Q0 – Q7	Parallel data output
8	GND	Ground (0V)
9	Q7'	Serial data output
10	$\overline{MR}$	master reset (active LOW)
11	SH_{CP}	Shift register clock input
12	ST_{CP}	Storage register clock input
13	$\overline{OE}$	Output enable input (active LOW)
14	D_S	Serial data input
16	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS		FUNCTION
SH_{CP}	ST_{CP}	$\overline{OE}$	$\overline{MR}$	D_S	Q7'	Qn	
X	X	L	L	X	L	NC	A LOW level on $\overline{MR}$ only affects the shift registers
X	↑	L	L	X	L	L	Empty shift register loaded into storage register
X	X	H	L	X	L	Z	Shift register clear. Parallel outputs in high-impedance OFF-states
↑	X	L	H	H	Q6'	NC	Logic high level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6') appears on the serial output (Q7')
X	↑	L	H	X	NC	Qn'	Contents of shift register stages (internal Qn') are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6'	Qn'	Contents of shift register shifted through. Previous contents of the shift register are transferred to the storage register and the parallel output stages

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF-state
NC= No change
↑ = LOW-to-HIGH clock transition

8-Channel analog multiplexer/demultiplexer 74LV4051

FEATURES

- Optimized for Low Voltage applications: 1.0 to 6.0V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Low typ "ON" resistance:
  50Ω at $V_{CC} - V_{EE}$ = 4.5V
  70Ω at $V_{CC} - V_{EE}$ = 3.0V
  120Ω at $V_{CC} - V_{EE}$ = 2.0V
- Logic level translation: to enable 3V logic to communicate with ±3V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV4051 is a low-voltage CMOS device and is pin and function compatible with the 74HC/HCT4051.

The 74LV4051 is an 8-channel analog multiplexer/demultiplexer with three digital select inputs (S0 to S2), an active LOW enable input($\overline{E}$), eight independent inputs/outputs (Y0 to Y7) and a common input/output (Z).

With ($\overline{E}$) LOW, one of the eight switches is selected (low impedance ON-state) by S0 to S2. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of S0 to S2.

V_{CC} and GND are the supply voltage pins for the digital control inputs S0 to S2, and $\overline{E}$). The V_{CC} to GND ranges are 1.0 to 6.0V. The analog inputs/outputs (Y0 to Y7, and Z) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 6.0V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZH}/t_{PZL}	Turn "ON" time $\overline{E}$ to V_{OS} Sn to V_{OS}	C_L = 15pF R_L = 1KΩ V_{CC} = 3.3V	23 22	ns
t_{PHZ}/t_{PLZ}	Turn "OFF" time $\overline{E}$ to V_{OS} Sn to V_{OS}		25 20	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per switch	Notes 1, 2	25	pF
C_S	Maximum switch capacitance independent (Y) common (Z)		5 25	pF pF

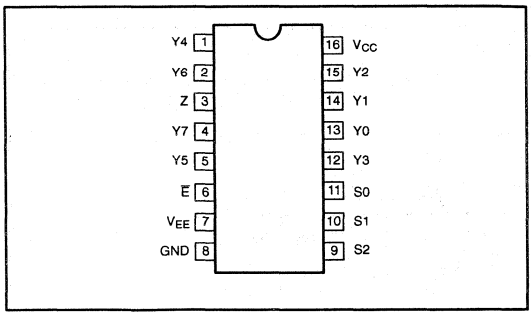
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma ((C_L + C_S) \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; C_S = max. switch capacitance in pF;
   V_{CC} = supply voltage in V;
   $\Sigma ((C_L + C_S) \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV4051N	16	DIL	Plastic	DIL16/SOT38Z
74LV4051D	16	SO	Plastic	SO16/SOT109A
74LV4051DB	16	SSOP	Plastic	SOP16/SOT338
74LV4051PW	16	TSSOP	Plastic	TSSOP16/SOT403

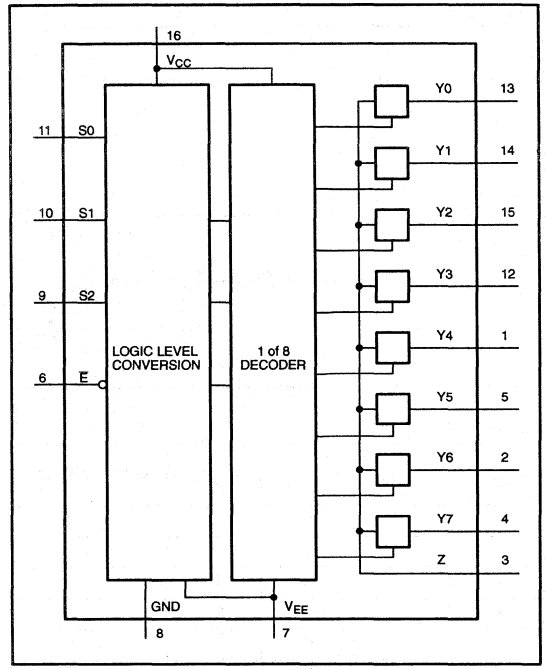
PIN CONFIGURATION



PIN DESCRIPTION

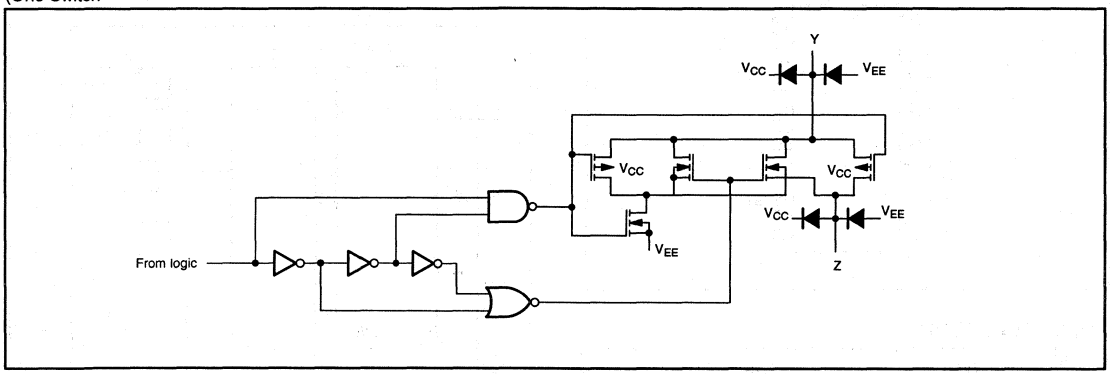
PIN NUMBER	SYMBOL	FUNCTION
3	Z	Common input/output
6	$\overline{E}$	Enable input (active LOW)
7	V_{EE}	Negative supply voltage
8	GND	Ground (0V)
11, 10, 9	S0 to S2	Select inputs
13, 14, 15, 12, 1, 5, 2, 4	Y0 to Y7	Independent inputs/outputs
16	V_{CC}	Positive supply voltage

FUNCTIONAL DIAGRAM



SCHEMATIC DIAGRAM

(One Switch



FUNCTION TABLE

INPUTS				CHANNEL ON
$\overline{E}$	S2	S1	S0	
L	L	L	L	Y0 – Z
L	L	L	H	Y1 – Z
L	L	H	L	Y2 – Z
L	L	H	H	Y3 – Z
L	H	L	L	Y4 – Z
L	H	L	H	Y5 – Z
L	H	H	L	Y6 – Z
L	H	H	H	Y7 – Z
H	X	X	X	none

H = HIGH voltage level
L = LOW voltage level
X = Don't care

Dual 4-channel analog multiplexer/demultiplexer 74LV4052

FEATURES

- Optimized for Low Voltage applications: 1.0 to 6.0V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Low typ "ON" resistance:
  60Ω at $V_{CC} - V_{EE}$ = 4.5V
  90Ω at $V_{CC} - V_{EE}$ = 3.0V
  145Ω at $V_{CC} - V_{EE}$ = 2.0V
- Logic level translation: to enable 3V logic to communicate with ±3V analog signals
- Typical "break before make" built in
- Analog/digital multiplexing and demultiplexing
- Signal gating
- Output capability: non-standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV4052 is a low-voltage CMOS device and is pin and function compatible with the 74HC/HCT4052.

The 74LV4052 is a dual 4-channel analog multiplexer/demultiplexer with common select logic. Each multiplexer has four independent inputs/outputs (nY0 to nY3) and a common input/output (nZ). The common channel select logics include two digital select inputs (S0 and S1) and an active LOW enable input ($\overline{E}$).

With ($\overline{E}$) LOW, one of the four switches is selected (low impedance ON-state) by S0 and S1. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state independent of S0 and S1.

V_{CC} and GND are the supply voltage pins for the digital control inputs S0, S1, and $\overline{E}$). The V_{CC} to GND ranges are 1.0 to 6.0V. The analog inputs/outputs (nY0 to nY3, and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 6.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZH}/t_{PZL}	Turn "ON" time $\overline{E}$ or Sn, V_{OS}	C_L = 15pF R_L = 1KΩ V_{CC} = 3.3V	30	ns
t_{PHZ}/t_{PLZ}	Turn "OFF" time $\overline{E}$ or Sn V_{OS}		22	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per switch	Notes 1, 2	57	pF
C_S	Maximum switch capacitance independent (Y) common (Z)		 5 12	 pF pF

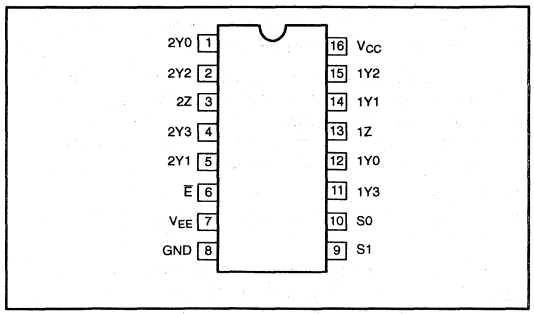
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma ((C_L + C_S) \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; C_S = max. switch capacitance in pF;
   V_{CC} = supply voltage in V;
   $\Sigma ((C_L + C_S) \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV4052N	16	DIL	Plastic	DIL16/SOT38Z
74LV4052D	16	SO	Plastic	SO16/SOT109A
74LV4052DB	16	SSOP	Plastic	SOP16/SOT338
74LV4052PW	16	TSSOP	Plastic	TSSOP16/SOT403

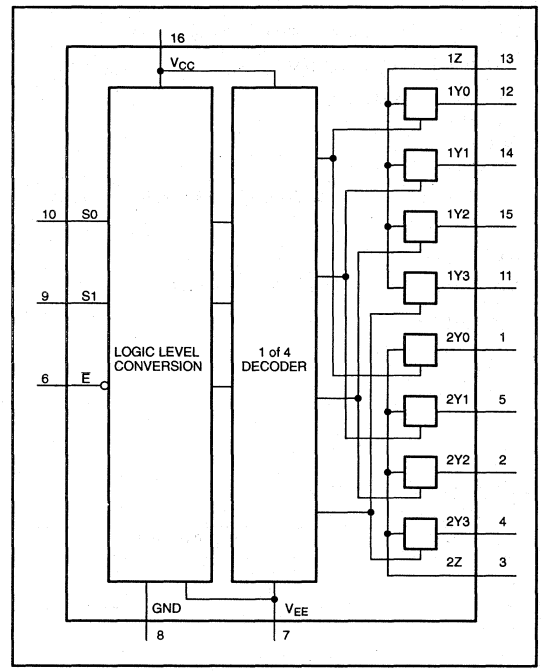
PIN CONFIGURATION



PIN DESCRIPTION

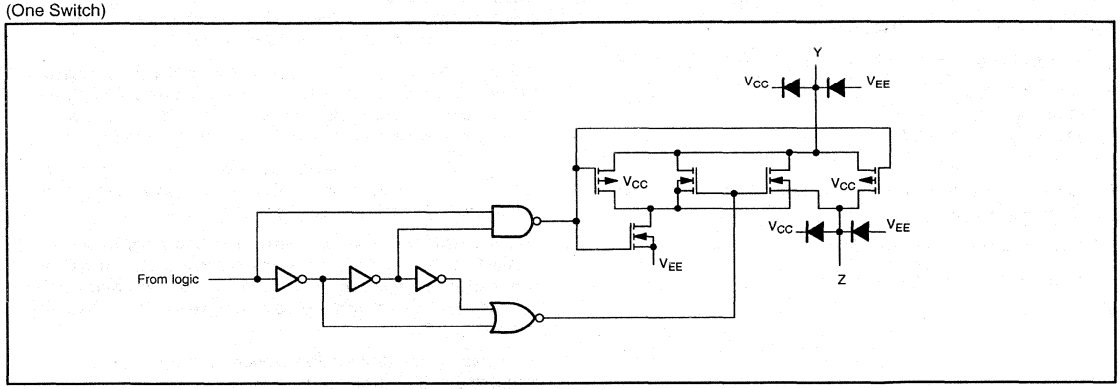
PIN NUMBER	SYMBOL	FUNCTION
1, 5, 2, 4	2Y0 to 2Y3	Independent inputs/outputs
6	$\overline{E}$	Enable input (active LOW)
7	V_{EE}	Negative supply voltage
8	GND	Ground (0V)
10, 9	S0 to S1	Select inputs
12, 14, 15, 11	1Y0 to 1Y3	Independent inputs/outputs
13, 3	1Z, 2Z	Common inputs/outputs
16	V_{CC}	Positive supply voltage

FUNCTIONAL DIAGRAM



SCHEMATIC DIAGRAM

(One Switch)



FUNCTION TABLE

INPUTS			CHANNEL ON
$\overline{E}$	S1	S0	
L	L	L	nY0 – nZ
L	L	H	nY1 – nZ
L	H	L	nY2 – nZ
L	H	H	nY3 – nZ
H	X	X	none

H = HIGH voltage level
L = LOW voltage level
X = Don't care

Triple 2-channel analog multiplexer/demultiplexer 74LV4053

FEATURES

- Optimized for Low Voltage applications: 1.0 to 6.0V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Low typ "ON" resistance:
  50Ω at $V_{CC} - V_{EE}$ = 4.5V
  70Ω at $V_{CC} - V_{EE}$ = 3.0V
  120Ω at $V_{CC} - V_{EE}$ = 2.0V
- Logic level translation: to enable 3V logic to communicate with ±3V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV4053 is a low-voltage CMOS device and is pin and function compatible with the 74HC/HCT4053.

The 74LV4053 is a triple 2-channel analog multiplexer/demultiplexer with a common enable input ($\overline{E}$). Each multiplexer/demultiplexer has two independent inputs/outputs (nY0 to nY1) a common input/output (nZ) and three digital select inputs (S1 to S3)

With ($\overline{E}$) LOW, one of the two switches is selected (low impedance ON-state) by S1 to S3. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state independent of S1 and S3.

V_{CC} and GND are the supply voltage pins for the digital control inputs S1 to S3, and $\overline{E}$). The V_{CC} to GND ranges are 1.0 to 6.0V. The analog inputs/outputs (nY0 to nY1, and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 6.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZH}/t_{PZL}	Turn "ON" time $\overline{E}$ to V_{OS} Sn to V_{OS}	C_L = 15pF R_L = 1KΩ V_{CC} = 3.3V	16 20	ns
t_{PHZ}/t_{PLZ}	Turn "OFF" time $\overline{E}$ to V_{OS} Sn to V_{OS}		17 16	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per switch	Notes 1, 2	36	pF
C_S	Maximum switch capacitance independent (Y) common (Z)		5 8	pF pF

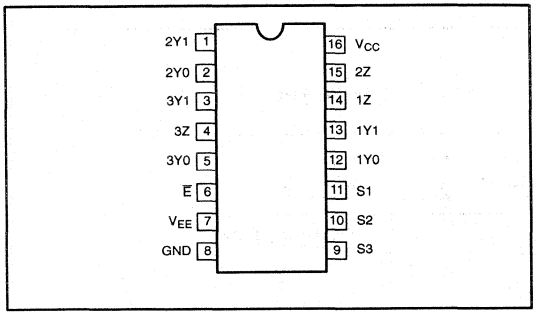
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma ((C_L + C_S) \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; C_S = max. switch capacitance in pF;
   V_{CC} = supply voltage in V;
   $\Sigma ((C_L + C_S) \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV4053N	16	DIL	Plastic	DIL16/SOT38Z
74LV4053D	16	SO	Plastic	SO16/SOT109A
74LV4053DB	16	SSOP	Plastic	SOP16/SOT338
74LV4053PW	16	TSSOP	Plastic	TSSOP16/SOT403

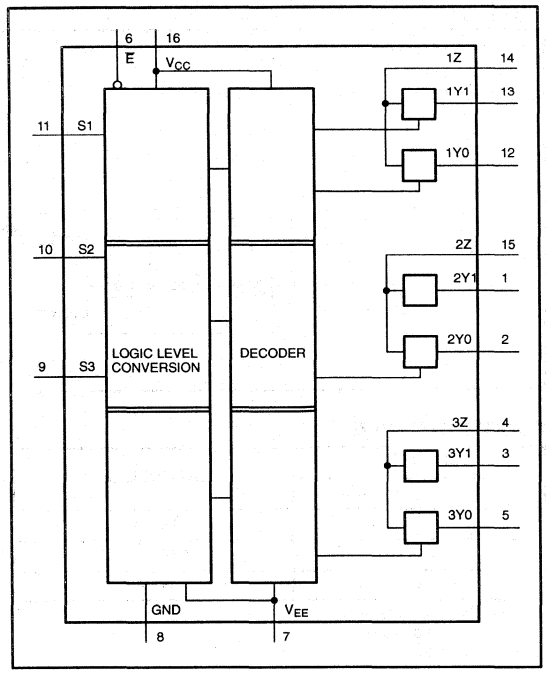
PIN CONFIGURATION



PIN DESCRIPTION

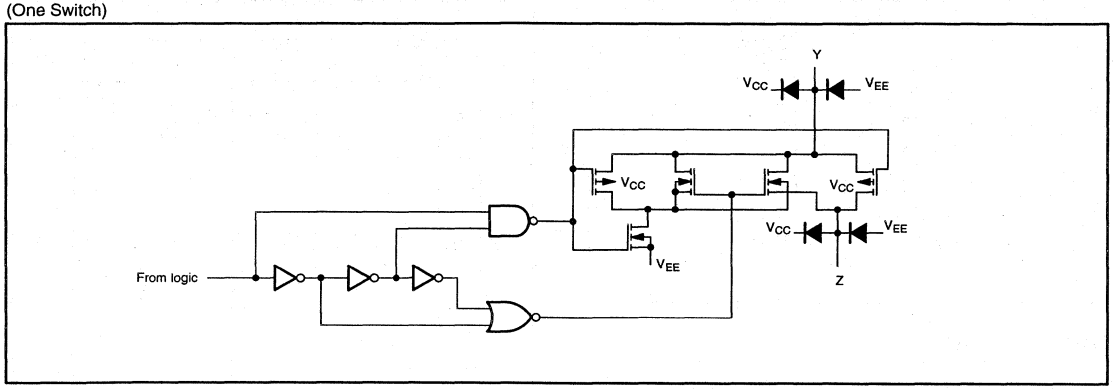
PIN NUMBER	SYMBOL	FUNCTION
2, 1	2Y0 to 2Y1	Independent inputs/outputs
5, 3	3Y0 to 3Y1	Independent inputs/outputs
6	$\overline{E}$	Enable input (active LOW)
7	V_{EE}	Negative supply voltage
8	GND	Ground (0V)
11, 10, 9	S0 to S1	Select inputs
12, 13	1Y0 to 1Y1	Independent inputs/outputs
14, 15, 4	1Z to 3Z	Common inputs/outputs
16	V_{CC}	Positive supply voltage

FUNCTIONAL DIAGRAM



SCHEMATIC DIAGRAM

(One Switch)



FUNCTION TABLE

INPUTS		CHANNEL ON
$\overline{E}$	S2	
L	L	nY0 – nZ
L	H	nY1 – nZ
H	X	none

H = HIGH voltage level
L = LOW voltage level
X = Don't care

Quad bilateral switches | 74LV4066

FEATURES

- Optimized for Low Voltage applications: 1.0 to 6.0V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Very low "ON" resistance:
  25Ω at $V_{CC} - V_{EE}$ = 4.5V
  35Ω at $V_{CC} - V_{EE}$ = 3.0V
  60Ω at $V_{CC} - V_{EE}$ = 2.0V
- Output capability: non-standard
- I_{CC} category: SSI

DESCRIPTION

The 74LV4066 is a low-voltage CMOS device and is pin and function compatible with the 74HC/HCT4066.

The 74LV4066 has four independent analog switches. Each switch has two input/output terminals (nY, nZ) and an active HIGH enable input (nE). When nE is LOW the corresponding analog switch is turned off.

The 74LV4066 has an "ON" resistance which is dramatically reduced in comparison with 74HC/HCT4066.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZH}/t_{PZL}	Turn-on time $n\overline{E}$ to V_{OS}	C_L = 15pF R_L = 1KΩ V_{CC} = 3.3V	10	ns
t_{PHZ}/t_{PLZ}	Turn-off time $n\overline{E}$ to V_{OS}		13	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per switch	Notes 1, 2	11	pF
C_S	Maximum switch capacitances		8	pF

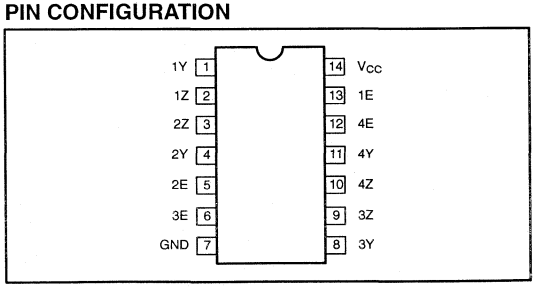
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma ((C_L + C_S) \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; C_S = max. switch capacitance in pF;
   $\Sigma \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of the outputs.
   V_{CC} = supply voltage in V;
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV4066N	14	DIL	Plastic	DIL14/SOT27
74LV4066D	14	SO	Plastic	SO14/SOT108A
74LV4066DB	14	SSOP	Plastic	SOP14/SOT337
74LV4066PW	14	TSSOP	Plastic	TSSOP14/SOT402

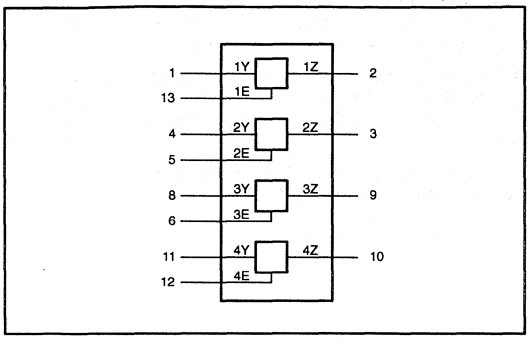
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 4, 8, 11	1Y – 4YZ	Independent inputs/outputs
2, 3, 9, 10	1Z – 4Z	Independent inputs/outputs
13, 5, 6, 12	1E – 4E	Enable inputs (active HIGH)
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

FUNCTIONAL DIAGRAM



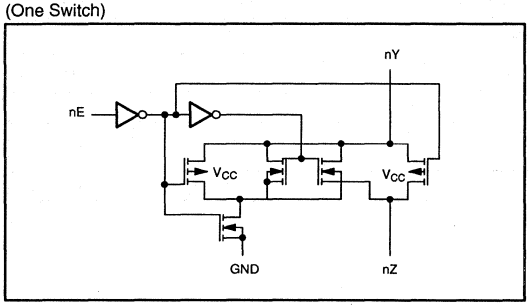
FUNCTION TABLE

INPUT nE	SWITCH
L	off
H	on

H = HIGH voltage level
L = LOW voltage level

SCHEMATIC DIAGRAM

(One Switch)



Quad bilateral switches 74LV4316

FEATURES

- Optimized for Low Voltage applications: 1.0V to 6.0V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Low typ "ON" resistance:
  80Ω at V_{CC} – VEE = 4.5V
  120Ω at V_{CC} – VEE = 3.0V
  295Ω at V_{CC} – VEE = 2.0V
- Logic level translation: to enable 3V logic to communicate with ±3V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV4316 is a low-voltage CMOS device that is pin and function compatible with 74HC/HCT4316.

The74LV4316 has four independent analog switches. Each switch has two input/output terminals (nY, nZ) and an active HIGH select input (nS). When the enable input ($\overline{E}$) is HIGH, all four analog switches are turned off.

Current through a switch will not cause additional VCC current provided the voltage at the terminals of the switch is maintained within the supply voltage range; $V_{CC} > (V_Y, V_Z) > V_{EE}$. Inputs nY and nZ are electrically equivalent terminals. V_{CC} and GND are the supply voltage pins for the digital control inputs ($\overline{E}$ and nS). The V_{CC} to GND ranges are 1.0 to 6.0V.

The analog inputs/outputs (nY and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit.

$V_{CC} - V_{EE}$ may not exceed 6.0V.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Turn "ON" time: $\overline{E}$ to V_{OS} nS to V_{OS}	C_L = 15pF R_L = 1KΩ V_{CC}= 3.3V	19	ns
t_{PHL}/t_{PLH}	Turn "ON" time: $\overline{E}$ to V_{OS} nS to V_{OS}		20	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per switch	Notes 1, 2	13	pF
C_S	Maximum switch capacitance		5	pF

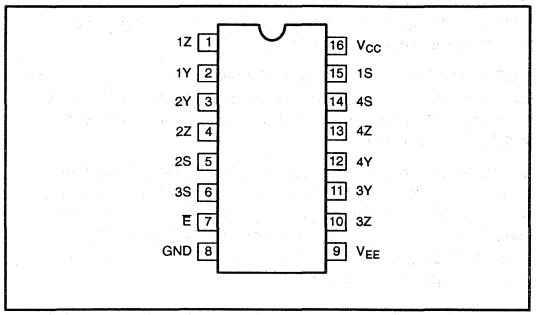
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma ((C_L + C_S) \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; C_S = max. switch capacitance in pF;
   V_{CC} = supply voltage in V;
   $\Sigma ((C_L + C_S) \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV4316N	16	DIL	Plastic	DIL16/SOT38Z
74LV4316D	16	SO	Plastic	SO16/SOT109A
74LV4316DB	16	SSOP	Plastic	SSOP16/SOT338
74LV4316PW	16	TSSOP	Plastic	TSSOP16/SOT403

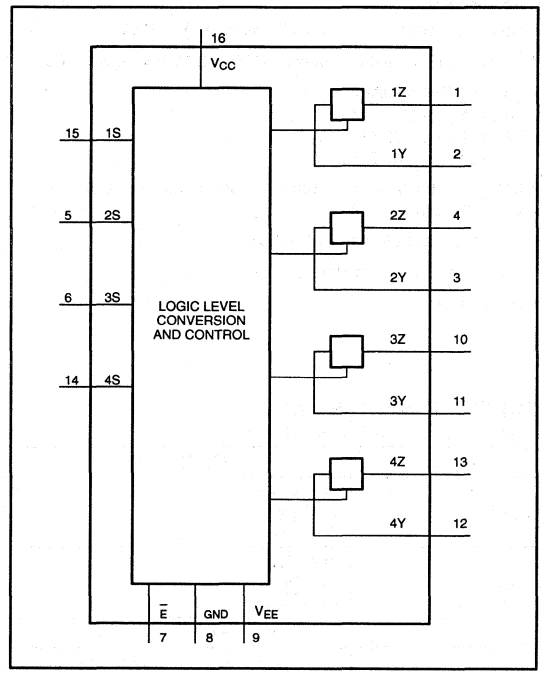
PIN CONFIGURATION



PIN DESCRIPTION

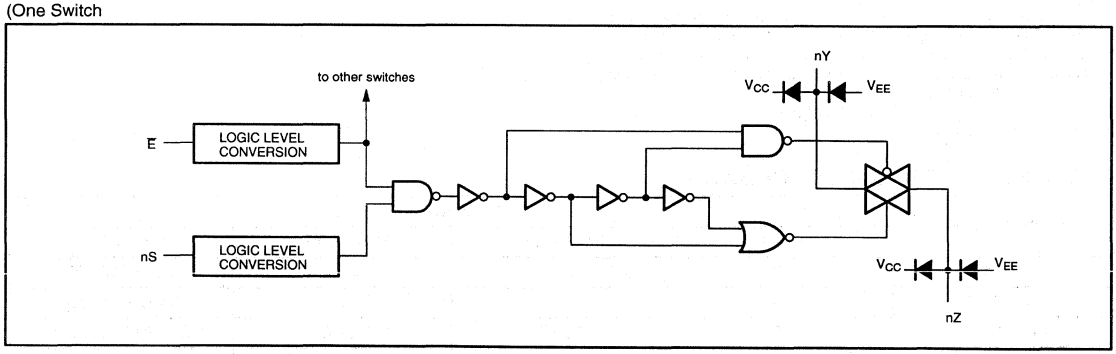
PIN NUMBER	SYMBOL	FUNCTION
1, 4, 10, 13	1Z – 4Z	Independent inputs/ouputs
2, 3, 11, 12	1Y – 4Y	Independent inputs/ouputs
7	$\overline{E}$	Enable input (active LOW)
8	GND	Ground (0V)
9	V_{EE}	Negative supply voltage
15, 5, 6, 14	1S – 4S	Select inputs (active HIGH)
16	V_{CC}	Positive supply voltage

FUNCTIONAL DIAGRAM



SCHEMATIC DIAGRAM

(One Switch



LV Netlists

LV BERKELEY SPICE MODELS

```
* LV.CIR
* STANDARD LOGIC PRODUCT GROUP
* PHILIPS SEMICONDUCTORS
* 3/28/95
*-----------------------------------------------------------------*
* SIMULATION MODULES OF CMOS LOGIC PARTS OF PHILIPS LV  FAMILY *
*                   BERKELEY SPICE FORMAT                         *
*-----------------------------------------------------------------*
* IN ORDER TO SIMULATE A SPECIFIC LVC DEVICE, GO TO THE END OF *
* FILE UNDER HEADING 'START RUNNING CIRCUIT MODEL' AND REMOVE  *
* THE COMMENT STATEMENT '*' BEFORE THE REQUIRED DEVICE.        *
* ALL OTHER DEVICES MUST HAVE AN '*' COMMENT STATEMENT.        *
* IF YOU LIKE TO SIMULATE WITH FAST OR SLOW PARAMETERS, GO TO  *
* HEADING 'PROCESS MODELS' AND REMOVE THE COMMENT STATEMENT '*'*
* BEFORE THE REQUIRED PROCESS MODEL.                           *
* YOU MAY ONLY SIMULATE ONE DEVICE AT THE TIME.                *
* THE LOAD CIRCUIT AND SIMULATION TIMING SHOULD NORMALLY BE    *
* ADAPTED TO YOUR SPECIFIC SITUATION.                          *
*-----------------------------------------------------------------*

*********************************************************************
*                                                                   *
* These LV  models represent only one data input and one output  *
* of the device. Devices with a 3-state output buffer also have  *
* an Output Enable (OE) input. The LV138 also has an Input Enable*
* (EN) input. Other control inputs such as DIR or CLK inputs are *
* not modeled. Circuitry between the input and output buffers are*
* also omitted, such as gates, registers, latches, mux's and     *
* intermediate buffers. One result of this is that LV models do  *
* not show the exact function of the device.  Another result of  *
* this is that propagation delays in SPICE will not necessarily  *
* match with the published AC timing specifications in the device*
* datasheet.                                                     *
*                                                                   *
*********************************************************************
.OPTIONS  ACCT   LIST  OPTS  ITL5=25000  NOMOD

* Nominal parameters
.INC c:\spice\lv\lvnomi.cir

* Fast parameters
*.INC c:\spice\lv\lvfast.cir

* Slow parameters
*.INC c:\spice\lv\lvslow.cir

*************  START RUNNING CIRCUIT MODEL  **************

*XLV00   2  3  1  0        INV2
XLV04   2  3  1  0        INV0
*XLV14   2  3  1  0        INVSMT
*XLV32   2  3  1  0        NINV1
*XLV74   2  3  1  0        INV1
*XLV123  2  3  1  0        INV1
*XLV132  2  3  1  0        INV1
*XLV138  2  5  3  1  0     NANDINV
*XLV161  2  3  1  0        INV2
*XLV163  2  3  1  0        INV2
*XLV244  2  5  3  1  0     NINV3
```

```
*XLV245  2  5  3  1  0     NINV3
*XLV273  2  3  1  0        NINV1
*XLV373  2  5  3  1  0     NINV3
*XLV374  2  5  3  1  0     NINV3
*XLV595  2  5  3  1  0     NINV3
*XLV4040 2  3  1  0        NINV1
*XLV4051 2  3  4  5  1  0  SWI1
*XLV4052 2  3  4  5  1  0  SWI1
*XLV4053 2  3  4  5  1  0  SWI1
*XLV4066 2  3  4  1  0     SWI2
*XLV4316 2  3  4  5  1  0  SWI3
*XLV4538 2  3  1  0        INV1

*******************************************************************************

*R1  3  1  1K
* Use only for 3-state Tplz

*R1  3  0  1K
* Use only for 3-state Tphz

C1   3  0  50P
R1   3  0  1K
VCC  1  0  DC   3.0
VIN1 2  0  PULSE 0  3.0  5N  2.5N  2.5N  30N 100N

*VEN   5  0  DC   0.0
* Use only for LV138/244/245/373/374/595

****Use this part only for 4051 - 4053 and the 4316 Ron calculations ****
*VEE   5  0  DC  -4.5
*VIN2  2  0  DC   4.5

**VIN3  3  5  PULSE 0  4.5  5N  6N  6N  40N  70N
*Only for TRAN*

*VIN4  3  5  DC   9.0
*ILAST 4  5  DC   1mA
*C1    3  0  50P
*C2    4  0  50P
*******************************************************************************

***********Use this part only for the 4066 Ron calculations *************
*VIN2  2  0  DC   4.5

**VIN3  3  0  PULSE 0  4.5  5N  6N  6N  40N  70N
*Only for TRAN*

*VIN4  3  0  DC   4.5
*ILAST 4  0  DC   1mA
*C1    3  0  50P
*C2    4  0  50P
*******************************************************************************

*.PRINT TRAN  V(3)  V(4)
*Only for 4051 - 4060 with TRAN analysis

.TRAN  1N   100N
.PRINT TRAN  V(2)  V(3)
.PROBE  V(2) V(3)
.END
```

LVNOMI.CIR Subcircuit

```
* LV Subcircuit and Primitive Elements Library
* LVNOMI.CIR
* Nominal Process Corner
* Standard Logic Product Group
* Philips Semiconductors
* 3/28/95
************************************************
*          NOMINAL N-Channel Transistor        *
*             UCB-3 Parameter Set              *
*          LOW VOLTAGE CMOS Logic Family       *
*                10-Jan.-1995                  *
************************************************
.Model MLVNEN NMOS
+LEVEL = 3
+KP    = 65.0E-6
+VTO   = 0.46
+TOX   = 30.0E-9
+NSUB  = 2.8E15
+GAMMA = 0.94
+PHI   = 0.65
+VMAX  = 150E3
+RS    = 30
+RD    = 30
+XJ    = 0.11E-6
+LD    = 0.4E-6
+DELTA = 0.315
+THETA = 0.054
+ETA   = 0.015
+KAPPA = 0.0
+WD    = 0.0

************************************************
*         NOMINAL P-Channel transistor         *
*            UCB-3 Parameter Set               *
*          LOW VOLTAGE CMOS Logic Family       *
*                10-Jan.-1995                  *
************************************************
.Model MLVPEN PMOS
+LEVEL = 3
+KP    = 20.3E-6
+VTO   = -0.61
+TOX   = 30.0E-9
+NSUB  = 3.3E16
+GAMMA = 0.92
+PHI   = 0.65
+VMAX  = 970E3
+RS    = 60
+RD    = 60
+XJ    = 0.63E-6
+LD    = 0.15E-6
+DELTA = 2.24
+THETA = 0.108
+ETA   = 0.322
+KAPPA = 0.0
+WD    = 0.0
```

```
****************************************
*   START OF SUB-CIRCUIT DESCRIPTION   *
*            MARCH 28, 1995            *
****************************************

*****NOMIN.CIR*****

.SUBCKT INP0N  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2  3  100
MP1 3 50 50 50  MLVPEN W=20U L=2.0U AD=100P AS=100P PD=40U PS= 20U
MN1 3 60 60 60  MLVNEN W=35U L=2.0U AD=260P AS=260P PD=70U PS= 20U
.ENDS

.SUBCKT INP1N  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MLVPEN W=20U L=2.0U AD=100P AS=100P PD=40U PS= 20U
MN1 4 60 60 60  MLVNEN W=35U L=2.0U AD=260P AS=260P PD=70U PS= 20U
MP2 3  4 50 50  MLVPEN W=88U L=2.0U AD=290P AS=550P PD=10U PS=100U
MN2 3  4 60 60  MLVNEN W=56U L=2.0U AD=162P AS=550P PD=10U PS= 75U
.ENDS

.SUBCKT INP2N  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MLVPEN W= 20U L=2.0U AD= 100P AS=100P PD= 40U PS= 20U
MN1 4 60 60 60  MLVNEN W= 35U L=2.0U AD= 260P AS=260P PD= 70U PS= 20U
MP2 3  4 50 50  MLVPEN W=176U L=2.0U AD= 580P AS=1000P PD=10U PS=200U
MN2 3  4 60 60  MLVNEN W=112U L=2.0U AD= 325P AS=1000P PD=10U PS=150U
.ENDS

.SUBCKT SMT1N  2  3  50  60
* SCHMITT-TRIGGER INPUT FOR LV14 CMOS INPUT LEVELS
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MLVPEN W=20U L=2.0U AD=100P AS=100P PD=40U PS=20U
MN1 4 60 60 60  MLVNEN W=35U L=2.0U AD=140P AS=140P PD=50U PS=35U
MP2 5  4 50 50  MLVPEN W=36U L=2.0U AD=140P AS=140P PD=50U PS=35U
MN2 6  4 60 60  MLVNEN W=16U L=2.0U AD= 70P AS= 70P PD=15U PS=17U
MP3 3  4  5 50  MLVPEN W=44U L=4.0U AD=220P AS=220P PD=60U PS=44U
MN3 3  4  6  6  MLVNEN W=17U L=2.0U AD= 70P AS= 70P PD=15U PS=16U
MP4 5  3 60 50  MLVPEN W=36U L=2.0U AD=150P AS=150P PD=60U PS=36U
MN4 6  3 50  6  MLVNEN W= 6U L=4.0U AD= 25P AS= 25P PD=10U PS= 6U
.ENDS

.SUBCKT INVN  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
MP1 3  2 50 50  MLVPEN W=364U L=2.0U AD=500P  AS=500P PD=10U PS=430U
MN1 3  2 60 60  MLVNEN W=184U L=2.0U AD=275P  AS=275P PD=10U PS=270U
.ENDS

.SUBCKT NANDN  2  3  4  50  60
*INTERNAL NAND
*IN1 = 2, IN2 = 3, OUT = 4, VCC= 50, GND = 60
MP1 4  2  50  50  MLVPEN W=112U  L=2.0U AD=150P AS=300P PD= 75U PS=150U
MP2 4  3  50  50  MLVPEN W=112U  L=2.0U AD=150P AS=300P PD= 75U PS=150U
MN1 4  2   5  60  MLVNEN W=300U  L=2.0U AD=300P AS=300P PD=300U PS=300U
MN2 5  3  60  60  MLVNEN W=300U  L=2.0U AD=300P AS=300P PD=300U PS=300U
.ENDS
```

```
.SUBCKT LLCN  2  3  40  50  60
* LEVEL CONVERTER
* INA = 2,  OUT = 3,  VEE = 40,  VCC = 50,  GND =  60
MP4 4  2  50  50  MLVPEN W= 30U  L= 2.4U AD=120P AS=120P PD= 40U PS= 30U
MN4 4  2  60  60  MLVNEN W= 15U  L= 2.4U AD= 60P AS= 60P PD= 20U PS= 15U
MP1 5  2  50  50  MLVPEN W=135U  L= 2.4U AD=500P AS=500P PD=100U PS=135U
MP2 6  2  50  50  MLVPEN W=135U  L= 2.4U AD=500P AS=500P PD=100U PS=135U
MN1 5  6  40  40  MLVNEN W=6.4U  L=18.8U AD= 25P AS= 25P PD= 20U PS=6.4U
MN2 6  5  40  40  MLVNEN W=6.4U  L=18.8U AD= 25P AS= 25P PD= 20U PS=6.4U
MP3 7  6  50  50  MLVPEN W= 10U  L= 4.0U AD= 40P AS= 40P PD= 20U PS= 10U
MN3 7  6  40  40  MLVNEN W=  5U  L= 4.0U AD= 20P AS= 20P PD= 10U PS=  5U
MP5 3  7  50  50  MLVPEN W= 30U  L= 2.4U AD=120P AS=120P PD= 40U PS= 30U
MN5 3  7  40  40  MLVNEN W= 15U  L= 2.4U AD= 60P AS= 60P PD= 20U PS= 15U
.ENDS

.SUBCKT SWITCH1N  2  8  9  40  50
* ANALOG SWITCH
* INPUT = 2   Y = 8  Z = 9  VEE = 40  VCC =50
MP1 3  2  50  50  MLVPEN W=  88U L=2.0U AD= 350P AS= 350P PD=100U PS=  88U
MN1 3  2  40  40  MLVNEN W=  56U L=2.0U AD= 225P AS= 225P PD= 70U PS=  56U
MP4 4  3  50  50  MLVPEN W= 350U L=2.0U AD= 900P AS= 900P PD=200U PS= 350U
MN4 4  3  40  40  MLVNEN W= 150U L=2.0U AD= 400P AS= 400P PD=100U PS= 150U
MP5 8  4   5  50  MLVPEN W= 216U L=2.0U AD= 900P AS= 900P PD=100U PS= 216U
MN5 8  3   5   5  MLVNEN W= 108U L=2.0U AD= 430P AS= 430P PD= 50U PS= 108U
MN6 5  4  40  40  MLVNEN W= 145U L=2.0U AD= 600P AS= 600P PD= 75U PS= 145U
MP7 9  4   8  50  MLVPEN W=1068U L=2.0U AD=2500P AS=2500P PD= 10U PS=1068U
MN7 9  3   8   5  MLVNEN W= 312U L=2.0U AD=1200P AS=1200P PD= 10U PS= 312U
.ENDS

.SUBCKT SWITCH2N  2  8  9  50  60
* ANALOG SWITCH
* INPUT= 2   Y= 8   Z= 9  VCC= 50   GND= 60
MP1 3  2  50  50  MLVPEN W=  88U L=2.0U AD= 350P AS= 350P PD=100U PS=  88U
MN1 3  2  60  60  MLVNEN W=  56U L=2.0U AD= 225P AS= 225P PD= 70U PS=  56U
MP4 4  3  50  50  MLVPEN W= 350U L=2.0U AD= 900P AS= 900P PD=200U PS= 350U
MN4 4  3  60  60  MLVNEN W= 150U L=2.0U AD= 400P AS= 400P PD=100U PS= 150U
MP5 5  3   8  50  MLVPEN W=  85U L=2.0U AD= 355P AS= 355P PD= 40U PS=  85U
MN5 5  4   8   5  MLVNEN W=  42U L=2.0U AD= 170P AS= 170P PD= 20U PS=  42U
MN6 5  3  60  60  MLVNEN W= 145U L=2.0U AD= 600P AS= 600P PD= 75U PS= 145U
MP7 9  3   8  50  MLVPEN W=1900U L=2.0U AD=2500P AS=2500P PD= 10U PS=1900U
MN7 9  4   8   5  MLVNEN W= 576U L=2.0U AD=1200P AS=1200P PD= 10U PS= 576U
.ENDS

.SUBCKT SWITCH3N  2  8  9  40  50
* ANALOG SWITCH
* INPUT = 2   Y = 8  Z = 9  VEE = 40  VCC = 50
MP1 3  2  50  50  MLVPEN W=  88U L=2.0U AD= 350P AS= 350P PD=100U PS=  88U
MN1 3  2  40  40  MLVNEN W=  56U L=2.0U AD= 225P AS= 225P PD= 70U PS=  56U
MP4 4  3  50  50  MLVPEN W= 350U L=2.0U AD= 900P AS= 900P PD=200U PS= 350U
MN4 4  3  40  40  MLVNEN W= 150U L=2.0U AD= 400P AS= 400P PD=100U PS= 150U
MP5 9  3   8  50  MLVPEN W=1168U L=2.0U AD=2730P AS=2730P PD= 10U PS=1168U
MN5 9  4   8  40  MLVNEN W= 312U L=2.0U AD=1200P AS=1200P PD= 10U PS= 312U
.ENDS
```

```
.SUBCKT BUSOUTPN  2   3   4   50   60
* INPUT = 2  OEN = 3 (LOW)  OUT = 4  VCC = 50  GND = 60
* 3-STATE BUS OUTPUT
MP1 5  3  50  50  MLVPEN W= 90U  L=2.0U AD= 360P AS= 360P PD= 30U PS=360U
MN1 5  3  60  60  MLVNEN W= 40U  L=2.0U AD= 160P AS= 160P PD= 20U PS= 40U
MP2 6  2  50  50  MLVPEN W=480U  L=2.0U AD=1800P AS=1800P PD=100U PS=480U
MN2 7  2  60  60  MLVNEN W=240U  L=2.0U AD=1000P AS=1000P PD= 50U PS=240U
MP3 7  3   6  50  MLVPEN W=280U  L=2.0U AD=1120P AS=1120P PD= 55U PS=280U
MN3 7  3  60  60  MLVNEN W=160U  L=2.0U AD= 640P AS= 640P PD= 40U PS=160U
MP4 6  5  50  50  MLVPEN W=240U  L=2.0U AD=1000P AS=1000P PD= 50U PS=240U
MN4 7  5   7  60  MLVNEN W=190U  L=2.0U AD= 760P AS= 760P PD= 45U PS=190U
R1  6  8  200
R2  7  9  200
MP5 4  8  50  50  MLVPEN W=540U  L=2.0U AD=1500P AS=1500P PD=10U PS=540U
MN5 4  9  60  60  MLVNEN W=233U  L=2.0U AD= 750P AS= 750P PD=10U PS=233U
R3  8  10  100
R4  9  11  100
MP6 4  10  50  50  MLVPEN W=540U  L=2.0U AD=1500P AS=1500P PD=10U PS=540U
MN6 4  11  60  60  MLVNEN W=233U  L=2.0U AD= 750P AS= 750P PD=10U PS=233U
R5 10  12  50
R6 11  13  50
MP7 4  12  50  50  MLVPEN W=540U  L=2.0U AD=1500P AS=1500P PD=10U PS=540U
MN7 4  13  60  60  MLVNEN W=233U  L=2.0U AD= 750P AS= 750P PD=10U PS=233U
.ENDS

.SUBCKT OUTPN 2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2 4 100
MP1 3 4 50 50  MLVPEN W=360U L=2.0U AD=400P AS=400P PD=10U PS=180U
MN1 3 4 60 60  MLVNEN W=140U L=2.0U AD=200P AS=300P PD=10U PS=130U
R2  4 5 50
MP2 3 5 50 50  MLVPEN W=360U L=2.0U AD=400P AS=400P PD=10U PS=180U
MN2 3 5 60 60  MLVNEN W=140U L=2.0U AD=200P AS=200P PD=10U PS=130U
R3  5 6 50
MP3 3 6 50 50  MLVPEN W=360U L=2.0U AD=400P AS=400P PD=10U PS=180U
MN3 3 6 60 60  MLVNEN W=140U L=2.0U AD=200P AS=200P PD=10U PS=130U
.ENDS

*********************************************************************
*********************************************************************

******CIR_NOMIN******
.SUBCKT INV0  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP0N
XOUTP 25  30  50  60    OUTPN
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  30   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS
```

```
.SUBCKT INV1  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP1N
XINV  25  35  50  60    INVN
XOUTP 35  40  50  60    OUTPN
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  40   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT INV2  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP2N
XINV  25  35  50  60    INVN
XOUTP 35  40  50  60    OUTPN
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  40   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT INVSMT  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    SMT1N
XINV  25  30  50  60    INVN
XOUTP 30  40  50  60    OUTPN
L1  80  50   3.54NH
L2  60  90   3.54NH
L3   2  20   3.54NH
L4  40   3   3.54NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT NINV1  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP1N
XINV0 25  30  50  60    INVN
XINV1 30  35  50  60    INVN
XOUTP 35  40  50  60    OUTPN
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  40   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS
```

```
.SUBCKT NANDINV 2  5  3  80  90
*INVERTING 2-NAND
*EN = 5, IN = 2, OUT = 3, VCC = 80, GND = 90
XIN1  20  25      50  60   INP2N
XIN2  30  35      50  60   INP2N
XNAND 25  35  36  50  60   NANDN
XOUT  36  40      50  60   OUTPN
L1     2  20   4.28NH
L2     5  30   4.28NH
L3    40   3   6.08NH
L4    80  50   6.08NH
L5    60  90   6.08NH
C1    20  90   1.5P
C2    30  90   1.5P
C3    40  90   1.5P
C4    50  90   1.5P
C5    60  90   1.5P
.ENDS

.SUBCKT SWI1  2  3  4  70  80  90
* INP = 2  Y = 3  Z = 4  VEE = 70  VCC = 80  GND = 90
XINP 20  25  50  60      INP2N
XLC  25  30  40  50  60  LLCN
XAS  30   3   4  40  50  SWITCH1N
L1   80  50   6.08NH
L2   70  40   6.08NH
L3   60  90   6.08NH
L4    2  20   4.28NH
C1   50  90   1.5P
C2   40  90   1.5P
C3   60  90   1.5P
C4   20  90   1.5P
C5   3   90   1.5P
C6   4   90   1.5P
.ENDS

.SUBCKT SWI2  2  3  4  80  90
* INP = 2  Y = 3  Z = 4  VCC = 80  GND = 90
XINP  20  25  50  60      INP2N
XAS   25   8   9  50  60  SWITCH2N
L1   80  50   3.53NH
L2   60  90   3.54NH
L3    2  20   3.53NH
L4    8   3   3.54NH
L5    9   4   3.54NH
C1   50  90   1.5P
C2   60  90   1.5P
C3   20  90   1.5P
C4   3   90   1.5P
C5   4   90   1.5P
.ENDS
```

```
.SUBCKT SWI3  2  3  4  70  80  90
* INP = 2  Y = 3  Z = 4  VEE = 70  VCC = 80  GND = 90
XINP 20  25  50  60      INP1N
XLC  25  30  40  50  60  LLCN
XAS  30   3   4  40  50  SWITCH3N
L1  80  50   5.97NH
L2  70  40   5.97NH
L3  60  90   5.97NH
L4   2  20   4.28NH
C1  50  90   1.5P
C2  40  90   1.5P
C3  60  90   1.5P
C4  20  90   1.5P
C5  3   90   1.5P
C6  4   90   1.5P
.ENDS

.SUBCKT NINV3  2  5  3  80  90
* INP = 2  OEN = 5(LOW)  OUT = 3   VCC = 80  GND = 90
XINP      20  25  50  60      INP2N
XINV      25  30  50  60      INVN
XBUSOUTP  30  15  35  50  60  BUSOUTPN
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   6.87NH
L4   5  15   5.97NH
L5  35   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C4  20  90   1.5P
C5  15  90   1.5P
C6   3  90   1.5P
.ENDS

************************************************************
```

LVFAST.CIR Subcircuit

```
* LV Subcircuit and Primitive Elements Library
* LVFAST.CIR
* Fast Process Corner
* Standard Logic Product Group
* Philips Semiconductors
* 3/28/95
**********************************************
*            FAST N-Channel Transistor       *
*             UCB-3 Parameter Set            *
*          LOW VOLTAGE CMOS Logic Family     *
*                10-Jan.-1995                *
**********************************************
.Model MLVNEF NMOS
+LEVEL = 3
+KP    = 78E-6
+VTO   = 0.31
+TOX   = 28.5E-9
+NSUB  = 4.0E15
+GAMMA = 0.74
+PHI   = 0.65
+VMAX  = 135E3
+RS    = 20
+RD    = 20
+XJ    = 0.10E-6
+LD    = 0.55E-6
+DELTA = 0.38
+THETA = 0.048
+ETA   = 0.010
+KAPPA = 0.0
+WD    = 0.5E-6

**********************************************
*          FAST P-Channel transistor         *
*           UCB-3 Parameter Set              *
*          LOW VOLTAGE CMOS Logic Family     *
*                10-Jan.-1995                *
**********************************************
.Model MLVPEF PMOS
+LEVEL = 3
+KP    = 26.1E-6
+VTO   = -0.46
+TOX   = 28.5E-9
+NSUB  = 3.6E16
+GAMMA = 0.82
+PHI   = 0.65
+VMAX  = 600E3
+RS    = 40
+RD    = 40
+XJ    = 0.61E-6
+LD    = 0.30E-6
+DELTA = 2.12
+THETA = 0.100
+ETA   = 0.260
+KAPPA = 0.0
+WD    = 0.5E-6
```

```
****************************************
*   START OF SUB-CIRCUIT DESCRIPTION   *
*           MARCH 28, 1995             *
****************************************

*****FAST.CIR*****
.SUBCKT INP0F  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2  3  100
MP1 3 50 50 50  MLVPEF W=20U L=2.0U AD=100P AS=100P PD=40U PS= 20U
MN1 3 60 60 60  MLVNEF W=35U L=2.0U AD=260P AS=260P PD=70U PS= 20U
.ENDS

.SUBCKT INP1F  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MLVPEF W=20U L=2.0U AD=100P AS=100P PD=40U PS= 20U
MN1 4 60 60 60  MLVNEF W=35U L=2.0U AD=260P AS=260P PD=70U PS= 20U
MP2 3  4 50 50  MLVPEF W=88U L=2.0U AD=290P AS=550P PD=10U PS=100U
MN2 3  4 60 60  MLVNEF W=56U L=2.0U AD=162P AS=550P PD=10U PS= 75U
.ENDS

.SUBCKT INP2F  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MLVPEF W= 20U L=2.0U AD= 100P AS=100P PD= 40U PS= 20U
MN1 4 60 60 60  MLVNEF W= 35U L=2.0U AD= 260P AS=260P PD= 70U PS= 20U
MP2 3  4 50 50  MLVPEF W=176U L=2.0U AD= 580P AS=1000P PD=10U PS=200U
MN2 3  4 60 60  MLVNEF W=112U L=2.0U AD= 325P AS=1000P PD=10U PS=150U
.ENDS

.SUBCKT SMT1F  2  3  50  60
* SCHMITT-TRIGGER INPUT FOR LV14 CMOS INPUT LEVELS
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MLVPEF W=20U L=2.0U AD=100P AS=100P PD=40U PS=20U
MN1 4 60 60 60  MLVNEF W=35U L=2.0U AD=140P AS=140P PD=50U PS=35U
MP2 5  4 50 50  MLVPEF W=36U L=2.0U AD=140P AS=140P PD=50U PS=35U
MN2 6  4 60 60  MLVNEF W=16U L=2.0U AD= 70P AS= 70P PD=15U PS=17U
MP3 3  4  5 50  MLVPEF W=44U L=4.0U AD=220P AS=220P PD=60U PS=44U
MN3 3  4  6  6  MLVNEF W=17U L=2.0U AD= 70P AS= 70P PD=15U PS=16U
MP4 5  3 60 50  MLVPEF W=36U L=2.0U AD=150P AS=150P PD=60U PS=36U
MN4 6  3 50  6  MLVNEF W= 6U L=4.0U AD= 25P AS= 25P PD=10U PS= 6U
.ENDS

.SUBCKT INVF   2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
MP1 3  2 50 50  MLVPEF W=364U L=2.0U AD=500P  AS=500P PD=10U PS=430U
MN1 3  2 60 60  MLVNEF W=184U L=2.0U AD=275P  AS=275P PD=10U PS=270U
.ENDS

.SUBCKT NANDF  2  3  4  50  60
*INTERNAL NAND
*IN1 = 2, IN2 = 3, OUT = 4, VCC= 50, GND = 60
MP1 4  2  50  50  MLVPEF W=112U  L=2.0U AD=150P AS=300P PD= 75U PS=150U
MP2 4  3  50  50  MLVPEF W=112U  L=2.0U AD=150P AS=300P PD= 75U PS=150U
MN1 4  2   5  60  MLVNEF W=300U  L=2.0U AD=300P AS=300P PD=300U PS=300U
MN2 5  3  60  60  MLVNEF W=300U  L=2.0U AD=300P AS=300P PD=300U PS=300U
.ENDS
```

```
.SUBCKT LLCF  2  3  40  50  60
* LEVEL CONVERTER
* INA = 2,  OUT = 3,  VEE = 40,  VCC = 50,  GND =  60
MP4 4  2  50  50  MLVPEF W= 30U  L= 2.4U AD=120P AS=120P PD= 40U PS= 30U
MN4 4  2  60  60  MLVNEF W= 15U  L= 2.4U AD= 60P AS= 60P PD= 20U PS= 15U
MP1 5  2  50  50  MLVPEF W=135U  L= 2.4U AD=500P AS=500P PD=100U PS=135U
MP2 6  2  50  50  MLVPEF W=135U  L= 2.4U AD=500P AS=500P PD=100U PS=135U
MN1 5  6  40  40  MLVNEF W=6.4U  L=18.8U AD= 25P AS= 25P PD= 20U PS=6.4U
MN2 6  5  40  40  MLVNEF W=6.4U  L=18.8U AD= 25P AS= 25P PD= 20U PS=6.4U
MP3 7  6  50  50  MLVPEF W= 10U  L= 4.0U AD= 40P AS= 40P PD= 20U PS= 10U
MN3 7  6  40  40  MLVNEF W=  5U  L= 4.0U AD= 20P AS= 20P PD= 10U PS=  5U
MP5 3  7  50  50  MLVPEF W= 30U  L= 2.4U AD=120P AS=120P PD= 40U PS= 30U
MN5 3  7  40  40  MLVNEF W= 15U  L= 2.4U AD= 60P AS= 60P PD= 20U PS= 15U
.ENDS

.SUBCKT SWITCH1F  2  8  9  40  50
* ANALOG SWITCH
* INPUT = 2   Y = 8  Z = 9  VEE = 40  VCC =50
MP1 3  2  50  50  MLVPEF W=  88U L=2.0U AD= 350P AS= 350P PD=100U PS=  88U
MN1 3  2  40  40  MLVNEF W=  56U L=2.0U AD= 225P AS= 225P PD= 70U PS=  56U
MP4 4  3  50  50  MLVPEF W= 350U L=2.0U AD= 900P AS= 900P PD=200U PS= 350U
MN4 4  3  40  40  MLVNEF W= 150U L=2.0U AD= 400P AS= 400P PD=100U PS= 150U
MP5 8  4   5  50  MLVPEF W= 216U L=2.0U AD= 900P AS= 900P PD=100U PS= 216U
MN5 8  3   5   5  MLVNEF W= 108U L=2.0U AD= 430P AS= 430P PD= 50U PS= 108U
MN6 5  4  40  40  MLVNEF W= 145U L=2.0U AD= 600P AS= 600P PD= 75U PS= 145U
MP7 9  4   8  50  MLVPEF W=1068U L=2.0U AD=2500P AS=2500P PD= 10U PS=1068U
MN7 9  3   8   5  MLVNEF W= 312U L=2.0U AD=1200P AS=1200P PD= 10U PS= 312U
.ENDS

.SUBCKT SWITCH2F  2  8  9  50  60
* ANALOG SWITCH
* INPUT= 2   Y= 8   Z= 9  VCC= 50   GND= 60
MP1 3  2  50  50  MLVPEF W=  88U L=2.0U AD= 350P AS= 350P PD=100U PS=  88U
MN1 3  2  60  60  MLVNEF W=  56U L=2.0U AD= 225P AS= 225P PD= 70U PS=  56U
MP4 4  3  50  50  MLVPEF W= 350U L=2.0U AD= 900P AS= 900P PD=200U PS= 350U
MN4 4  3  60  60  MLVNEF W= 150U L=2.0U AD= 400P AS= 400P PD=100U PS= 150U
MP5 5  3   8  50  MLVPEF W=  85U L=2.0U AD= 355P AS= 355P PD= 40U PS=  85U
MN5 5  4   8   5  MLVNEF W=  42U L=2.0U AD= 170P AS= 170P PD= 20U PS=  42U
MN6 5  3  60  60  MLVNEF W= 145U L=2.0U AD= 600P AS= 600P PD= 75U PS= 145U
MP7 9  3   8  50  MLVPEF W=1900U L=2.0U AD=2500P AS=2500P PD= 10U PS=1900U
MN7 9  4   8   5  MLVNEF W= 576U L=2.0U AD=1200P AS=1200P PD= 10U PS= 576U
.ENDS

.SUBCKT SWITCH3F  2  8  9  40  50
* ANALOG SWITCH
* INPUT = 2   Y = 8  Z = 9  VEE = 40  VCC = 50
MP1 3  2  50  50  MLVPEF W=  88U L=2.0U AD= 350P AS= 350P PD=100U PS=  88U
MN1 3  2  40  40  MLVNEF W=  56U L=2.0U AD= 225P AS= 225P PD= 70U PS=  56U
MP4 4  3  50  50  MLVPEF W= 350U L=2.0U AD= 900P AS= 900P PD=200U PS= 350U
MN4 4  3  40  40  MLVNEF W= 150U L=2.0U AD= 400P AS= 400P PD=100U PS= 150U
MP5 9  3   8  50  MLVPEF W=1168U L=2.0U AD=2730P AS=2730P PD= 10U PS=1168U
MN5 9  4   8  40  MLVNEF W= 312U L=2.0U AD=1200P AS=1200P PD= 10U PS= 312U
.ENDS
```

```
.SUBCKT BUSOUTPF  2   3   4   50   60
* INPUT = 2  OEN = 3 (LOW)  OUT = 4  VCC = 50  GND = 60
* 3-STATE BUS OUTPUT
MP1 5  3  50  50  MLVPEF W= 90U  L=2.0U AD= 360P AS= 360P PD= 30U PS=360U
MN1 5  3  60  60  MLVNEF W= 40U  L=2.0U AD= 160P AS= 160P PD= 20U PS= 40U
MP2 6  2  50  50  MLVPEF W=480U  L=2.0U AD=1800P AS=1800P PD=100U PS=480U
MN2 7  2  60  60  MLVNEF W=240U  L=2.0U AD=1000P AS=1000P PD= 50U PS=240U
MP3 7  3   6  50  MLVPEF W=280U  L=2.0U AD=1120P AS=1120P PD= 55U PS=280U
MN3 7  3  60  60  MLVNEF W=160U  L=2.0U AD= 640P AS= 640P PD= 40U PS=160U
MP4 6  5  50  50  MLVPEF W=240U  L=2.0U AD=1000P AS=1000P PD= 50U PS=240U
MN4 7  5   7  60  MLVNEF W=190U  L=2.0U AD= 760P AS= 760P PD= 45U PS=190U
R1  6  8  200
R2  7  9  200
MP5 4  8  50  50  MLVPEF W=540U  L=2.0U AD=1500P AS=1500P PD=10U PS=540U
MN5 4  9  60  60  MLVNEF W=233U  L=2.0U AD= 750P AS= 750P PD=10U PS=233U
R3  8  10  100
R4  9  11  100
MP6 4  10  50  50  MLVPEF W=540U  L=2.0U AD=1500P AS=1500P PD=10U PS=540U
MN6 4  11  60  60  MLVNEF W=233U  L=2.0U AD= 750P AS= 750P PD=10U PS=233U
R5 10  12  50
R6 11  13  50
MP7 4  12  50  50  MLVPEF W=540U  L=2.0U AD=1500P AS=1500P PD=10U PS=540U
MN7 4  13  60  60  MLVNEF W=233U  L=2.0U AD= 750P AS= 750P PD=10U PS=233U
.ENDS

.SUBCKT OUTPF 2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2 4 100
MP1 3 4 50 50  MLVPEF W=360U L=2.0U AD=400P AS=400P PD=10U PS=180U
MN1 3 4 60 60  MLVNEF W=140U L=2.0U AD=200P AS=300P PD=10U PS=130U
R2  4 5 50
MP2 3 5 50 50  MLVPEF W=360U L=2.0U AD=400P AS=400P PD=10U PS=180U
MN2 3 5 60 60  MLVNEF W=140U L=2.0U AD=200P AS=200P PD=10U PS=130U
R3  5 6 50
MP3 3 6 50 50  MLVPEF W=360U L=2.0U AD=400P AS=400P PD=10U PS=180U
MN3 3 6 60 60  MLVNEF W=140U L=2.0U AD=200P AS=200P PD=10U PS=130U
.ENDS

**********************************************************************
**********************************************************************

******CIR_FAST******
.SUBCKT INV0  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP0F
XOUTP 25  30  50  60    OUTPF
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  30   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS
```

```
.SUBCKT INV1  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP1F
XINV  25  35  50  60    INVF
XOUTP 35  40  50  60    OUTPF
L1   80  50   6.87NH
L2   60  90   6.87NH
L3    2  20   5.97NH
L4   40   3   5.97NH
C1   50  90   1.5P
C2   60  90   1.5P
C3   20  90   1.5P
C4   3   90   1.5P
.ENDS

.SUBCKT INV2  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP2F
XINV  25  35  50  60    INVF
XOUTP 35  40  50  60    OUTPF
L1   80  50   6.87NH
L2   60  90   6.87NH
L3    2  20   5.97NH
L4   40   3   5.97NH
C1   50  90   1.5P
C2   60  90   1.5P
C3   20  90   1.5P
C4   3   90   1.5P
.ENDS

.SUBCKT INVSMT  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    SMT1F
XINV  25  30  50  60    INVF
XOUTP 30  40  50  60    OUTPF
L1   80  50   3.54NH
L2   60  90   3.54NH
L3    2  20   3.54NH
L4   40   3   3.54NH
C1   50  90   1.5P
C2   60  90   1.5P
C3   20  90   1.5P
C4   3   90   1.5P
.ENDS

.SUBCKT NINV1  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP1F
XINV0 25  30  50  60    INVF
XINV1 30  35  50  60    INVF
XOUTP 35  40  50  60    OUTPF
L1   80  50   6.87NH
L2   60  90   6.87NH
L3    2  20   5.97NH
L4   40   3   5.97NH
C1   50  90   1.5P
C2   60  90   1.5P
C3   20  90   1.5P
C4   3   90   1.5P
.ENDS
```

```
.SUBCKT NANDINV 2  5  3  80  90
*INVERTING 2-NAND
*EN = 5, IN = 2, OUT = 3, VCC = 80, GND = 90
XIN1  20  25      50  60   INP2F
XIN2  30  35      50  60   INP2F
XNAND 25  35  36  50  60   NANDF
XOUT  36  40      50  60   OUTPF
L1     2  20   4.28NH
L2     5  30   4.28NH
L3    40   3   6.08NH
L4    80  50   6.08NH
L5    60  90   6.08NH
C1    20  90   1.5P
C2    30  90   1.5P
C3    40  90   1.5P
C4    50  90   1.5P
C5    60  90   1.5P
.ENDS

.SUBCKT SWI1  2  3  4  70  80  90
* INP = 2  Y = 3  Z = 4  VEE = 70  VCC = 80  GND = 90
XINP 20  25  50  60      INP2F
XLC  25  30  40  50  60  LLCF
XAS  30   3   4  40  50  SWITCH1F
L1  80  50   6.08NH
L2  70  40   6.08NH
L3  60  90   6.08NH
L4   2  20   4.28NH
C1  50  90   1.5P
C2  40  90   1.5P
C3  60  90   1.5P
C4  20  90   1.5P
C5  3   90   1.5P
C6  4   90   1.5P
.ENDS

.SUBCKT SWI2  2  3  4  80  90
* INP = 2  Y = 3  Z = 4  VCC = 80  GND = 90
XINP  20  25  50  60      INP2F
XAS   25   8   9  50  60  SWITCH2F
L1  80  50   3.53NH
L2  60  90   3.54NH
L3   2  20   3.53NH
L4   8   3   3.54NH
L5   9   4   3.54NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
C5  4   90   1.5P
.ENDS
```

```
.SUBCKT SWI3  2  3  4  70  80  90
* INP = 2  Y = 3  Z = 4  VEE = 70  VCC = 80  GND = 90
XINP 20  25  50  60      INP1F
XLC  25  30  40  50  60  LLCF
XAS  30   3   4  40  50  SWITCH3F
L1   80  50   5.97NH
L2   70  40   5.97NH
L3   60  90   5.97NH
L4    2  20   4.28NH
C1   50  90   1.5P
C2   40  90   1.5P
C3   60  90   1.5P
C4   20  90   1.5P
C5   3   90   1.5P
C6   4   90   1.5P
.ENDS

.SUBCKT NINV3  2  5  3  80  90
* INP = 2  OEN = 5(LOW)  OUT = 3  VCC = 80  GND = 90
XINP      20  25  50  60      INP2F
XINV      25  30  50  60      INVF
XBUSOUTP  30  15  35  50  60  BUSOUTPF
L1   80  50   6.87NH
L2   60  90   6.87NH
L3    2  20   6.87NH
L4    5  15   5.97NH
L5   35   3   5.97NH
C1   50  90   1.5P
C2   60  90   1.5P
C4   20  90   1.5P
C5   15  90   1.5P
C6    3  90   1.5P
.ENDS

************************************************************
```

LVSLOW.CIR Subcircuit

```
* LV Subcircuit and Primitive Elements Library
* LVSLOW.CIR
* Slow Process Corner
* Standard Logic Product Group
* Philips Semiconductors
* 3/28/95
************************************************
*          SLOW N-Channel Transistor           *
*            UCB-3 Parameter Set               *
*         LOW VOLTAGE CMOS Logic Family        *
*                10-Jan.-1995                  *
************************************************
.Model MLVNES NMOS
+LEVEL = 3
+KP    = 52.0E-6
+VTO   = 0.610
+TOX   = 31.5E-9
+NSUB  = 2.0E15
+GAMMA = 1.14
+PHI   = 0.65
+VMAX  = 175E3
+RS    = 40
+RD    = 40
+XJ    = 0.12E-6
+LD    = 0.25E-6
+DELTA = 0.25
+THETA = 0.060
+ETA   = 0.020
+KAPPA = 0.0
+WD    = -0.5E-6

************************************************
*          SLOW P-Channel transistor           *
*           UCB-3 Parameter Set                *
*         LOW VOLTAGE CMOS Logic Family        *
*               10-Jan.-1995                   *
************************************************
.Model MLVPES PMOS
+LEVEL = 3
+KP    = 14.5E-6
+VTO   = -0.76
+TOX   = 31.5E-9
+NSUB  = 3.0E16
+GAMMA = 1.02
+PHI   = 0.65
+VMAX  = 180E4
+RS    = 80
+RD    = 80
+XJ    = 0.65E-6
+LD    = 0.0E-6
+DELTA = 2.35
+THETA = 0.120
+ETA   = 0.380
+KAPPA = 0.0
+WD    = -0.5E-6
```

```
****************************************
*   START OF SUB-CIRCUIT DESCRIPTION   *
*            MARCH 28, 1995            *
****************************************

*****SLOW.CIR*****

.SUBCKT INP0S  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2  3  100
MP1 3 50 50 50  MLVPES W=20U L=2.0U AD=100P AS=100P PD=40U PS= 20U
MN1 3 60 60 60  MLVNES W=35U L=2.0U AD=260P AS=260P PD=70U PS= 20U
.ENDS

.SUBCKT INP1S  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MLVPES W=20U L=2.0U AD=100P AS=100P PD=40U PS= 20U
MN1 4 60 60 60  MLVNES W=35U L=2.0U AD=260P AS=260P PD=70U PS= 20U
MP2 3  4 50 50  MLVPES W=88U L=2.0U AD=290P AS=550P PD=10U PS=100U
MN2 3  4 60 60  MLVNES W=56U L=2.0U AD=162P AS=550P PD=10U PS= 75U
.ENDS

.SUBCKT INP2S  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MLVPES W= 20U L=2.0U AD= 100P AS=100P PD= 40U PS= 20U
MN1 4 60 60 60  MLVNES W= 35U L=2.0U AD= 260P AS=260P PD= 70U PS= 20U
MP2 3  4 50 50  MLVPES W=176U L=2.0U AD= 580P AS=1000P PD=10U PS=200U
MN2 3  4 60 60  MLVNES W=112U L=2.0U AD= 325P AS=1000P PD=10U PS=150U
.ENDS

.SUBCKT SMT1S  2  3  50  60
* SCHMITT-TRIGGER INPUT FOR LV14 CMOS INPUT LEVELS
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MLVPES W=20U L=2.0U AD=100P AS=100P PD=40U PS=20U
MN1 4 60 60 60  MLVNES W=35U L=2.0U AD=140P AS=140P PD=50U PS=35U
MP2 5  4 50 50  MLVPES W=36U L=2.0U AD=140P AS=140P PD=50U PS=35U
MN2 6  4 60 60  MLVNES W=16U L=2.0U AD= 70P AS= 70P PD=15U PS=17U
MP3 3  4  5 50  MLVPES W=44U L=4.0U AD=220P AS=220P PD=60U PS=44U
MN3 3  4  6  6  MLVNES W=17U L=2.0U AD= 70P AS= 70P PD=15U PS=16U
MP4 5  3 60 50  MLVPES W=36U L=2.0U AD=150P AS=150P PD=60U PS=36U
MN4 6  3 50  6  MLVNES W= 6U L=4.0U AD= 25P AS= 25P PD=10U PS= 6U
.ENDS

.SUBCKT INVS   2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
MP1 3  2 50 50  MLVPES W=364U L=2.0U AD=500P  AS=500P PD=10U PS=430U
MN1 3  2 60 60  MLVNES W=184U L=2.0U AD=275P  AS=275P PD=10U PS=270U
.ENDS

.SUBCKT NANDS  2  3  4  50  60
*INTERNAL NAND
*IN1 = 2, IN2 = 3, OUT = 4, VCC= 50, GND = 60
MP1 4  2  50  50  MLVPES W=112U  L=2.0U AD=150P AS=300P PD= 75U PS=150U
MP2 4  3  50  50  MLVPES W=112U  L=2.0U AD=150P AS=300P PD= 75U PS=150U
MN1 4  2   5  60  MLVNES W=300U  L=2.0U AD=300P AS=300P PD=300U PS=300U
MN2 5  3  60  60  MLVNES W=300U  L=2.0U AD=300P AS=300P PD=300U PS=300U
.ENDS
```

```
.SUBCKT LLCS  2  3  40  50  60
* LEVEL CONVERTER
* INA = 2,  OUT = 3,  VEE = 40,  VCC = 50,  GND =  60
MP4 4  2  50  50  MLVPES W= 30U  L= 2.4U AD=120P AS=120P PD= 40U PS= 30U
MN4 4  2  60  60  MLVNES W= 15U  L= 2.4U AD= 60P AS= 60P PD= 20U PS= 15U
MP1 5  2  50  50  MLVPES W=135U  L= 2.4U AD=500P AS=500P PD=100U PS=135U
MP2 6  2  50  50  MLVPES W=135U  L= 2.4U AD=500P AS=500P PD=100U PS=135U
MN1 5  6  40  40  MLVNES W=6.4U  L=18.8U AD= 25P AS= 25P PD= 20U PS=6.4U
MN2 6  5  40  40  MLVNES W=6.4U  L=18.8U AD= 25P AS= 25P PD= 20U PS=6.4U
MP3 7  6  50  50  MLVPES W= 10U  L= 4.0U AD= 40P AS= 40P PD= 20U PS= 10U
MN3 7  6  40  40  MLVNES W=  5U  L= 4.0U AD= 20P AS= 20P PD= 10U PS=  5U
MP5 3  7  50  50  MLVPES W= 30U  L= 2.4U AD=120P AS=120P PD= 40U PS= 30U
MN5 3  7  40  40  MLVNES W= 15U  L= 2.4U AD= 60P AS= 60P PD= 20U PS= 15U
.ENDS

.SUBCKT SWITCH1S  2  8  9  40  50
* ANALOG SWITCH
* INPUT = 2   Y = 8  Z = 9  VEE = 40  VCC =50
MP1 3  2  50  50  MLVPES W=  88U L=2.0U AD= 350P AS= 350P PD=100U PS=  88U
MN1 3  2  40  40  MLVNES W=  56U L=2.0U AD= 225P AS= 225P PD= 70U PS=  56U
MP4 4  3  50  50  MLVPES W= 350U L=2.0U AD= 900P AS= 900P PD=200U PS= 350U
MN4 4  3  40  40  MLVNES W= 150U L=2.0U AD= 400P AS= 400P PD=100U PS= 150U
MP5 8  4   5  50  MLVPES W= 216U L=2.0U AD= 900P AS= 900P PD=100U PS= 216U
MN5 8  3   5   5  MLVNES W= 108U L=2.0U AD= 430P AS= 430P PD= 50U PS= 108U
MN6 5  4  40  40  MLVNES W= 145U L=2.0U AD= 600P AS= 600P PD= 75U PS= 145U
MP7 9  4   8  50  MLVPES W=1068U L=2.0U AD=2500P AS=2500P PD= 10U PS=1068U
MN7 9  3   8   5  MLVNES W= 312U L=2.0U AD=1200P AS=1200P PD= 10U PS= 312U
.ENDS

.SUBCKT SWITCH2S  2  8  9  50  60
* ANALOG SWITCH
* INPUT= 2   Y= 8   Z= 9  VCC= 50   GND= 60
MP1 3  2  50  50  MLVPES W=  88U L=2.0U AD= 350P AS= 350P PD=100U PS=  88U
MN1 3  2  60  60  MLVNES W=  56U L=2.0U AD= 225P AS= 225P PD= 70U PS=  56U
MP4 4  3  50  50  MLVPES W= 350U L=2.0U AD= 900P AS= 900P PD=200U PS= 350U
MN4 4  3  60  60  MLVNES W= 150U L=2.0U AD= 400P AS= 400P PD=100U PS= 150U
MP5 5  3   8  50  MLVPES W=  85U L=2.0U AD= 355P AS= 355P PD= 40U PS=  85U
MN5 5  4   8   5  MLVNES W=  42U L=2.0U AD= 170P AS= 170P PD= 20U PS=  42U
MN6 5  3  60  60  MLVNES W= 145U L=2.0U AD= 600P AS= 600P PD= 75U PS= 145U
MP7 9  3   8  50  MLVPES W=1900U L=2.0U AD=2500P AS=2500P PD= 10U PS=1900U
MN7 9  4   8   5  MLVNES W= 576U L=2.0U AD=1200P AS=1200P PD= 10U PS= 576U
.ENDS

.SUBCKT SWITCH3S  2  8  9  40  50
* ANALOG SWITCH
* INPUT = 2   Y = 8  Z = 9  VEE = 40  VCC = 50
MP1 3  2  50  50  MLVPES W=  88U L=2.0U AD= 350P AS= 350P PD=100U PS=  88U
MN1 3  2  40  40  MLVNES W=  56U L=2.0U AD= 225P AS= 225P PD= 70U PS=  56U
MP4 4  3  50  50  MLVPES W= 350U L=2.0U AD= 900P AS= 900P PD=200U PS= 350U
MN4 4  3  40  40  MLVNES W= 150U L=2.0U AD= 400P AS= 400P PD=100U PS= 150U
MP5 9  3   8  50  MLVPES W=1168U L=2.0U AD=2730P AS=2730P PD= 10U PS=1168U
MN5 9  4   8  40  MLVNES W= 312U L=2.0U AD=1200P AS=1200P PD= 10U PS= 312U
.ENDS
```

```
.SUBCKT BUSOUTPS  2   3   4   50   60
* INPUT = 2  OEN = 3 (LOW)  OUT = 4  VCC = 50  GND = 60
* 3-STATE BUS OUTPUT
MP1 5  3  50  50  MLVPES W= 90U  L=2.0U AD= 360P AS= 360P PD= 30U PS=360U
MN1 5  3  60  60  MLVNES W= 40U  L=2.0U AD= 160P AS= 160P PD= 20U PS= 40U
MP2 6  2  50  50  MLVPES W=480U  L=2.0U AD=1800P AS=1800P PD=100U PS=480U
MN2 7  2  60  60  MLVNES W=240U  L=2.0U AD=1000P AS=1000P PD= 50U PS=240U
MP3 7  3   6  50  MLVPES W=280U  L=2.0U AD=1120P AS=1120P PD= 55U PS=280U
MN3 7  3  60  60  MLVNES W=160U  L=2.0U AD= 640P AS= 640P PD= 40U PS=160U
MP4 6  5  50  50  MLVPES W=240U  L=2.0U AD=1000P AS=1000P PD= 50U PS=240U
MN4 7  5   7  60  MLVNES W=190U  L=2.0U AD= 760P AS= 760P PD= 45U PS=190U
R1  6  8  200
R2  7  9  200
MP5 4  8  50  50  MLVPES W=540U  L=2.0U AD=1500P AS=1500P PD=10U PS=540U
MN5 4  9  60  60  MLVNES W=233U  L=2.0U AD= 750P AS= 750P PD=10U PS=233U
R3  8  10  100
R4  9  11  100
MP6 4  10  50  50  MLVPES W=540U  L=2.0U AD=1500P AS=1500P PD=10U PS=540U
MN6 4  11  60  60  MLVNES W=233U  L=2.0U AD= 750P AS= 750P PD=10U PS=233U
R5 10  12  50
R6 11  13  50
MP7 4  12  50  50  MLVPES W=540U  L=2.0U AD=1500P AS=1500P PD=10U PS=540U
MN7 4  13  60  60  MLVNES W=233U  L=2.0U AD= 750P AS= 750P PD=10U PS=233U
.ENDS

.SUBCKT OUTPS  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2 4 100
MP1 3 4 50 50  MLVPES W=360U L=2.0U AD=400P AS=400P PD=10U PS=180U
MN1 3 4 60 60  MLVNES W=140U L=2.0U AD=200P AS=300P PD=10U PS=130U
R2  4 5 50
MP2 3 5 50 50  MLVPES W=360U L=2.0U AD=400P AS=400P PD=10U PS=180U
MN2 3 5 60 60  MLVNES W=140U L=2.0U AD=200P AS=200P PD=10U PS=130U
R3  5 6 50
MP3 3 6 50 50  MLVPES W=360U L=2.0U AD=400P AS=400P PD=10U PS=180U
MN3 3 6 60 60  MLVNES W=140U L=2.0U AD=200P AS=200P PD=10U PS=130U
.ENDS

*********************************************************************
*********************************************************************

******CIR_SLOW******

.SUBCKT INV0  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP0S
XOUTP 25  30  50  60    OUTPS
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  30   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS
```

```
.SUBCKT INV1  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP1S
XINV  25  35  50  60    INVS
XOUTP 35  40  50  60    OUTPS
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  40   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT INV2  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP2S
XINV  25  35  50  60    INVS
XOUTP 35  40  50  60    OUTPS
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  40   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT INVSMT  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    SMT1S
XINV  25  30  50  60    INVS
XOUTP 30  40  50  60    OUTPS
L1  80  50   3.54NH
L2  60  90   3.54NH
L3   2  20   3.54NH
L4  40   3   3.54NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT NINV1  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP1S
XINV0 25  30  50  60    INVS
XINV1 30  35  50  60    INVS
XOUTP 35  40  50  60    OUTPS
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  40   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS
```

```
.SUBCKT NANDINV 2  5  3  80  90
*INVERTING 2-NAND
*EN = 5, IN = 2, OUT = 3, VCC = 80, GND = 90
XIN1   20  25      50  60   INP2S
XIN2   30  35      50  60   INP2S
XNAND  25  35  36  50  60   NANDS
XOUT   36  40      50  60   OUTPS
L1      2  20   4.28NH
L2      5  30   4.28NH
L3     40   3   6.08NH
L4     80  50   6.08NH
L5     60  90   6.08NH
C1     20  90   1.5P
C2     30  90   1.5P
C3     40  90   1.5P
C4     50  90   1.5P
C5     60  90   1.5P
.ENDS

.SUBCKT SWI1  2  3  4  70  80  90
* INP = 2  Y = 3  Z = 4  VEE = 70  VCC = 80  GND = 90
XINP 20  25  50  60      INP2S
XLC  25  30  40  50  60  LLCS
XAS  30   3   4  40  50  SWITCH1S
L1   80  50   6.08NH
L2   70  40   6.08NH
L3   60  90   6.08NH
L4    2  20   4.28NH
C1   50  90   1.5P
C2   40  90   1.5P
C3   60  90   1.5P
C4   20  90   1.5P
C5   3   90   1.5P
C6   4   90   1.5P
.ENDS

.SUBCKT SWI2  2  3  4  80  90
* INP = 2  Y = 3  Z = 4  VCC = 80  GND = 90
XINP  20  25  50  60      INP2S
XAS   25   8   9  50  60  SWITCH2S
L1   80  50   3.53NH
L2   60  90   3.54NH
L3    2  20   3.53NH
L4    8   3   3.54NH
L5    9   4   3.54NH
C1   50  90   1.5P
C2   60  90   1.5P
C3   20  90   1.5P
C4   3   90   1.5P
C5   4   90   1.5P
.ENDS
```

```
.SUBCKT SWI3  2  3  4  70  80  90
* INP = 2  Y = 3  Z = 4  VEE = 70  VCC = 80  GND = 90
XINP 20  25  50  60       INP1S
XLC  25  30  40  50  60   LLCS
XAS  30   3   4  40  50   SWITCH3S
L1   80  50   5.97NH
L2   70  40   5.97NH
L3   60  90   5.97NH
L4    2  20   4.28NH
C1   50  90   1.5P
C2   40  90   1.5P
C3   60  90   1.5P
C4   20  90   1.5P
C5   3   90   1.5P
C6   4   90   1.5P
.ENDS

.SUBCKT NINV3  2  5  3  80  90
* INP = 2  OEN = 5(LOW)  OUT = 3  VCC = 80  GND = 90
XINP       20  25  50  60       INP2S
XINV       25  30  50  60       INVS
XBUSOUTP   30  15  35  50  60   BUSOUTPS
L1   80  50   6.87NH
L2   60  90   6.87NH
L3    2  20   6.87NH
L4    5  15   5.97NH
L5   35   3   5.97NH
C1   50  90   1.5P
C2   60  90   1.5P
C4   20  90   1.5P
C5   15  90   1.5P
C6    3  90   1.5P
.ENDS

************************************************************
```

Section 10
HCMOS

SPICE

CONTENTS

Each HCMOS device requires some combination of one or two input stages, an output stage, possibly one or two inverting stages, possibly a NAND stage, and some package parasitics. Switch part types have an input stage, possibly a level converter, and an analog switch. Table 10-1 shows LV model combinations that correlate the various subcircuit structures for each part type. Dashes indicate that a particular stage is not needed.

Table 10-1. HCMOS Model Combinations

HC(T)	Input Circuit	Inverter Circuit	NAND Circuit	Output Circuit	Level Converter	Analog Switch	Subcircuit Name
00	INP2(T)	INV	–	OUTP	–	–	INV2(T)
04	INP0	–	–	OUTP	–	–	INV0(T)
14	SMT1/SMTTL1	INV	–	OUTP	–	–	INVSMT(T)
32	INP1(T)	INV/INV	–	OUTP	–	–	NINV1(T)
74	INP1(T)	INV	–	OUTP	–	–	INV1(T)
123	INP1(T)	INV	–	OUTP	–	–	INV1(T)
132	SMT1/SMTTL1	INV	–	OUTP	–	–	INVSMT(T)
138	2–INP2(T)	–	NAND	OUTP	–	–	NANDINV(T)
161	INP2(T)	INV	–	OUTP	–	–	INV2(T)
163	INP2(T)	INV	–	OUTP	–	–	INV2(T)
244	INP2(T)	INV	–	BUSOUTP	–	–	NINV3(T)
245	INP2(T)	INV	–	BUSOUTP	–	–	NINV3(T)
273	INP1(T)	INV/INV		OUTP	–	–	NINV1(T)
373	INP2(T)	INV	–	BUSOUTP	–	–	NINV3(T)
374	INP2(T)	INV	–	BUSOUTP	–	–	NINV3(T)
595	INP2(T)	INV	–	BUSOUTP	–	–	NINV3(T)
4040	INP1(T)	INV/INV	–	OUTP	–	–	NINV1(T)
4051	INP2(T)	–	–	–	LLC	SWITCH1	SWI1(T)
4052	INP2(T)	–	–	–	LLC	SWITCH1	SWI1(T)
4053	INP2(T)	–	–	–	LLC	SWITCH1	SWI1(T)
4066	INP2(T)	–	–	–	–	SWITCH2	SWI2(T)
4316	INP1(T)	–	–	–	LLC	SWITCH3	SWI3(T)
4538	INP1(T)	INV	–	OUTP	–	–	INVSMT(T)

The data sheet section provides reference information on the part types if needed. Each data sheet contains a part description, part features, quick reference data, ordering information, pin configuration, logic symbol or diagram, and function table.

To do simulations on a particular part type, refer to the HCMOS Netlists section of the book. That section has a file called "HCT.CIR" that contains simulation test circuits for individual device types. The file is also in the HCMOS directory in the attached diskette, and it is written in the Berkeley SPICE format only. Figures 10-1 through 10-7 show examples of how the test circuits are assembled.

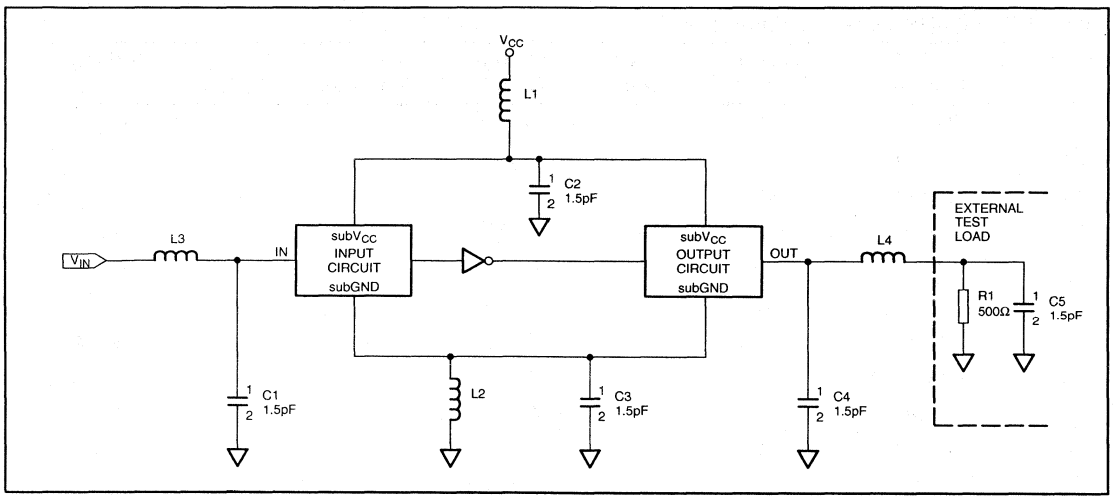


Figure 10-1. Test Circuit for HC(T)00/14/74/123/132/161/163/4538

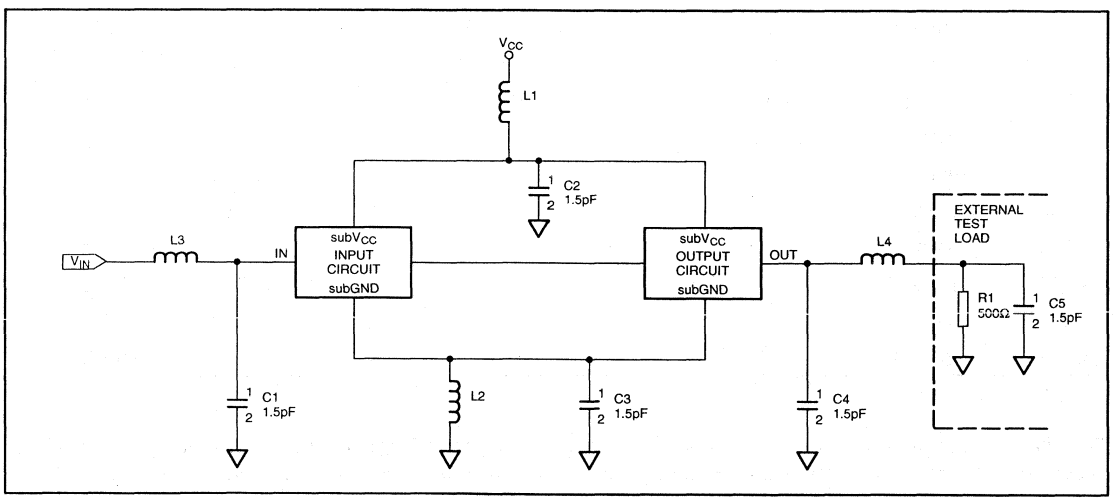


Figure 10-2. Test Circuit for HC(T)04

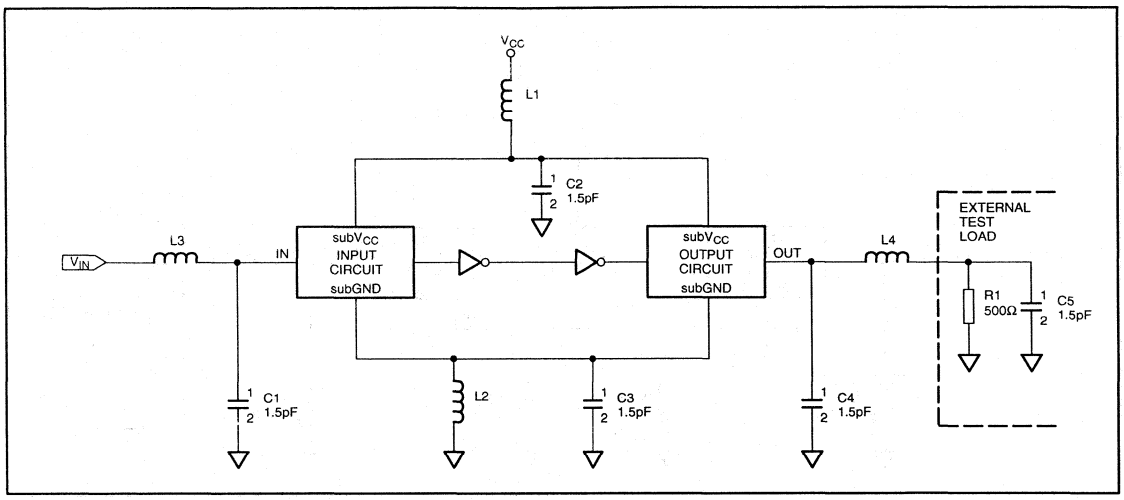


Figure 10-3. Test Circuit for HC(T)32/273/4040

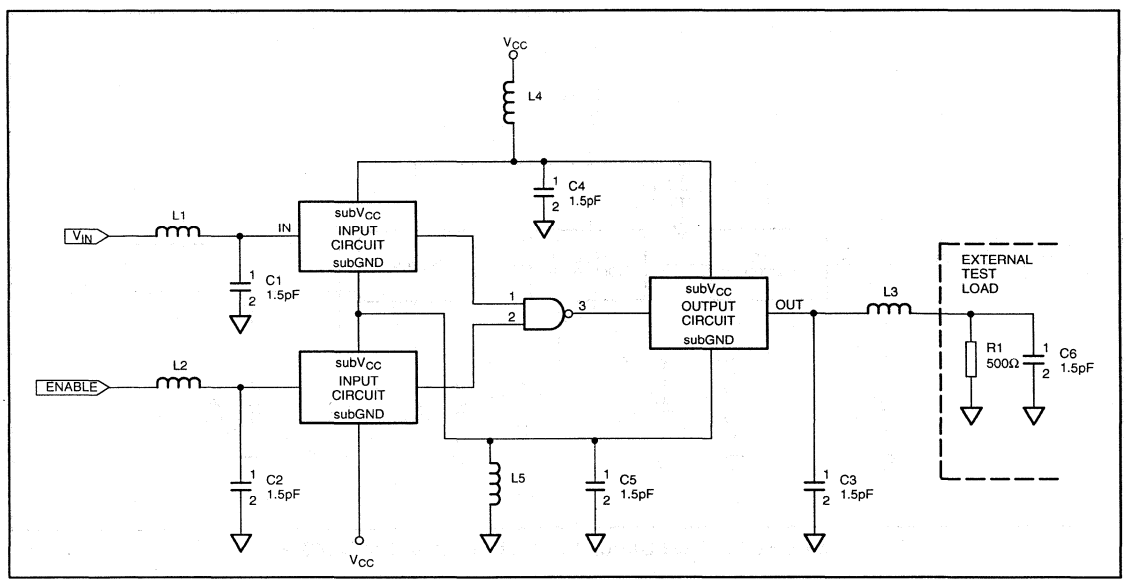


Figure 10-4. Test Circuit for HC(T)138

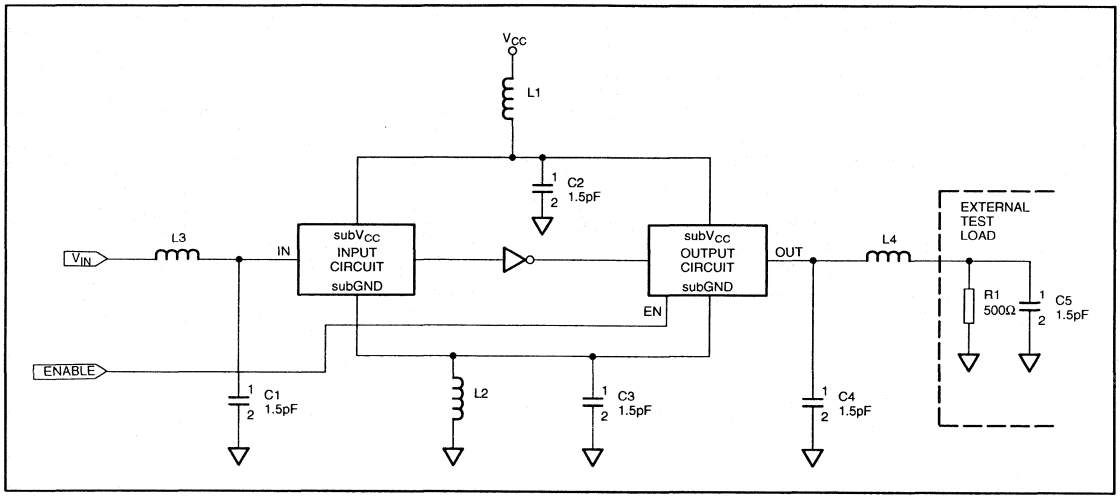


Figure 10-5. Test Circuit for HC(T)244/245/373/374/595

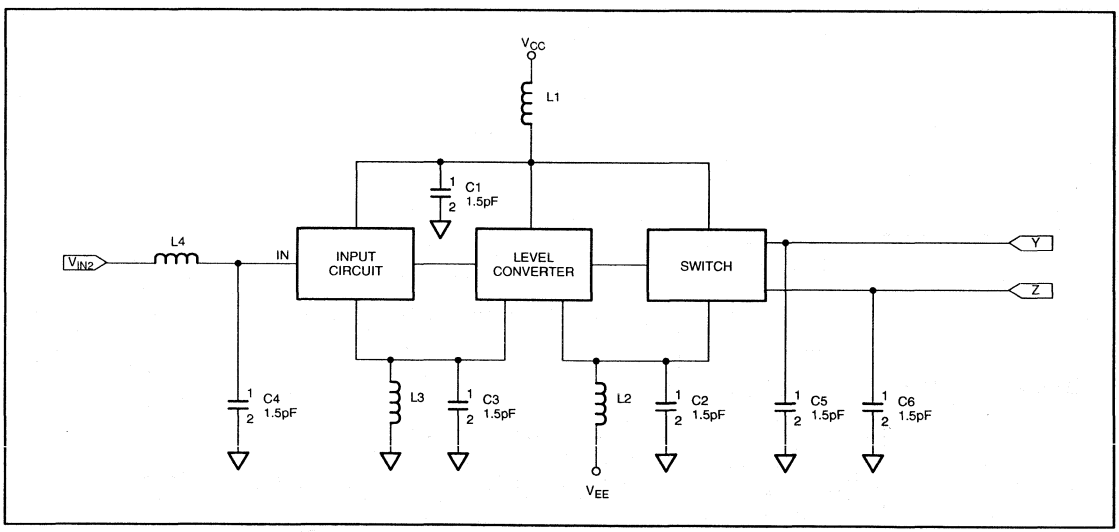


Figure 10-6. Test Circuit for HC(T)4051/4052/4053/4316

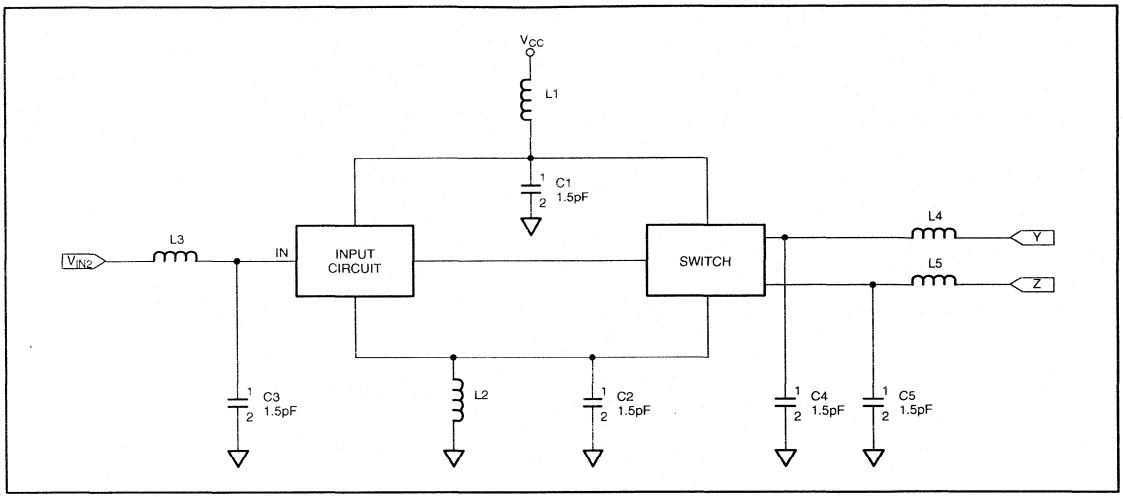


Figure 10-7. Test Circuit for HC(T)4066

Also in the HCMOS Netlists section of the book and in the HCMOS directory of the diskette are files for subcircuits and primitive elements, such as transistors, diodes, and resistors. These files are called HC_TXXXX.CIR, the "XXXX" standing for NOMI, FAST, and SLOW, representing the nominal, fast, and slow process corners. The files contain the subcircuit elements, and they also have package parasitics connected to simulate a device in a package. Package parasitic values can be changed to suit the application. See the Packaging section of the book for values.

For clarification, the following illustration shows how the two programs interact with each other:

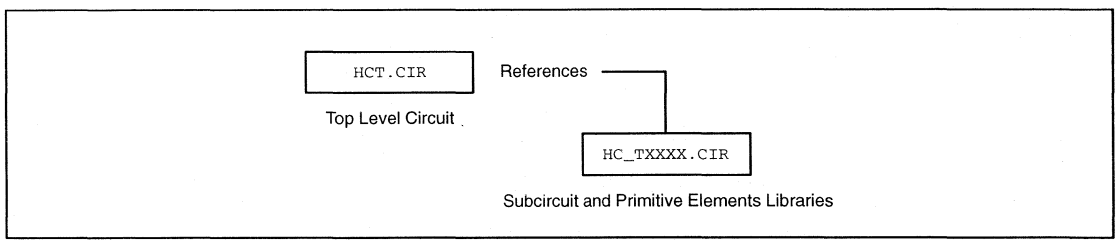


Figure 10-8. HCMOS SPICE Program Hierarchy

The top level program, HCT.CIR, uses an AC test set-up with a 4.5V square wave input, 5ns delay, 6ns rise and fall times, 40ns pulse width, 80ns period, 4.5V V_{CC}, 0V applied to the output enable, and a 1kΩ, 50pF load. These conditions may be modified to suit the application. Pay particular attention to the commented commands in the program when changing simulations from logic devices to the analog switches. Some of the previous commands for the logic devices will have to be commented out. Also, the ".INC" command that specifies the path to reference the other program should be modified to reflect your disk directory structure.

HCMOS Short-form Datasheets

Quad 2-input NAND gate | 74HC/HCT00

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT00 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standdard no. 7A. The 74HC/HCT00 provide the 2-input NAND function.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 6ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	Propagation delay nA, nB to nY	C_L = 15pF; V_{CC} = 5V	7	10	ns
C_I	Input capacitance		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1 and 2	22	22	pF

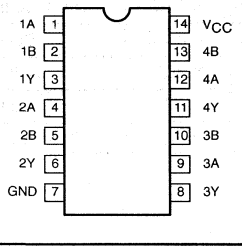
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW): $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; f_o = output frequency in MHz
   C_L = output load capacitance in pF; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5V

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE		DRAWING NUMBER
		HC	HCT	
14-pin plastic DIP	–40 to +125°C	74HC00N	74HCT00N	SOT27-1
14-pin plastic SO	–40 to +125°C	74HC00D	74HCT00D	SOT108-1
14-pin plastic SSOP Type II	–40 to +125°C	74HC00DB	74HCT00DB	SOT337-1
14-pin plastic TSSOP Type III	–40 to +125°C	74HC00PW	74HCT00PW	SOT402-1

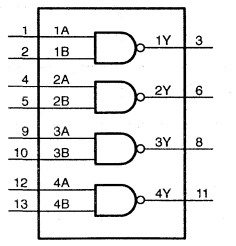
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data inputs
2, 5, 10, 13	1B to 4B	Data inputs
3, 6, 8, 11	1Y to 4Y	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

Hex inverter | 74HC/HCT04

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT04 are high-speed Si-gate CMOS devices and rea pin compatible with low power Schottky TTL (LSTTL). they are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT04 provide six inverting buffers

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 6ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	Propagation delay nA to nY	C_L = 15pF; V_{CC} = 5V	7	8	ns
C_I	Input capacitance		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1 and 2	21	24	pF

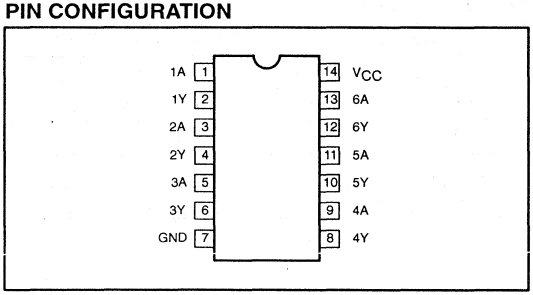
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW): $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; f_o = output frequency in MHz
   C_L = output load capacitance in pF; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5V

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE		DRAWING NUMBER
		HC	HCT	
14-pin plastic DIP	–40 to +125°C	74HC04N	74HCT04N	SOT27-1
14-pin plastic SO	–40 to +125°C	74HC04D	74HCT04D	SOT108-1
14-pin plastic SSOP Type II	–40 to +125°C	74HC04DB	74HCT04DB	SOT337-1
14-pin plastic TSSOP Type III	–40 to +125°C	74HC04PW	74HCT04PW	SOT402-1

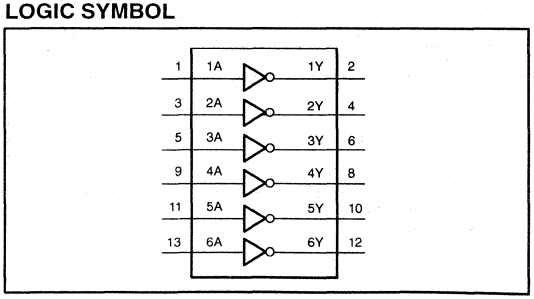
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	Data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUTS	OUTPUTS
nA	nY
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

Hex inverting Schmitt trigger | 74HC/HCT14

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT14 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT14 provide six inverting buffers with Schmitt-trigger action. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 6ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL} / t_{PLH}	Propagation delay nA to nY	C_L = 15pF; V_{CC} = 5V	12	17	ns
C_I	Input capacitance		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per gate	notes 1 and 2	7	8	pF

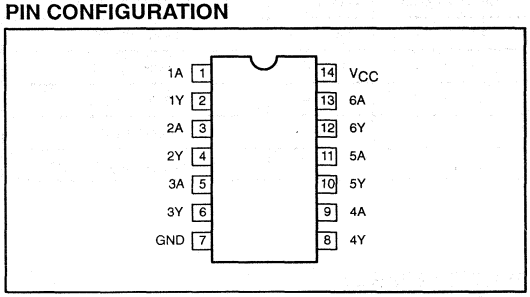
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW): $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; f_o = output frequency in MHz
   C_L = output load capacitance in pF; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5V

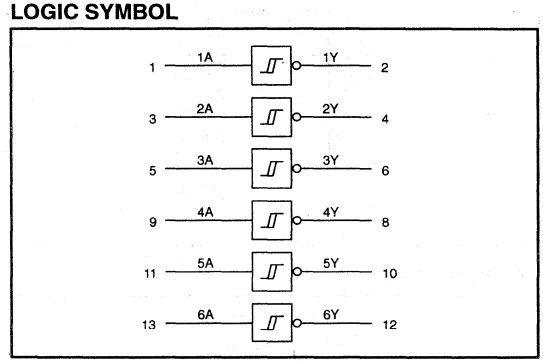
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE		DRAWING NUMBER
		HC	HCT	
14-pin plastic DIP	–40 to +125°C	74HC14N	74HCT14N	SOT27-1
14-pin plastic SO	–40 to +125°C	74HC14D	74HCT14D	SOT108-1
14-pin plastic SSOP Type II	–40 to +125°C	74HC14DB	74HCT14DB	SOT337-1
14-pin plastic TSSOP Type III	–40 to +125°C	74HC14PW	74HCT14PW	SOT402-1

PIN CONFIGURATION



LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	Data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

Quad 2-input OR gate | 74HC/HCT32

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The HC/HCT32 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT32 provide the 2-input OR function.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 6ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL} / t_{PLH}	Propagation delay nA, nB to nY	C_L = 15pF; V_{CC} = 5V	6	9	ns
C_I	Input capacitance		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1 and 2	16	28	pF

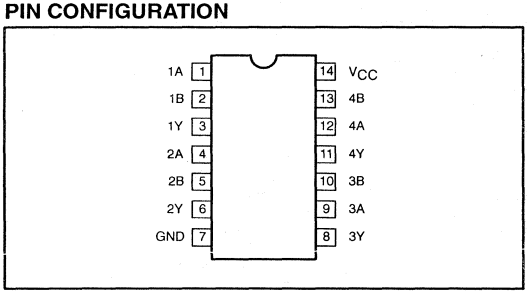
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW): $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; f_o = output frequency in MHz
   C_L = output load capacitance in pF; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5V

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE		DRAWING NUMBER
		HC	HCT	
14-pin plastic DIP	−40 to +125°C	74HC32N	74HCT32N	SOT27-1
14-pin plastic SO	−40 to +125°C	74HC32D	74HCT32D	SOT108-1
14-pin plastic SSOP Type II	−40 to +125°C	74HC32DB	74HCT32DB	SOT337-1
14-pin plastic TSSOP Type III	−40 to +125°C	74HC32PW	74HCT32PW	SOT402-1

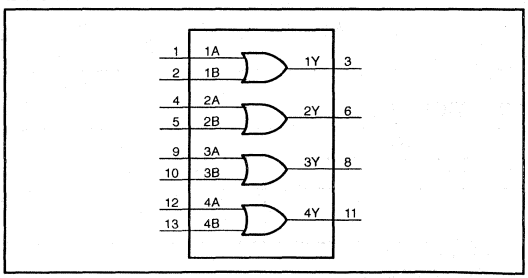
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data inputs
2, 5, 10, 13	1B to 4B	Data inputs
3, 6, 8, 11	1Y to 4Y	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH voltage level
L = LOW voltage level

Dual D-type flip-flop with set and reset; positive-edge trigger

74HC/HCT74

FEATURES

- Output capability: standard
- I_{CC} category: flip-flops

GENERAL DESCRIPTION

The 74HC/HCT74 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT74 are dual positive-edge triggered, D-type flip-flops with individual data (D) inputs, clock (CP) inputs, set ($\overline{S}_D$) and reset ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 6ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL} t_{PLH}	Propagation delay nCP to nQ, n$\overline{Q}$ n$\overline{S}_D$ to nQ, n$\overline{Q}$ n$\overline{R}_D$ to nQ, n$\overline{Q}$	C_L = 15pF; V_{CC} = 5V	 14 15 16	 15 18 18	 ns ns ns
f_{MAX}	Maximum clock frequency		76	59	MHz
C_I	Input capacitance		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per flip-flop	notes 1 and 2	24	29	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW): $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; f_o = output frequency in MHz
   C_L = output load capacitance in pF; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5V

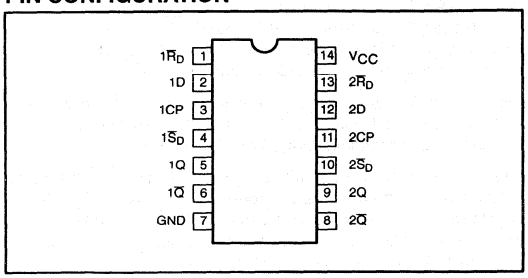
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE		DRAWING NUMBER
		HC	HCT	
14-pin plastic DIP	−40 to +125°C	74HC74N	74HCT74N	SOT27-1
14-pin plastic SO	−40 to +125°C	74HC74D	74HCT74D	SOT108-1
14-pin plastic SSOP Type II	−40 to +125°C	74HC74DB	74HCT74DB	SOT337-1
14-pin plastic TSSOP Type III	−40 to +125°C	74HC74PW	74HCT74PW	SOT402-1

Dual D-type flip-flop with set and reset; positive-edge trigger

74HC/HCT74

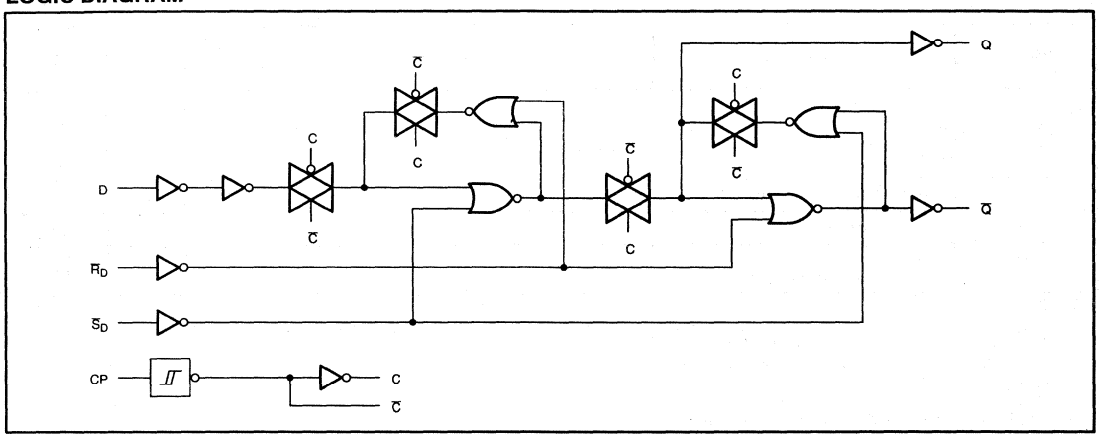
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 13	1$\overline{R}_D$, 2$\overline{R}_D$	Asynchronous reset-direct input (active LOW)
2, 12	1D, 2D	Data inputs
3, 11	1CP, 2CP	Clock input (LOW-to-HIGH, edge-triggered)
4, 10	1$\overline{S}_D$, 2$\overline{S}_D$	Asynchronous set-direct input (active LOW)
5, 9	1Q, 2Q	True flip-flop outputs
6, 8	1$\overline{Q}$, 2$\overline{Q}$	Complement flip-flop outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLES

INPUTS				OUTPUTS	
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

INPUTS				OUTPUTS	
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH CP transition
Q_{n+1} = state after the next LOW-to-HIGH CP transition

Dual retriggerable monostable multivibrator with reset

74HC/HCT123

FEATURES

- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100% duty factor
- Direct reset terminates output pulse
- Schmitt-trigger action on all inputs except for the reset input
- Output capability: standard (except for nR_{EXT}/C_{EXT})
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT123 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT123 are dual retriggerable monostable multivibrators with output pulse width control by three methods. The basic pulse time is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}). The external resistor and capacitor are normally connected as shown in the figure entitled "Timing Component Connections".

Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ($n\overline{A}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period (nQ = HIGH, $n\overline{Q}$ =LOW) can be made as long as desired. Alternatively, an output delay can be terminated at any time by a LOW-going edge on input $n\overline{R}_D$, which also inhibits the triggering.

An internal connection from $n\overline{R}_D$ to the input gates makes it possible to trigger the circuit by a positieve-going signal at input $n\overline{R}_D$ as shown in the Function Table. The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT}. When C_{EXT} > 10,000pF, the typical output pulse width is defined as:

$t_W = 0.45 \times C_{EXT}$ (typ.),

where, t_W = pulse width in ns;
R_{EXT} = external resistor in kΩ;
C_{EXT} = external capacitor in pF.

Schmitt-trigger action in the $n\overline{A}$ and nB inputs, makes the circuit highly tolerant to slower input rise and fall times.

The 74HC/HCT123 is identical the the 74HC/HCT423, but can be triggered via the reset input.

QUICK REFERENCE DATA

GND = 0V; T_{AMB} = 25°C; $t_r = t_f$ = 6ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL} t_{PLH}	Propagation delay $n\overline{A}$, nB to nQ, $n\overline{Q}$ $n\overline{R}_D$ to nQ, $n\overline{Q}$	C_L = 15pF; V_{CC} = 5V R_{EXT} = 5kΩ C_{EXT} = 0pF	26 20	26 23	ns ns
C_I	Input capacitance		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per monostable	Notes 1 and 2	54	56	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) + 0.75 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 16 \times V_{CC}$ where:
   f_i = input frequency in MHz; f_o = output frequency in MHz
   D = duty factor in %; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF; V_{CC} = supply voltage in V
   C_{EXT} = timing capacitance in pF
2. For HC the condition V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5V

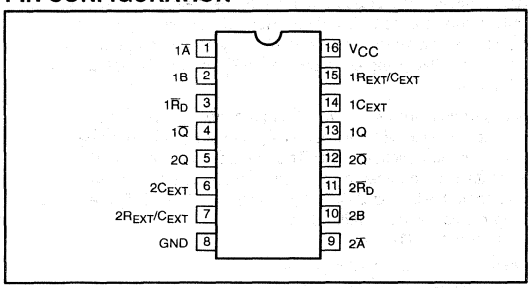
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE		DRAWING NUMBER
		HC	HCT	
16-pin plastic DIP	–40 to +125°C	74HC123N	74HCT123N	SOT38-1
16-pin plastic SO	–40 to +125°C	74HC123D	74HCT123D	SOT109-1
16-pin plastic SSOP Type II	–40 to +125°C	74HC123DB	74HCT123DB	SOT338-1
16-pin plastic TSSOP Type III	–40 to +125°C	74HC123PW	74HCT123PW	SOT403-1

Dual retriggerable monostable multivibrator with reset

74HC/HCT123

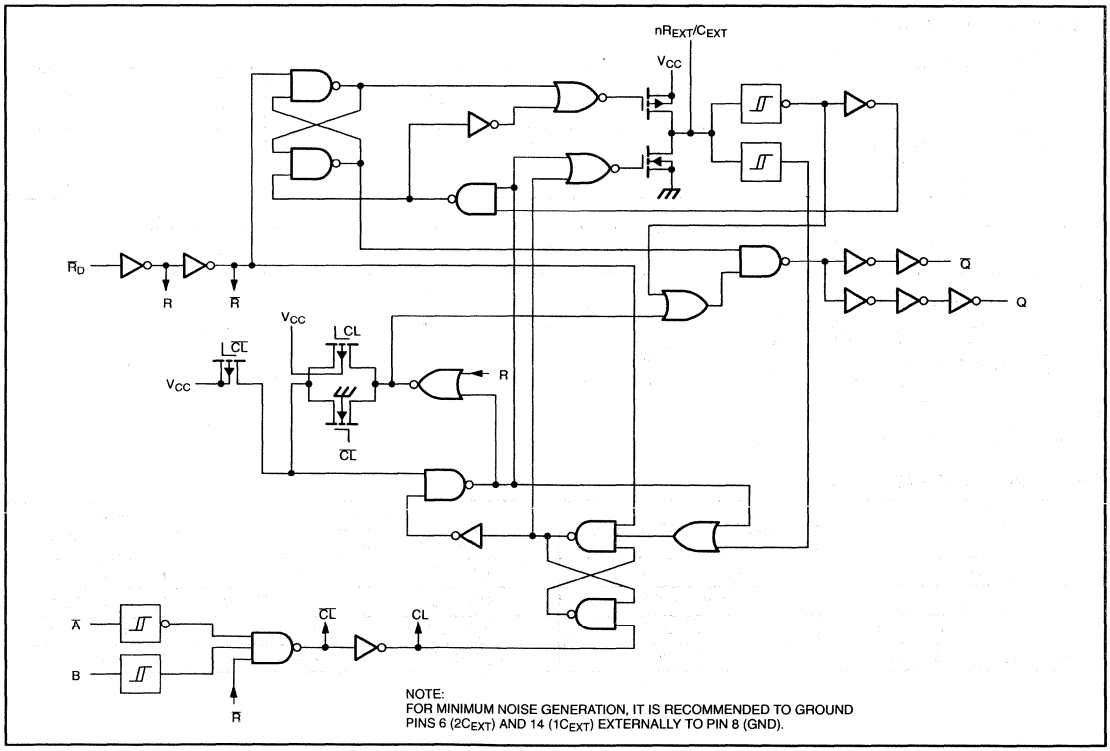
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 9	$1\overline{A}$, $2\overline{A}$	Trigger inputs (negative-edge triggered)
2, 10	1B, 2B	Trigger inputs (positive-edge triggered)
3, 11	$1\overline{R}_D$, $2\overline{R}_D$	Direct reset LOW and trigger action at positive edge
4, 12	$1\overline{Q}$, $2\overline{Q}$	Outputs (active LOW)
7	$2R_{EXT}/C_{EXT}$	External resistor/capacitor connection
8	GND	Ground (0V)
13, 5	1Q, 2Q	Outputs (active HIGH)
14, 6	$1C_{EXT}$, $2C_{EXT}$	External capacitor connection
15	$1R_{EXT}/C_{EXT}$	External resistor/capacitor connection
16	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



NOTE:
FOR MINIMUM NOISE GENERATION, IT IS RECOMMENDED TO GROUND PINS 6 ($2C_{EXT}$) AND 14 ($1C_{EXT}$) EXTERNALLY TO PIN 8 (GND).

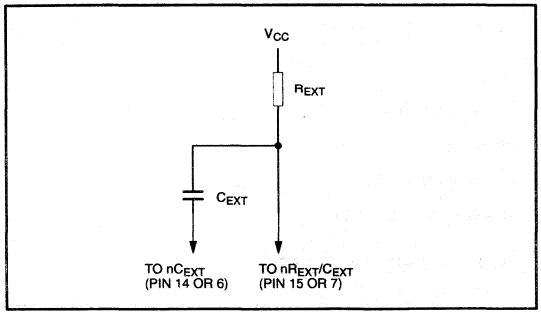
Dual retriggerable monostable multivibrator with reset

FUNCTION TABLE

INPUTS			OUTPUTS	
$n\overline{R}_D$	$n\overline{A}$	nB	nQ	$n\overline{Q}$
L	X	X	L	H
X	H	X	L *	H *
X	X	L	L *	H *
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
⎍ = one HIGH level output pulse
⎍ = one LOW level output pulse

TIMING COMPONENT CONNECTIONS



Quad 2-input NAND Schmitt trigger | 74HC/HCT132

FEATURES

- Output capability: standard
- I_{CC} category: SSI

APPLICATIONS

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators

GENERAL DESCRIPTION

The 74HC/HCT132 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT132 contain four 2-input NAND gates which accept standard input signals. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

The gate switches at different points for positive and negative-going signals. The difference between the positive voltage V_{T+} and the negative voltage V_{T-} is defined as the hysteresis voltage V_H.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 6ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	Propagation delay nA, nB to nY	C_L = 15pF; V_{CC} = 5V	11	17	ns
C_I	Input capacitance		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1 and 2	24	20	pF

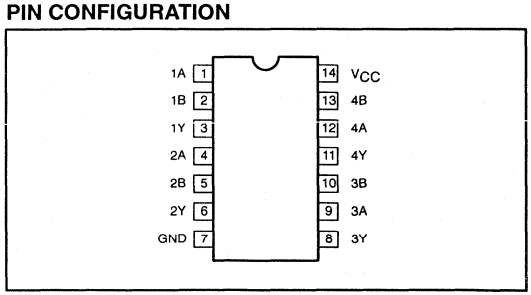
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW): $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; f_o = output frequency in MHz
   C_L = output load capacitance in pF; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs
2. For HC the condition V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5V

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE		DRAWING NUMBER
		HC	HCT	
14-pin plastic DIP	–40 to +125°C	74HC132N	74HCT132N	SOT27-1
14-pin plastic SO	–40 to +125°C	74HC132D	74HCT132D	SOT108-1
14-pin plastic SSOP Type II	–40 to +125°C	74HC132DB	74HCT132DB	SOT337-1
14-pin plastic TSSOP Type III	–40 to +125°C	74HC132PW	74HCT132PW	SOT402-1

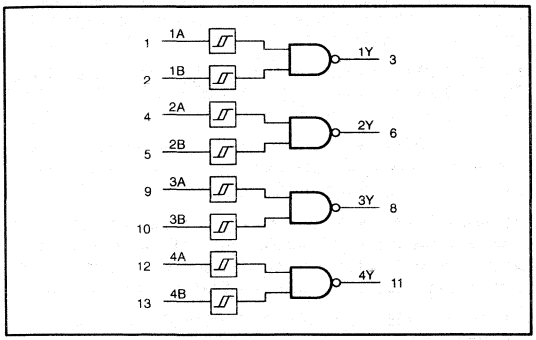
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data inputs
2, 5, 10, 13	1B to 4B	Data inputs
3, 6, 8, 11	1Y to 4Y	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

3-to-8 line decoder/multiplexer; inverting 74HC/HCT138

FEATURES

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT138 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT138 decoders accept three binary weighted address inputs (A0, A1, A2) and when enabled, provide 8 mutually exclusive active LOW outputs ($\overline{Y}0$ to $\overline{Y}7$).

The 74HC/HCT138 features three enable inputs: two active LOW ($\overline{E}1$ and $\overline{E}2$) and one active HIGH (E3). Every output will be HIGH unless $\overline{E}1$ and $\overline{E}2$ are LOW and E3 is HIGH.

This multiple enable function allows easy parallel expansion of the 74HC/HCT138 to a 1-of-32 (5 lines to 32 lines) decoder with just four 74HC/HCT138 ICs and one inverter.

The 74HC/HCT138 can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

The 74HC/HCT138 is identical to the 74HC/HCT238, but has inverting outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 6ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	Propagation delay An to $\overline{Y}n$	C_L = 15pF; V_{CC} = 5V	12	17	ns
	Propagation delay E3 to $\overline{Y}n$ $\overline{E}n$ to $\overline{Y}n$		14	19	ns
C_I	Input capacitance		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per package	Notes 1 and 2	67	67	pF

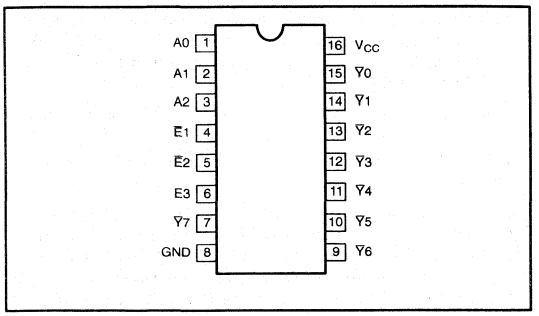
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW): $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; f_o = output frequency in MHz
   C_L = output load capacitance in pF; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs
2. For HC the condition V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5V

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE		DRAWING NUMBER
		HC	HCT	
16-pin plastic DIP	−40 to +125°C	74HC138N	74HCT138N	SOT38-1
16-pin plastic SO	−40 to +125°C	74HC138D	74HCT138D	SOT109-1
16-pin plastic SSOP Type II	−40 to +125°C	74HC138DB	74HCT138DB	SOT338-1
16-pin plastic TSSOP Type III	−40 to +125°C	74HC138PW	74HCT138PW	SOT403-1

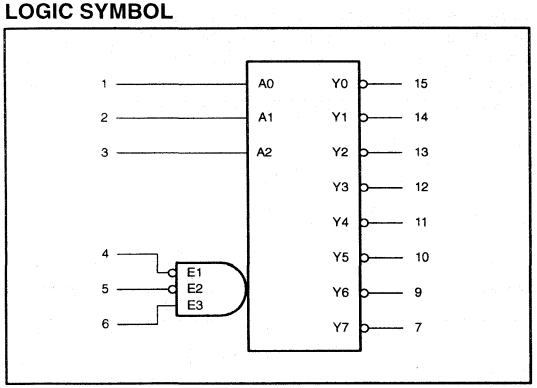
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 3	A0 – A2	Address inputs
4, 5	$\overline{E1}$ – $\overline{E2}$	Enable inputs (active LOW)
6	E3	Enable input (active HIGH)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y0}$ – $\overline{Y7}$	Outputs (active LOW)
8	GND	Ground (0V)
16	V_{CC}	Positive power supply

LOGIC SYMBOL



FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E1}$	$\overline{E2}$	E3	A0	A1	A2	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	Y6	$\overline{Y7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

Presettable synchronous 4-bit binary counter; asynchronous reset

74HC/HCT161

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Asynchronous reset
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT161 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT161 are synchronous presettable binary counters which feature an internal look-ahead carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).

The outputs (Q0 to Q3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D0 to D3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold timer requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

A LOW level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q0 to Q3) to LOW level regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q0. This pulse can be used to enable the next cascaded stage.

The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{MAX} = \frac{1}{t_{P(MAX)}\ (\text{CP to TC}) + t_{SU}\ (\text{CEP to CP})}$$

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 6ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	Propagation delay CP to Qn CP to TC $\overline{MR}$ to Qn $\overline{MR}$ to TC CET to TC	C_L = 15pF; V_{CC} = 5V	 19 21 20 20 10	 20 24 25 26 14	 ns ns ns ns ns
f_{MAX}	Maximum clock frequency		44	45	MHz
C_I	Input capacitance		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per package	Notes 1 and 2	33	35	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\ (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; f_o = output frequency in MHz
   C_L = output load capacitance in pF; V_{CC} = supply voltage in V
   $\Sigma\ (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs
2. For HC the condition V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5V

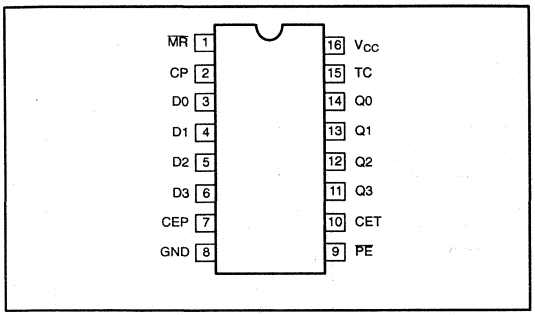
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE		DRAWING NUMBER
		HC	HCT	
16-pin plastic DIP	−40 to +125°C	74HC161N	74HCT161N	SOT38-1
16-pin plastic SO	−40 to +125°C	74HC161D	74HCT161D	SOT109-1
16-pin plastic SSOP Type II	−40 to +125°C	74HC161DB	74HCT161DB	SOT338-1
16-pin plastic TSSOP Type III	−40 to +125°C	74HC161PW	74HCT161PW	SOT403-1

Presettable synchronous 4-bit binary counter; asynchronous reset

74HC/HCT161

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	Asynchronous master reset (active LOW)
2	CP	Clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	D0 to D3	Data inputs
7	CEP	Count enable input
8	GND	Ground (0V)
9	$\overline{PE}$	Parallel enable input (active LOW)
10	CET	Count enable carry input
14, 13, 12, 11	Q0 to Q3	Flip-flop outputs
15	TC	Terminal count output
16	V_{CC}	Positive supply voltage

FUNCTION TABLE

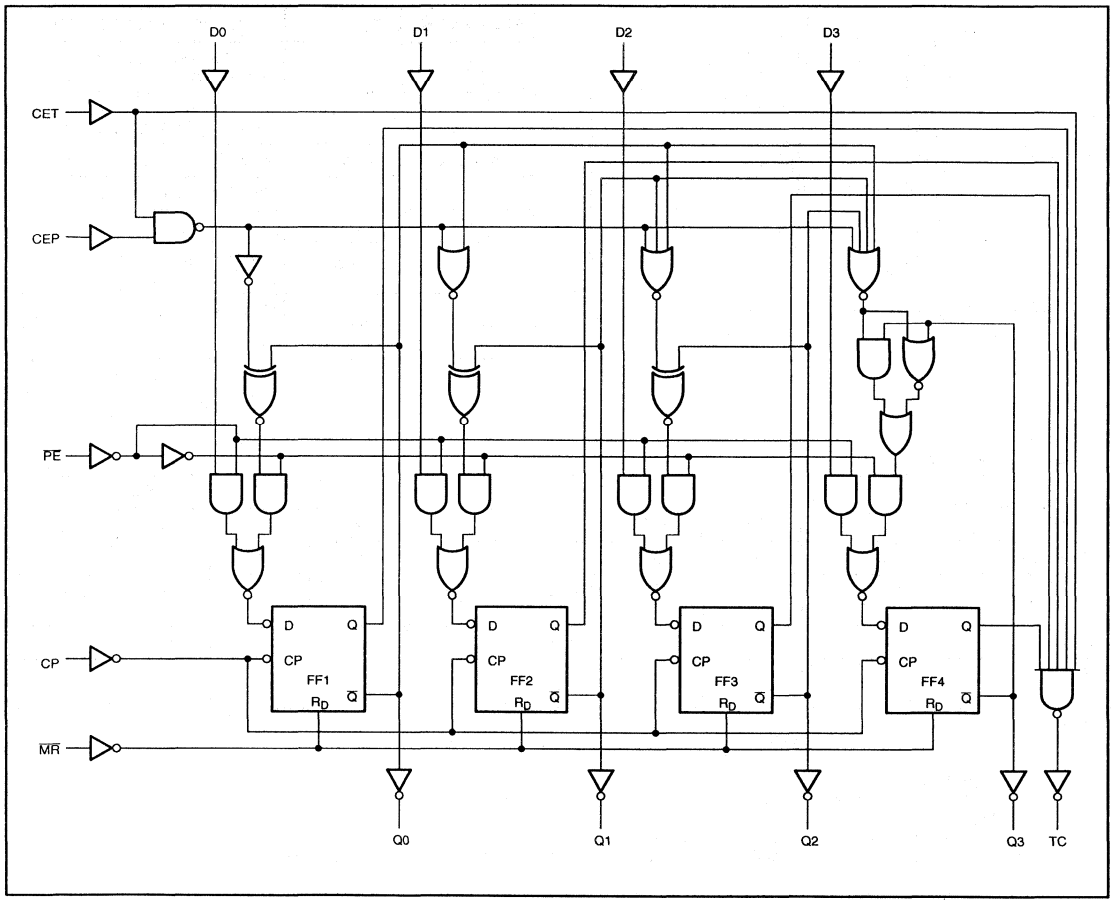
OPERATIONG MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	Dn	Qn	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H H	↑ ↑	X X	X X	l l	l h	L H	L *
Count	H	↑	h	h	h	X	count	*
Hold (do nothing)	H H	X X	l X	X l	h h	X X	qn qn	* L

NOTE:

* The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH).

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = Lower case letters indicate the state of the reference output one set-up time prior to the LOW-to-HIGH CP transition
X = Don't care
↑ = LOW-to-HIGH CP transition

LOGIC DIAGRAM



Presettable synchronous 4-bit binary counter; synchronous reset

74HC/HCT163

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Synchronous reset
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT163 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT163 are synchronous presettable binary counters which feature an internal look-ahead carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).

The outputs (Q0 to Q3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D0 to D3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

For the 74HC/HCT163, the clear function is synchronous.

A LOW level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q0 to Q3) to LOW level after the next positive-going transition on the clock (CP) input (provided that the set-up and hold time requirements for $\overline{MR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET and CEP inputs.

This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q0. This pulse can be used to enable the next cascaded stage.

The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{MAX} = \frac{1}{t_{P(MAX)}\ (\text{CP to TC}) + t_{SU}\ (\text{CEP to CP})}$$

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 6ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	Propagation delay CP to Qn CP to TC CET to TC	C_L = 15pF; V_{CC} = 5V	 17 21 11	 20 25 14	 ns ns ns
f_{MAX}	Maximum clock frequency		51	50	MHz
C_I	Input capacitance		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per package	Notes 1 and 2	33	35	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\ (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; f_o = output frequency in MHz
   C_L = output load capacitance in pF; V_{CC} = supply voltage in V
   $\Sigma\ (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs
2. For HC the condition V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5V

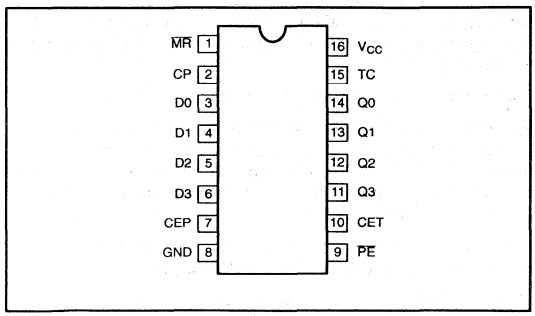
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE		DRAWING NUMBER
		HC	HCT	
16-pin plastic DIP	–40 to +125°C	74HC163N	74HCT163N	SOT38-1
16-pin plastic SO	–40 to +125°C	74HC163D	74HCT163D	SOT109-1
16-pin plastic SSOP Type II	–40 to +125°C	74HC163DB	74HCT163DB	SOT338-1
16-pin plastic TSSOP Type III	–40 to +125°C	74HC163PW	74HCT163PW	SOT403-1

Presettable synchronous 4-bit binary counter; synchronous reset

74HC/HCT163

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	Synchronous master reset (active LOW)
2	CP	Clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	D0 to D3	Data inputs
7	CEP	Count enable input
8	GND	Ground (0V)
9	$\overline{PE}$	Parallel enable input (active LOW)
10	CET	Count enable carry input
14, 13, 12, 11	Q0 to Q3	Flip-flop outputs
15	TC	Terminal count output
16	V_{CC}	Positive supply voltage

FUNCTION TABLE

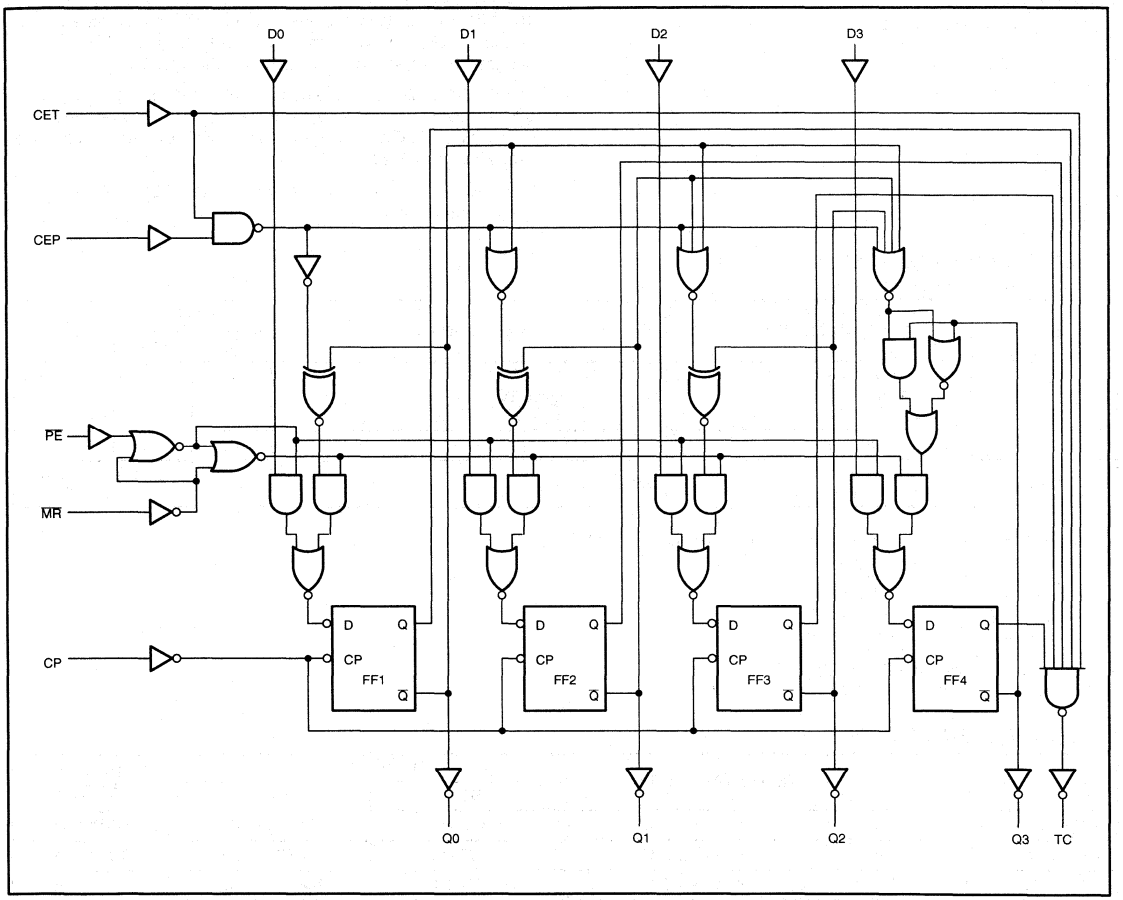
OPERATIONG MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	Dn	Qn	TC
Reset (clear)	l	↑	X	X	X	X	L	L
Parallel load	h h	↑ ↑	X X	X X	l l	l h	L H	L *
Count	h	↑	h	h	h	X	count	*
Hold (do nothing)	h h	X X	l X	X l	h h	X X	qn qn	* L

NOTE:

* The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH).

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = Lower case letters indicate the state of the reference output one set-up time prior to the LOW-to-HIGH CP transition
X = Don't care
↑ = LOW-to-HIGH CP transition

LOGIC DIAGRAM



Octal buffer/line driver (3-State) 74HC/HCT244

FEATURES

- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT244 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT244 are octal non-inverting buffer/line drivers with 3-State outputs. The 3-State outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.

The 74HC/HCT244 is identical to the 74HC/HCT240 but has non-inverting outputs.

QUICK REFERENCE DATA

GND = 0V; T_{AMB} = 25°C; $t_r = t_f$ = 6ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL} t_{PLH}	Propagation delay 1An to 1Yn; 2An to 2Yn	C_L = 15pF; V_{CC} = 5V	9	11	ns
C_I	Input capacitance		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1 and 2	35	35	pF

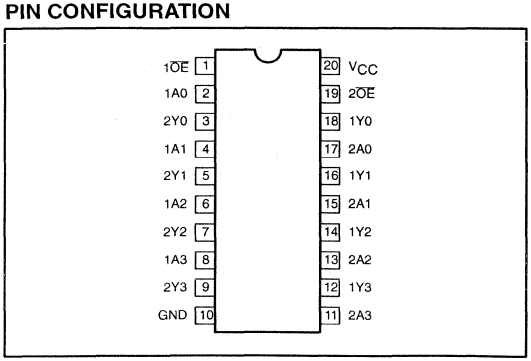
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5V

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE		DRAWING NUMBER
		HC	HCT	
20-pin plastic DIP	–40 to +125°C	74HC244N	74HCT244N	SOT146-1
20-pin plastic SO	–40 to +125°C	74HC244D	74HCT244D	SOT163-1
20-pin plastic SSOP Type II	–40 to +125°C	74HC244DB	74HCT244DB	SOT339-1
20-pin plastic TSSOP Type III	–40 to +125°C	74HC244PW	74HCT244PW	SOT360-1

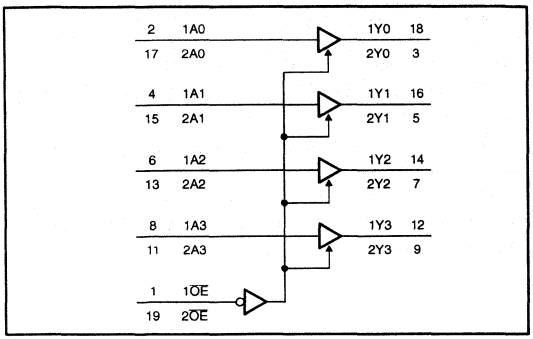
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 4, 6, 8	1A0 to 1A3	Data inputs
3, 5, 7, 9	2Y0 to 2Y3	Bus outputs
10	GND	Ground (0V)
17, 15, 13, 11	2A0 to 2A3	Data inputs
18, 16, 14, 12	1Y0 to 1Y3	Bus outputs
19	$2\overline{OE}$	Output enable input (active LOW)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nAn	nYn
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF-state

Octal bus transceiver (3-State) 74HC/HCT245

FEATURES

- Octal bidirectional bus interface
- Non-inverting 3-State outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT245 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT are octal tranceivers featuring non-inverting 3-State bus compatible outputs in both send and receive directions.

The 74HC/HCT245 features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.

The 74HC/HCT245 is similar to the 74HC/HCT640 but has true (non-inverting) outputs.

QUICK REFERENCE DATA

GND = 0V; T_{AMB} = 25°C; $t_r = t_f$ = 6ns

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL		UNIT
			HC	HCT	
t_{PHL} t_{PLH}	Propagation delay An to Bn; Bn to An	C_L = 15pF; V_{CC} = 5V	7	10	ns
C_I	Input capacitance		3.5	3.5	pF
$C_{I/O}$	Input/output capacitance		10	10	pF
C_{PD}	Power dissipation capacitance per transceiver	notes 1 and 2	30	30	pF

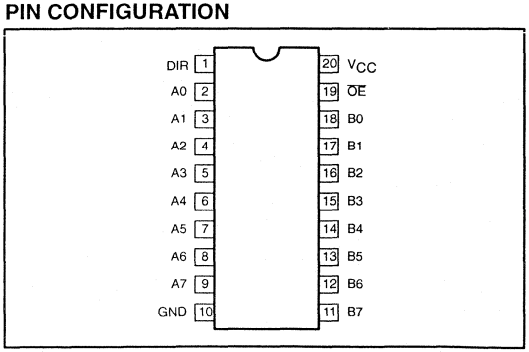
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; f_o = output frequency in MHz
   C_L = output load capacitance in pF; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs
2. For HC the condition V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5V

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE		DRAWING NUMBER
		HC	HCT	
20-pin plastic DIP	−40 to +125°C	74HC245N	74HCT245N	SOT146-1
20-pin plastic SO	−40 to +125°C	74HC245D	74HCT245D	SOT163-1
20-pin plastic SSOP Type II	−40 to +125°C	74HC245DB	74HCT245DB	SOT339-1
20-pin plastic TSSOP Type III	−40 to +125°C	74HC245PW	74HCT245PW	SOT360-1

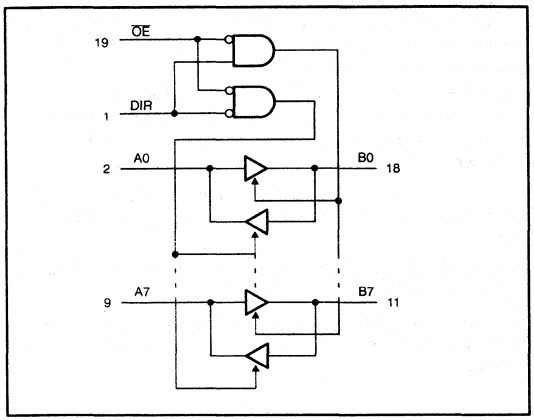
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	DIR	Direction control
2, 3, 4, 5, 6, 7, 8, 9	A0 to A7	Data inputs/outputs
10	GND	Ground (0V)
18, 17, 16, 15 14, 13, 12, 11	B0 to B7	Data inputs/outputs
19	$\overline{OE}$	Output enable input (active LOW)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	An	Bn
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF-state

Octal D-type flip-flop with reset; positive-edge trigger

74HC/HCT273

FEATURES

- Ideal buffer for MOS microprocessor or memory
- Common clock and master reset
- Eight positive edge-triggered D-type flip-flops
- See 74HC/HCT377 for clock enable version
- See 74HC/HCT373 for transparent latch version
- See 74HC/HCT374 for 3-State version
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT273 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT273 have eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Qn) of the flip-flop.

All outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the $\overline{MR}$ input.

The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.

QUICK REFERENCE DATA

GND = 0V; T_{AMB} = 25°C; $t_r = t_f$ = 6ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL} t_{PLH}	Propagation delay CP to Qn $\overline{MR}$ to Qn	C_L = 15pF; V_{CC} = 5V	15 15	15 20	ns ns
f_{MAX}	Maximum clock frequency		66	36	MHz
C_I	Input capacitance		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per flip-flop	notes 1 and 2	20	23	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; f_o = output frequency in MHz
   C_L = output load capacitance in pF; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs
2. For HC the condition V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5V

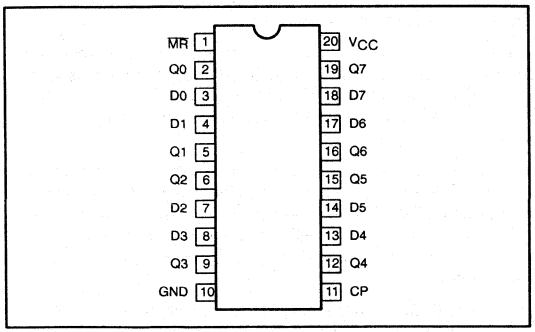
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE		DRAWING NUMBER
		HC	HCT	
20-pin plastic DIP	−40 to +125°C	74HC273N	74HCT273N	SOT146-1
20-pin plastic SO	−40 to +125°C	74HC273D	74HCT273D	SOT163-1
20-pin plastic SSOP Type II	−40 to +125°C	74HC273DB	74HCT273DB	SOT339-1
20-pin plastic TSSOP Type III	−40 to +125°C	74HC273PW	74HCT273PW	SOT360-1

Octal D-type flip-flop with reset; positive-edge trigger

74HC/HCT273

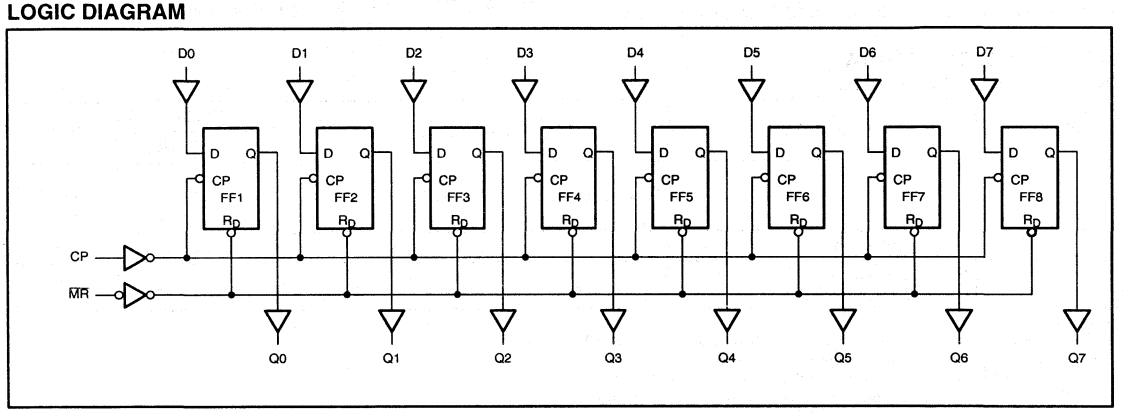
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	Master reset input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 to Q7	Flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data inputs
10	GND	Ground (0V)
11	CP	Clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUT	OPERATING MODES
$\overline{MR}$	CP	Dn	Qn	
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
↑ = LOW-to-HIGH clock transition
X = Don't care

Octal D-type transparent latch (3-State) 74HC/HCT373

FEATURES

- 3-State non-inverting outputs for bus oriented applications
- Common 3-State output enable input
- Functionally identical to the 74HC/HCT563, 74HC/HCT573 and 74HC/HCT533
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT373 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT373 are octal D-type transparent latches featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all latches.

The 74HC/HCT373 consists of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the Dn inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the 8 latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The 74HC/HCT373 is functionally identical to the 74HC/HCT533, 74HC/HCT563 and 74HC/HCT573, but the 74HC/HCT563 and 74HC/HCT533 have inverted outputs, and the 74HC/HCT563 and 74HC/HCT573 have a different pin arrangement.

QUICK REFERENCE DATA

GND = 0V; T_{AMB} = 25°C; $t_r = t_f$ = 6ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL} t_{PLH}	Propagation delay Dn to Qn LE to Qn	C_L = 15pF; V_{CC} = 5V	 12 15	 14 13	 ns ns
C_I	Input capacitance		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1 and 2	45	41	pF

NOTES:

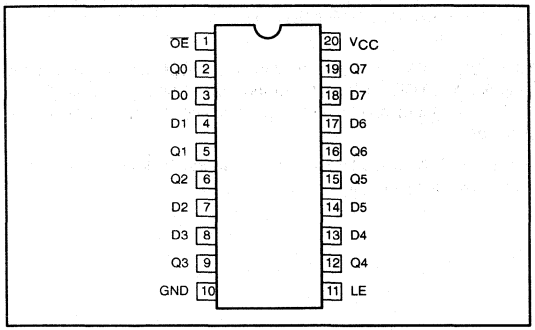
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; f_o = output frequency in MHz
   C_L = output load capacitance in pF; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs
2. For HC the condition V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5V

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE		DRAWING NUMBER
		HC	HCT	
20-pin plastic DIP	–40 to +125°C	74HC373N	74HCT373N	SOT146-1
20-pin plastic SO	–40 to +125°C	74HC373D	74HCT373D	SOT163-1
20-pin plastic SSOP Type II	–40 to +125°C	74HC373DB	74HCT373DB	SOT339-1
20-pin plastic TSSOP Type III	–40 to +125°C	74HC373PW	74HCT373PW	SOT360-1

Octal D-type transparent latch (3-State) 74HC/HCT373

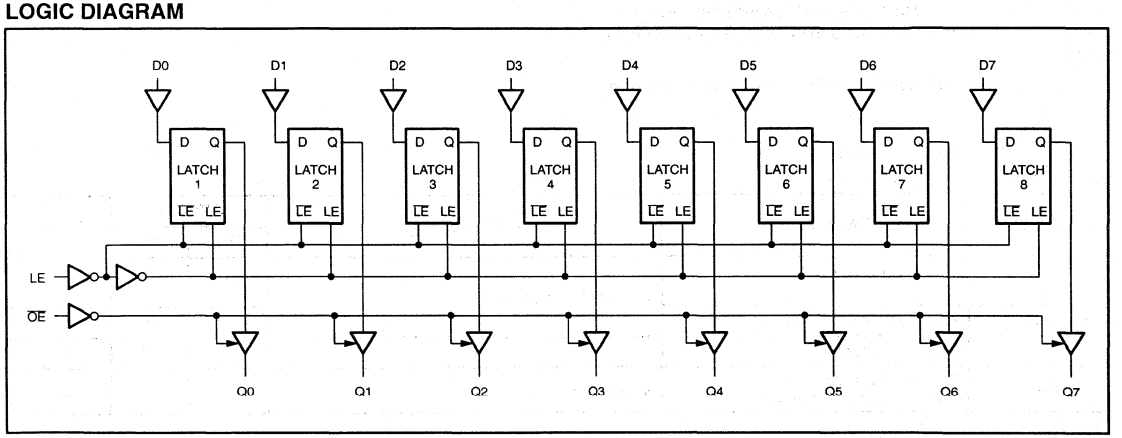
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-State output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 to Q7	3-State latch outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data inputs
10	GND	Ground (0V)
11	LE	Latch enable input (active HIGH)
20	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	Dn		Q0 to Q7
Enable and read register (transparent mode)	L L	H H	L H	L H	L H
Latch and read register	L L	L L	l h	L H	L H
Latch register and disable outputs	H H	X X	X X	X X	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = Don't care
Z = High impedance OFF-state

Octal D-type flip-flop; positive edge-trigger (3-State)

74HC/HCT374

FEATURES

- 3-State non-inverting outputs for bus oriented applications
- 8-bit positive, edge-triggered register
- Common 3-State output enable input
- Independent register and 3-State buffer operation
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT374 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT374 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-State outputs for bus oriented applications.

A clock (CP) and and output enable ($\overline{OE}$) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the 8 flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

the HC/HCT374 is functionally identical to the 74HC/HCT534, but has non-inverting outputs.

QUICK REFERENCE DATA

GND = 0V; T_{AMB} = 25°C; $t_r = t_f$ = 6ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	Propagation delay CP to Qn	C_L = 15pF; V_{CC} = 5V	15	13	ns
f_{MAX}	Maximum clock frequency		77	48	MHz
C_I	Input capacitance		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1 and 2	17	17	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; f_o = output frequency in MHz
   C_L = output load capacitance in pF; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs
2. For HC the condition V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5V

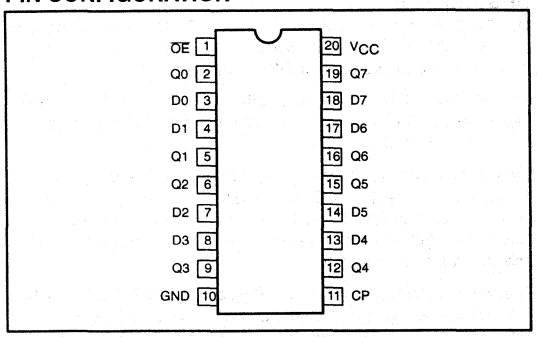
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE		DRAWING NUMBER
		HC	HCT	
20-pin plastic DIP	–40 to +125°C	74HC374N	74HCT374N	SOT146-1
20-pin plastic SO	–40 to +125°C	74HC374D	74HCT374D	SOT163-1
20-pin plastic SSOP Type II	–40 to +125°C	74HC374DB	74HCT374DB	SOT339-1
20-pin plastic TSSOP Type III	–40 to +125°C	74HC374PW	74HCT374PW	SOT360-1

Octal D-type flip-flop; positive edge-trigger (3-State)

74HC/HCT374

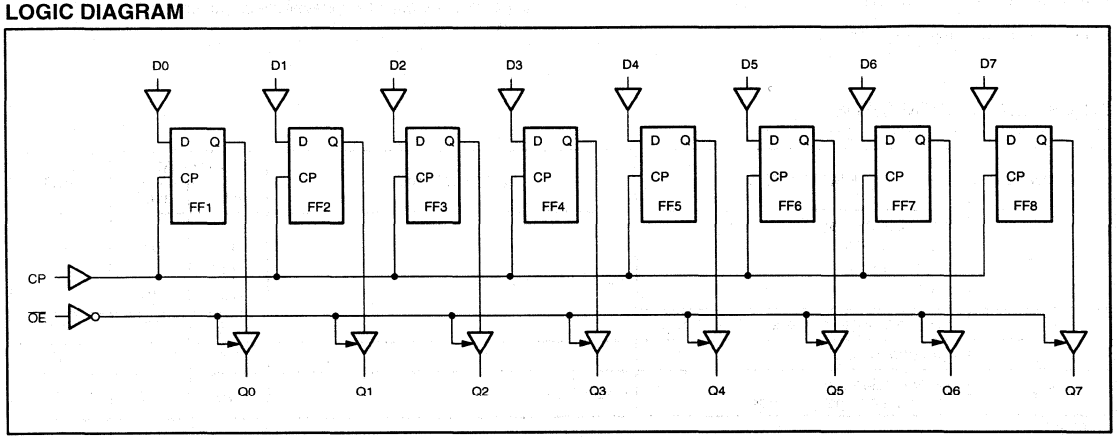
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-State output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 to Q7	3-State flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data inputs
10	GND	Ground (0V)
11	CP	Clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	Dn		Q0 TO Q7
Load and read register	L L	↑ ↑	l h	L H	L H
Load register and disable outputs	H H	↑ ↑	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
↑ = LOW-to-HIGH clock transition
X = Don't care

8-bit serial-in/serial or parallel-out shift register with output latches (3-State)

74HC/HCT595

FEATURES

- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-State outputs
- Shift register with direct clear
- 100MHz (typ.) shift out frequency
- Output capability:
  - Parallel outputs; bus driver
  - Serial output; standard
- I_{CC} category: MSI

APPLICATIONS

- Serial-to-parallel data conversion
- Remote control holding register

DESCRIPTION

The 74HC/HCT595 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT595 is an 8-stage serial shift register with a storage register and 3-State outputs. The shift register and storage register have separate clocks.

Data is shifted on the positive-going transitions of the SH_{CP} input. The data in each register is transferred to the storage register on a positive-going transition of the ST_{CP} input. If both clocks are connected together the shift register will always be one clock pulse ahead of the storage register.

The shift register has a serial input (D_S) and a serial standard output (Q7') for cascading. It is also provided with asynchronous reset (active LOW) for all 8 shift register stages. The storage register has 8 parallel 3-State bus driver outputs. Data in the storage register appears at the output whenever the output enable input (OE) is LOW.

QUICK REFERENCE DATA

GND = 0V; T_{AMB} = 25°C; $t_r = t_f$ = 6ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	Propagation delay SH_{CP} to Q7' ST_{CP} to Qn $\overline{MR}$ to Q7'	C_L = 15pF; V_{CC} = 5V	 16 17 14	 21 20 19	 ns ns ns
f_{MAX}	Maximum clock frequency SH_{CP}, ST_{CP}		100	57	MHz
C_I	Input capacitance		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per package	Notes 1 and 2	115	130	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; f_o = output frequency in MHz
   C_L = output load capacitance in pF; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs
2. For HC the condition V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5V

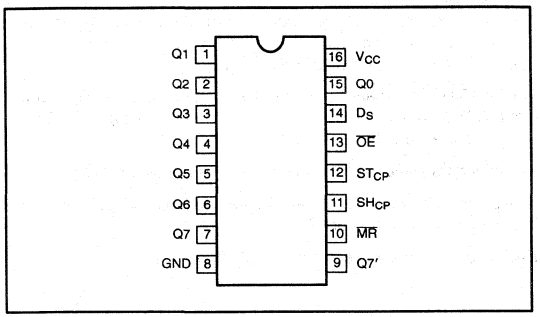
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE		DRAWING NUMBER
		HC	HCT	
16-pin plastic DIP	–40 to +125°C	74HC595N	74HCT595N	SOT38-1
16-pin plastic SO	–40 to +125°C	74HC595D	74HCT595D	SOT109-1
16-pin plastic SSOP Type II	–40 to +125°C	74HC595DB	74HCT595DB	SOT338-1
16-pin plastic TSSOP Type III	–40 to +125°C	74HC595PW	74HCT595PW	SOT403-1

8-bit serial-in/serial or parallel-out shift register with output latches (3-State)

74HC/HCT595

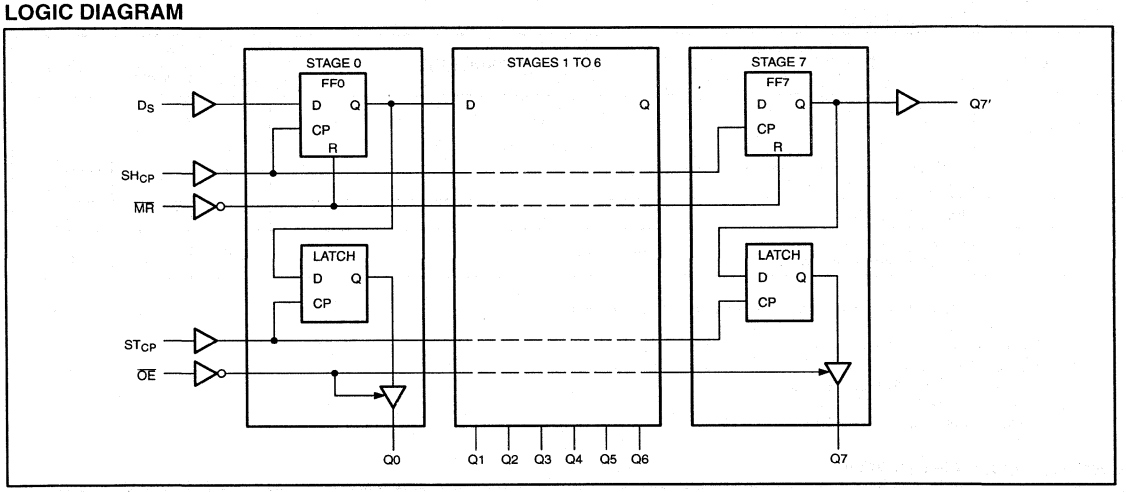
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 15	Q0 – Q7	Parallel data output
8	GND	Ground (0V)
9	Q7′	Serial data output
10	$\overline{MR}$	Master reset (active LOW)
11	SH_{CP}	Shift register clock input
12	ST_{CP}	Storage register clock input
13	$\overline{OE}$	Output enable (active LOW)
14	D_S	Serial data input
16	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS		FUNCTION
SH_{CP}	ST_{CP}	$\overline{OE}$	$\overline{MR}$	D_S	Q7′	Qn	
X	X	L	↓	X	L	NC	A LOW level on $\overline{MR}$ only affects the shift registers.
X	↑	L	L	X	L	L	Empty shift register loaded into storage register.
X	X	H	L	X	L	Z	Shift register clear. Parallel outputs in high-impedance OFF-state.
↑	X	L	H	H	Q6′	NC	Logic HIGH level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g., previous state of stage 6 (internal Q6′) appears on the serial output (Q7′).
X	↑	L	H	X	NC	Qn′	Contents of shift register stages (internal Qn′) are transferred to the storage register and parallel output stages.
↑	↑	L	H	X	Q6′	Qn′	Contents of shift register shifted through. Previous contents of the shift register is transferred to the storage rregister and the parallel output stages.

H = HIGH voltage level
L = LOW voltage level
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
Z = High impedance OFF-state
NC= No change
X = Don't care

12-stage binary ripple counter | 74HC/HCT4040

FEATURES

- Output capability: standard
- I_{CC} category: MSI

APPLICATIONS

- Frequency dividing circuits
- Time delay circuits
- Control counters

GENERAL DESCRIPTION

The 74HC/HCT4040 are high-speed Si-gate CMOS devices and are pin compatible with the "4040" of the "4000B" series. They are specified n compliance with JEDEC standard no. 7A.

The 74HC/HCT4040 are 12-stage binary ripple counters with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve parallel outputs (Q0 to Q11).

The counter advances on the HIGH-to-LOW transition of $\overline{CP}$.

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$.

Each counter stage is a static toggle flip-flop.

QUICK REFERENCE DATA

GND = 0V; T_{AMB} = 25°C; $t_r = t_f$ = 6ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	Propagation delay $\overline{CP}$ to Q0 Qn to Qn+1	C_L = 15pF; V_{CC} = 5V	 14 8	 16 8	 ns ns
f_{MAX}	Maximum clock frequency		90	79	MHz
C_I	Input capacitance		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per package	Notes 1 and 2	20	20	pF

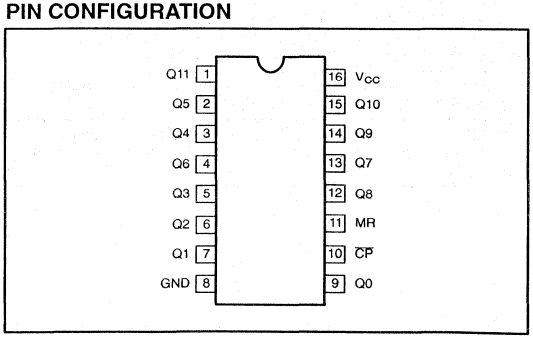
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; f_o = output frequency in MHz
   C_L = output load capacitance in pF; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs
2. For HC the condition V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5V

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE		DRAWING NUMBER
		HC	HCT	
16-pin plastic DIP	–40 to +125°C	74HC4040N	74HCT4040N	SOT38-1
16-pin plastic SO	–40 to +125°C	74HC4040D	74HCT4040D	SOT109-1
16-pin plastic SSOP Type II	–40 to +125°C	74HC4040DB	74HCT4040DB	SOT338-1
16-pin plastic TSSOP Type III	–40 to +125°C	74HC4040PW	74HCT4040PW	SOT403-1

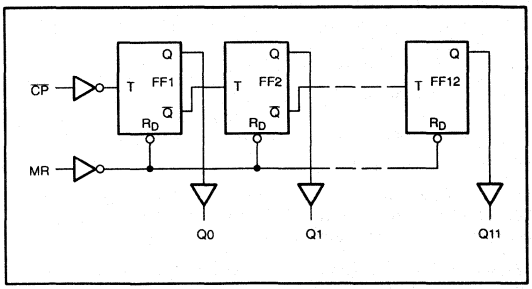
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
8	GND	Ground (0V)
9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1	Q0 – Q11	Parallel outputs
10	$\overline{CP}$	Clock input (HIGH-to-LOW, edge-triggered)
11	MR	Master reset input (active HIGH)
16	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
$\overline{CP}$	MR	Qn
↑	L	no change
↓	L	count
X	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

8-channel analog multiplexer/demultiplexer 74HC/HCT4051

FEATURES

- Wide analog input voltage range: ±5V
- Low "ON" resistance:
  80Ω (typ.) at $V_{CC} - V_{EE} = 4.5V$
  70Ω (typ.) at $V_{CC} - V_{EE} = 6.0V$
  60Ω (typ.) at $V_{CC} - V_{EE} = 9.0V$
- Logic level translation:
  to enable 5V logic to communicate with ±5V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- I_{CC} category: MSI

APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

GENERAL DESCRIPTION

The 74HC/HCT4051 are high-speed Si-gate CMOS devices and are pin compatible with the "4051" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4051 are 8-channel analog multiplexers/demultiplexers with three digital select inputs (S0 to S2), an active LOW enable input ($\overline{E}$), eight independent inputs/outputs (Y0 to Y7) and a common input/output (Z).

With $\overline{E}$ LOW, one of the eight switches is selected (low impedance ON-state) by S0 to S2. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of S0 to S2.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S0 to S2, and $\overline{E}$). The V_{CC} to GND ranges are 2.0 to 10.0V for HC and 4.5 to 5.5V for HCT. The analog inputs/outputs (Y0 to Y7, and Z) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 10.0V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

QUICK REFERENCE DATA

$V_{EE} = GND = 0V$; $T_{AMB} = 25°C$; $t_r = t_f = 6ns$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZH} t_{PZL}	Turn "ON" time $\overline{E}$ to V_{OS} Sn to V_{OS}	$C_L = 15pF$ $R_L = 1k\Omega$ $V_{CC} = 5V$	 22 20	 22 24	 ns ns
t_{PHZ} t_{PLZ}	Turn "OFF" time $\overline{E}$ to V_{OS} Sn to V_{OS}		 18 19	 16 20	 ns ns
C_I	Input capacitance		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per switch	Notes 1 and 2	25	25	pF
C_S	Max. switch capacitance independent (Y) common (Z)		 5 25	 5 25	 pF pF

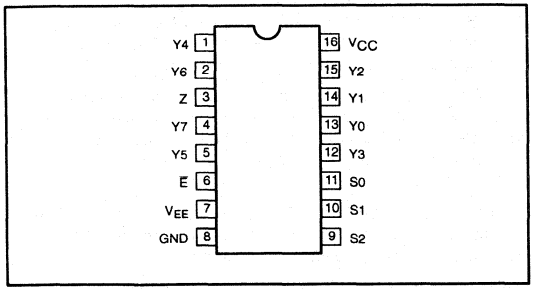
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\sum \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of outputs
   C_L = output load capacitance in pF
   C_S = maximum switch capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to $V_{CC} - 1.5V$

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE		DRAWING NUMBER
		HC	HCT	
16-pin plastic DIP	−40 to +125°C	74HC4051N	74HCT4051N	SOT38-1
16-pin plastic SO	−40 to +125°C	74HC4051D	74HCT4051D	SOT109-1
16-pin plastic SSOP Type II	−40 to +125°C	74HC4051DB	74HCT4051DB	SOT338-1
16-pin plastic TSSOP Type III	−40 to +125°C	74HC4051PW	74HCT4051PW	SOT403-1

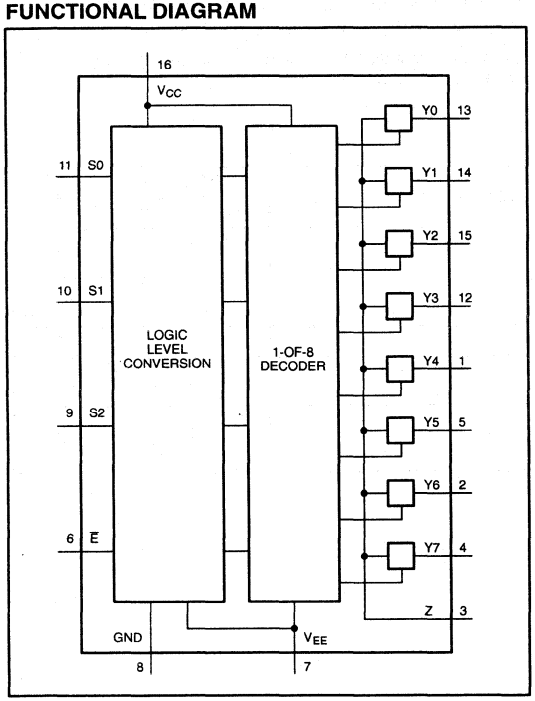
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
3	Z	Common input/output
6	$\overline{E}$	Enable input (active LOW)
7	V_{EE}	Negative supply voltage
8	GND	Ground (0V)
11, 10, 9	S0 to S2	Select inputs
13, 14, 15, 12, 1, 5, 2, 4	Y0 to Y7	Independent inputs/outputs
16	V_{CC}	Positive supply voltage

FUNCTIONAL DIAGRAM



FUNCTION TABLE

INPUTS				CHANNEL ON
$\overline{E}$	S2	S1	S0	
L	L	L	L	Y0 – Z
L	L	L	H	Y1 – Z
L	L	H	L	Y2 – Z
L	L	H	H	Y3 – Z
L	H	L	L	Y4 – Z
L	H	L	H	Y5 – Z
L	H	H	L	Y6 – Z
L	H	H	H	Y7 – Z
H	X	X	X	none

H = HIGH voltage level
L = LOW voltage level
X = Don't care

Dual 4-channel analog multiplexer/demultiplexer 74HC/HCT4052

FEATURES

- Wide analog input voltage range: ±5V
- Low "ON" resistance:
  80Ω (typ.) at $V_{CC} - V_{EE} = 4.5V$
  70Ω (typ.) at $V_{CC} - V_{EE} = 6.0V$
  60Ω (typ.) at $V_{CC} - V_{EE} = 9.0V$
- Logic level translation:
  to enable 5V logic to communicate with ±5V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- I_{CC} category: MSI

APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

GENERAL DESCRIPTION

The 74HC/HCT4052 are high-speed Si-gate CMOS devices and are pin compatible with the "4052" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4052 are dual 4-channel analog multiplexers/demultiplexers with common select logic. Each multiplexer has four independent inputs/outputs (nY0 to nY3) and a common input/output (nZ). The common channel select logics include two digital select inputs (S0 and S1) and an active LOW enable input ($\overline{E}$).

With $\overline{E}$ LOW, one of the four switches is selected (low impedance ON-state) by S0 and S1. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of S0 and S1.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S0 and S1, and $\overline{E}$). The V_{CC} to GND ranges are 2.0 to 10.0V for HC and 4.5 to 5.5V for HCT. The analog inputs/outputs (nY0 to nY3, and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 10.0V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

QUICK REFERENCE DATA

V_{EE} = GND = 0V; T_{AMB} = 25°C; $t_r = t_f$ = 6ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZH} t_{PZL}	Turn "ON" time $\overline{E}$ or Sn to V_{OS}	C_L = 15pF R_L = 1kΩ V_{CC} = 5V	28	18	ns
t_{PHZ} t_{PLZ}	Turn "OFF" time $\overline{E}$ or Sn to V_{OS}		21	13	ns
C_I	Input capacitance		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per switch	notes 1 and 2	57	57	pF
C_S	Max. switch capacitance independent (Y) common (Z)		5 12	5 12	pF pF

NOTES:

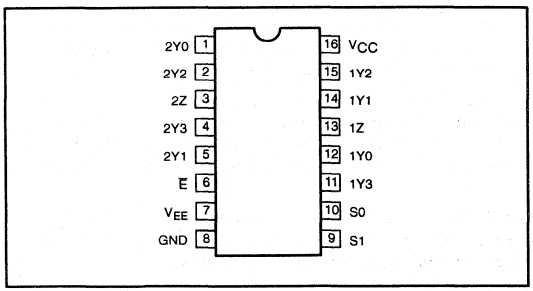
1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\sum \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of outputs
   C_L = output load capacitance in pF
   C_S = maximum switch capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5V

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE		DRAWING NUMBER
		HC	HCT	
16-pin plastic DIP	–40 to +125°C	74HC4052N	74HCT4052N	SOT38-1
16-pin plastic SO	–40 to +125°C	74HC4052D	74HCT4052D	SOT109-1
16-pin plastic SSOP Type II	–40 to +125°C	74HC4052DB	74HCT4052DB	SOT338-1
16-pin plastic TSSOP Type III	–40 to +125°C	74HC4052PW	74HCT4052PW	SOT403-1

Dual 4-channel analog multiplexer/demultiplexer 74HC/HCT4052

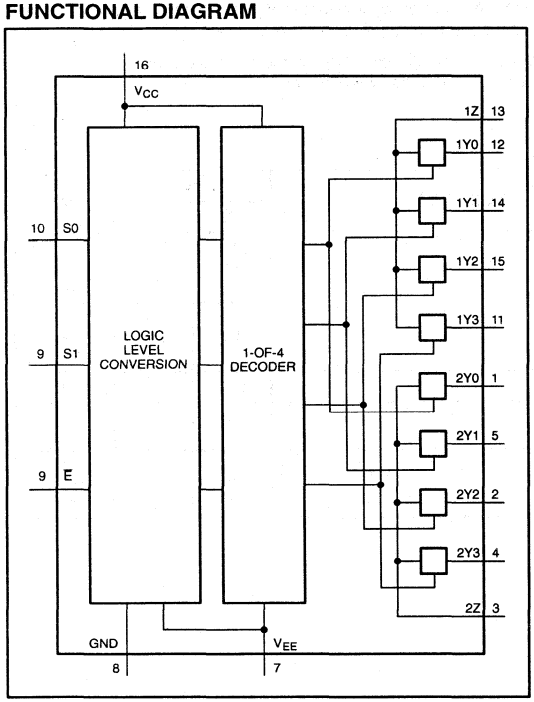
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 5, 2, 4	2Y0 to 2Y3	Independent inputs/outputs
6	$\overline{E}$	Enable input (active LOW)
7	V_{EE}	Negative supply voltage
8	GND	Ground (0V)
10, 9	S0, S1	Select inputs
12, 14, 15, 11	1Y0 to 1Y3	Independent inputs/outputs
13, 3	1Z, 2Z	Common inputs/outputs
16	V_{CC}	Positive supply voltage

FUNCTIONAL DIAGRAM



FUNCTION TABLE

INPUTS			CHANNEL ON
$\overline{E}$	S1	S0	
L	L	L	nY0 – nZ
L	L	H	nY1 – nZ
L	H	L	nY2 – nZ
L	H	H	nY3 – nZ
H	X	X	none

H = HIGH voltage level
L = LOW voltage level
X = Don't care

Triple 2-channel analog multiplexer/demultiplexer 74HC/HCT4053

FEATURES

- Low "ON" resistance:
  80Ω (typ.) at $V_{CC} - V_{EE} = 4.5V$
  70Ω (typ.) at $V_{CC} - V_{EE} = 6.0V$
  60Ω (typ.) at $V_{CC} - V_{EE} = 9.0V$
- Logic level translation:
  to enable 5V logic to communicate with ±5V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- I_{CC} category: MSI

APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

GENERAL DESCRIPTION

The 74HC/HCT4053 are high-speed Si-gate CMOS devices and are pin compatible with the "4053" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4053 are triple 2-channel analog multiplexers/demultiplexers with a common enable input ($\overline{E}$). Each multiplexer/demultiplexer has two independent inputs/outputs (nY0 and nY1), a common input/output (nZ) and three digital select inputs (S1 to S3).

With $\overline{E}$ LOW, one of the two switches is selected (low impedance ON-state) by S1 to S3. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of S1 to S3.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S1 to S3, and $\overline{E}$). The V_{CC} to GND ranges are 2.0 to 10.0V for HC and 4.5 to 5.5V for HCT. The analog inputs/outputs (nY0 and nY1, and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 10.0V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

QUICK REFERENCE DATA

V_{EE} = GND = 0V; T_{AMB} = 25°C; $t_r = t_f$ = 6ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZH} t_{PZL}	Turn "ON" time $\overline{E}$ to V_{OS} Sn to V_{OS}	C_L = 15pF R_L = 1kΩ V_{CC} = 5V	 17 21	 23 21	 ns ns
t_{PHZ} t_{PLZ}	Turn "OFF" time $\overline{E}$ to V_{OS} Sn to V_{OS}		 18 17	 20 19	 ns ns
C_I	Input capacitance		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per switch	Notes 1 and 2	36	36	pF
C_S	Max. switch capacitance independent (Y) common (Z)		 5 8	 5 8	 pF pF

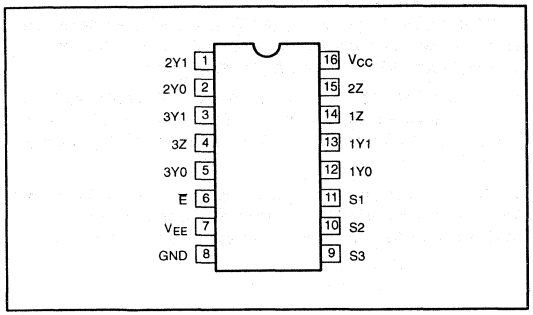
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\sum \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of outputs
   C_L = output load capacitance in pF
   C_S = maximum switch capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5V

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE		DRAWING NUMBER
		HC	HCT	
16-pin plastic DIP	–40 to +125°C	74HC4053N	74HCT4053N	SOT38-1
16-pin plastic SO	–40 to +125°C	74HC4053D	74HCT4053D	SOT109-1
16-pin plastic SSOP Type II	–40 to +125°C	74HC4053DB	74HCT4053DB	SOT338-1
16-pin plastic TSSOP Type III	–40 to +125°C	74HC4053PW	74HCT4053PW	SOT403-1

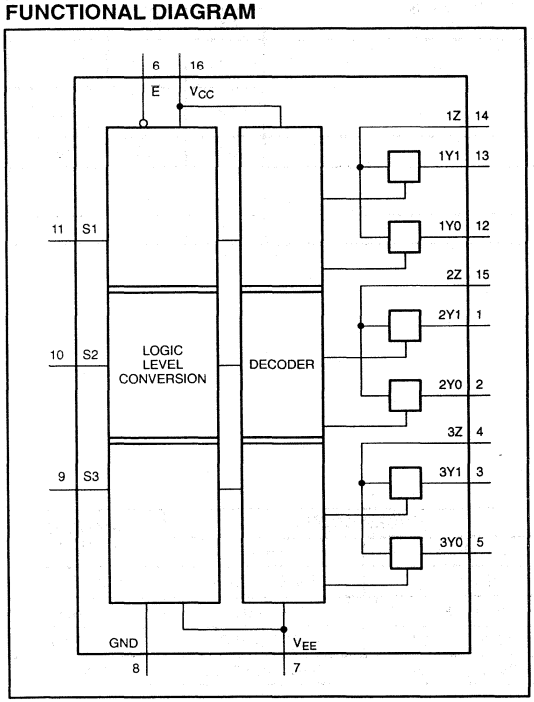
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 1	2Y0, 2Y1	Independent inputs/outputs
5, 3	3Y0, 3Y1	Independent inputs/outputs
6	$\overline{E}$	Enable input (active LOW)
7	V_{EE}	Negative supply voltage
8	GND	Ground (0V)
11, 10, 9	S1 to S3	Select inputs
12, 13	1Y0, 1Y1	Independent inputs/outputs
14, 15, 4	1Z to 3Z	Common inputs/outputs
16	V_{CC}	Positive supply voltage

FUNCTIONAL DIAGRAM



FUNCTION TABLE

INPUTS		CHANNEL ON
$\overline{E}$	Sn	
L	L	nY0 – nZ
L	H	nY1 – nZ
H	X	none

H = HIGH voltage level
L = LOW voltage level
X = don't care

Quad bilateral switches | 74HC/HCT4066

FEATURES

- Very low "ON" resistance:
  - 50Ω (typ.) at $V_{CC} - V_{EE} = 4.5V$
  - 45Ω (typ.) at $V_{CC} - V_{EE} = 6.0V$
  - 35Ω (typ.) at $V_{CC} - V_{EE} = 9.0V$
- Output capability: non-standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT4066 are high-speed Si-gate CMOS devices and are pin compatible with the "4066" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4066 have four independent analog switches. Each switch has two input/output terminals (nY, nZ) and an active HIGH enable input (nE). When nE is LOW the belonging analog switch is turned off.

The 74HC/HCT4066 is pin compatible with the 74HC/HCT4016, but exhibits a much lower "ON" resistance. In addition, the "ON" resistance is relatively constant over the full input signal range.

QUICK REFERENCE DATA

$V_{EE} = GND = 0V$; $T_{AMB} = 25°C$; $t_r = t_f = 6ns$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZH}/t_{PZL}	Turn "ON" time nE to V_{OS}	$C_L = 15pF$, $R_L = 1k\Omega$, $V_{CC} = 5V$	11	12	ns
t_{PHZ}/t_{PLZ}	Turn "OFF" time nE to V_{OS}		13	16	ns
C_I	Input capacitance		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per switch	Notes 1 and 2	11	12	pF
C_S	Max. switch capacitance		8	8	pF

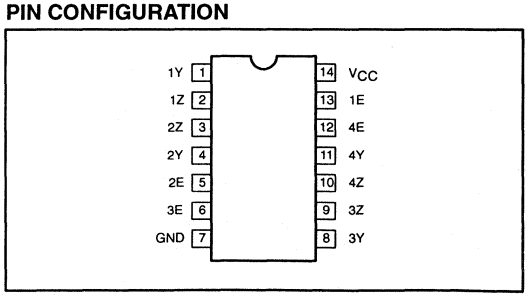
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of outputs
   C_L = output load capacitance in pF
   C_S = maximum switch capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to $V_{CC} - 1.5V$

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE		DRAWING NUMBER
		HC	HCT	
14-pin plastic DIP	–40 to +125°C	74HC4066N	74HCT4066N	SOT27-1
14-pin plastic SO	–40 to +125°C	74HC4066D	74HCT4066D	SOT108-1
14-pin plastic SSOP Type II	–40 to +125°C	74HC4066DB	74HCT4066DB	SOT337-1
14-pin plastic TSSOP Type III	–40 to +125°C	74HC4066PW	74HCT4066PW	SOT402-1

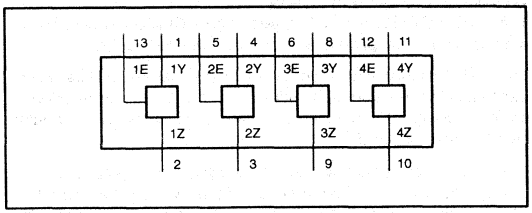
PIN CONFIGURATION



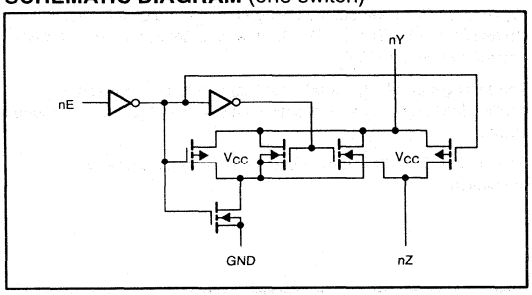
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 8, 11	1Y to 4Y	Independent inputs/outputs
2, 3, 9, 10	1Z to 4Z	Independent inputs/outputs
7	GND	Ground (0V)
13, 5, 6, 12	1E to 4E	Enable inputs (active HIGH)
14	V_{CC}	Positive supply voltage

FUNCTIONAL DIAGRAM



SCHEMATIC DIAGRAM (one switch)



FUNCTION TABLE

INPUT nE	SWITCH
L	off
H	on

H = High voltage level
L = Low voltage level

Quad bilateral switches | 74HC/HCT4316

FEATURES

- Low "ON" resistance:
  160Ω (typ.) at $V_{CC} - V_{EE} = 4.5V$
  120Ω (typ.) at $V_{CC} - V_{EE} = 6.0V$
  80Ω (typ.) at $V_{CC} - V_{EE} = 9.0V$
- Logic level translation:
  to enable 5V logic to communicate with ±5V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- I_{CC} category: MSI

APPLICATIONS

- Signal gating
- Modulation
- Demodulation
- Chopper

GENERAL DESCRIPTION

The 74HC/HCT4316 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4316 have four independent analog switches. Each switch has two input/output terminals (nY, nZ) and an active HIGH select input (nS). When the enable input ($\overline{E}$) is HIGH, all four analog switches are turned off.

Current through a switch will not cause additional V_{CC} current provided the voltage at ther temrinals of the switch is maintianed within the supply voltage range; $V_{CC} \geqslant (V_Y, V_Z) \geqslant V_{EE}$. Inputs nY and nZ are electrically equivalent terminals.

V_{CC} and GND are the supply voltage pins for the digital control inputs ($\overline{E}$ and nS). The V_{CC} to GND ranges are 2.0 to 10.0V for HC and 4.5 to 5.5V for HCT.

The analog inputs/outputs (nY and NZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 10.0V.

See the 74HC/HCT4016 for the version without logic level translation.

QUICK REFERENCE DATA

$V_{EE} = GND = 0V$; $T_{AMB} = 25°C$; $t_r = t_f = 6ns$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZH}	Turn "ON" time $\overline{E}$ to V_{OS} nS to V_{OS}	$C_L = 15pF$ $R_L = 1k\Omega$ $V_{CC} = 5V$	 19 16	 19 17	 ns ns
t_{PZL}	Turn "ON" time $\overline{E}$ to V_{OS} nS to V_{OS}		 19 16	 24 21	 ns ns
t_{PHZ}/ t_{PLZ}	Turn "OFF" time $\overline{E}$ to V_{OS} nS to V_{OS}		 20 16	 21 19	 ns ns
C_I	Input capacitance		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per switch	Notes 1 and 2	13	14	pF
C_S	Max. switch capacitance		5	5	pF

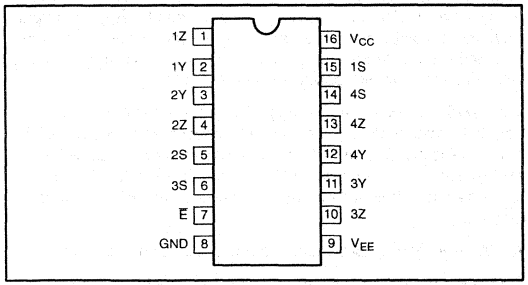
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:
   f_i = input frequency in MHz; f_o = output frequency in MHz
   $\sum \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of outputs
   C_L = output load capacitance in pF; C_S = maximum switch capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to $V_{CC} - 1.5V$

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE		DRAWING NUMBER
		HC	HCT	
16-pin plastic DIP	–40 to +125°C	74HC4316N	74HCT4316N	SOT38-1
16-pin plastic SO	–40 to +125°C	74HC4316D	74HCT4316D	SOT109-1
16-pin plastic SSOP Type II	–40 to +125°C	74HC4316DB	74HCT4316DB	SOT338-1
16-pin plastic TSSOP Type III	–40 to +125°C	74HC4316PW	74HCT4316PW	SOT403-1

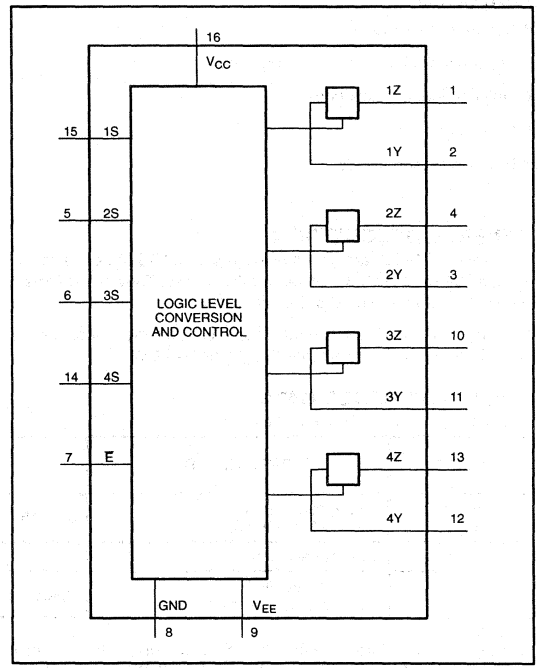
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1Z to 4Z	Independent inputs/outputs
2, 3, 11, 12	1Y to 4Y	Independent inputs/outputs
7	$\overline{E}$	Enable input (active LOW)
8	GND	Ground (0V)
9	V_{EE}	Negative supply voltage
15, 5, 6, 14	1S to 4S	Select inputs (active HIGH)
16	V_{CC}	Positive supply voltage

FUNCTIONAL DIAGRAM



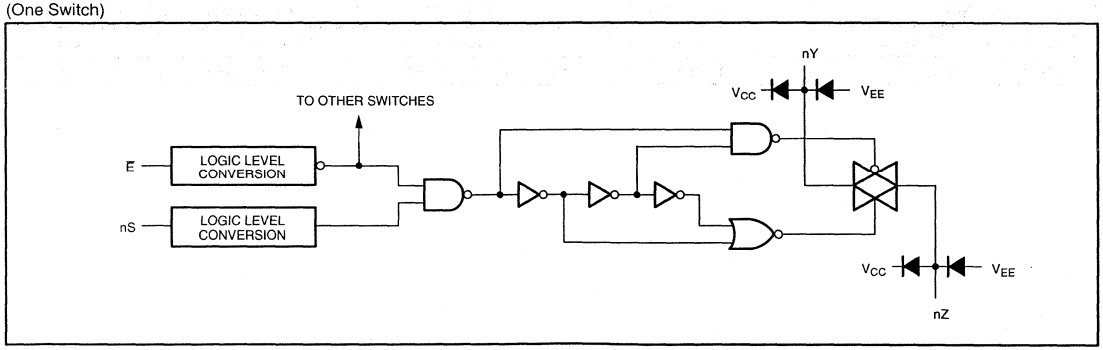
FUNCTION TABLE

INPUTS		SWITCH
$\overline{E}$	nS	
L	L	off
L	H	on
H	X	off

H = HIGH voltage level
L = LOW voltage level
X = Don't care

SCHEMATIC DIAGRAM

(One Switch)



Dual retriggerable precision monostable multivibrator

74HC/HCT4538

FEATURES

- Separate reset inputs
- Triggering from leading or trailing edge
- Output capability: standard
- I_{CC} category: MSI
- Power-on reset on-chip

GENERAL DESCRIPTION

The 74HC/HCT4538 are high-speed Si-gate CMOS devices and are pin compatible with "4538" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4538 are dual retriggerable-resettable monostable multivibrators. Each multivibrator has an active LOW trigger/retrigger input ($n\overline{A}0$), an active HIGH trigger/retrigger input (nA1), an overriding active LOW direct reset input ($n\overline{R}_D$), an output (nQ) and its complement ($n\overline{Q}$), and two pins (nC_{TC} and nRC_{TC}) for connecting the external timing components C_t and R_t. Typical pulse width variation over temperature range is ±0.2%.

The 74HC/HCT4538 may be triggered by either the positive or the negative edges of the input pulse. The duration and accuracy of the output pulse are determined by the external timing components C_t and R_t. The output pulse width (T) is equal to $0.7 \times R_t \times C_t$. The linear design techniques guarantee precise control of the output pulse width.

A LOW level at $n\overline{R}_D$ terminates the output pulse immediately.

Schmitt-trigger action in the trigger inputs makes the circuit highly tolerant to slower rise and fall times.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 6ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	Propagation delay $n\overline{A}0$, nA1 to nQ, $n\overline{Q}$	C_L = 15pF; V_{CC} = 5V	27	30	ns
C_I	Input capacitance		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per multivibrator	Notes 1 and 2	136	138	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) + 0.48 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 0.8 \times V_{CC}$ where:
   f_i = input frequency in MHz; f_o = output frequency in MHz
   C_L = output load capacitance in pF; V_{CC} = supply voltage in V
   D = duty factor in %; C_{EXT} = timing capacitance in pF
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs
2. For HC the condition V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5V

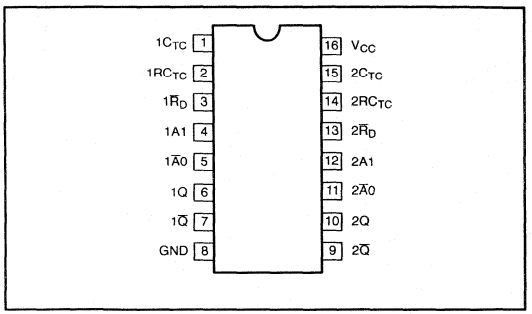
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE		DRAWING NUMBER
		HC	HCT	
16-pin plastic DIP	−40 to +125°C	74HC4538N	74HCT4538N	SOT38-1
16-pin plastic SO	−40 to +125°C	74HC4538D	74HCT4538D	SOT109-1
16-pin plastic SSOP Type II	−40 to +125°C	74HC4538DB	74HCT4538DB	SOT338-1
16-pin plastic TSSOP Type III	−40 to +125°C	74HC4538PW	74HCT4538PW	SOT403-1

Dual retriggerable precision monostable multivibrator

74HC/HCT4538

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 15	$1C_{TC}$, $2C_{TC}$	External capacitor connections
2, 14	$1RC_{TC}$, $2RC_{TC}$	External resistor/capacitor connections
3, 13	$1\overline{R}_D$, $2\overline{R}_D$	Direct reset inputs (active LOW)
4, 12	1A1, 2A1	Tirgger inputs (LOW-to-HIGH, edge-triggered)
5, 11	$1\overline{A}0$, $2\overline{A}0$	Tirgger inputs (HIGH-to-LOW, edge-triggered)
6, 10	1Q, 2Q	Pulse outputs
7, 9	$1\overline{Q}$, $2\overline{Q}$	Complementary pulse outputs
8	GND	Ground (0V)
16	V_{CC}	Positive supply voltage

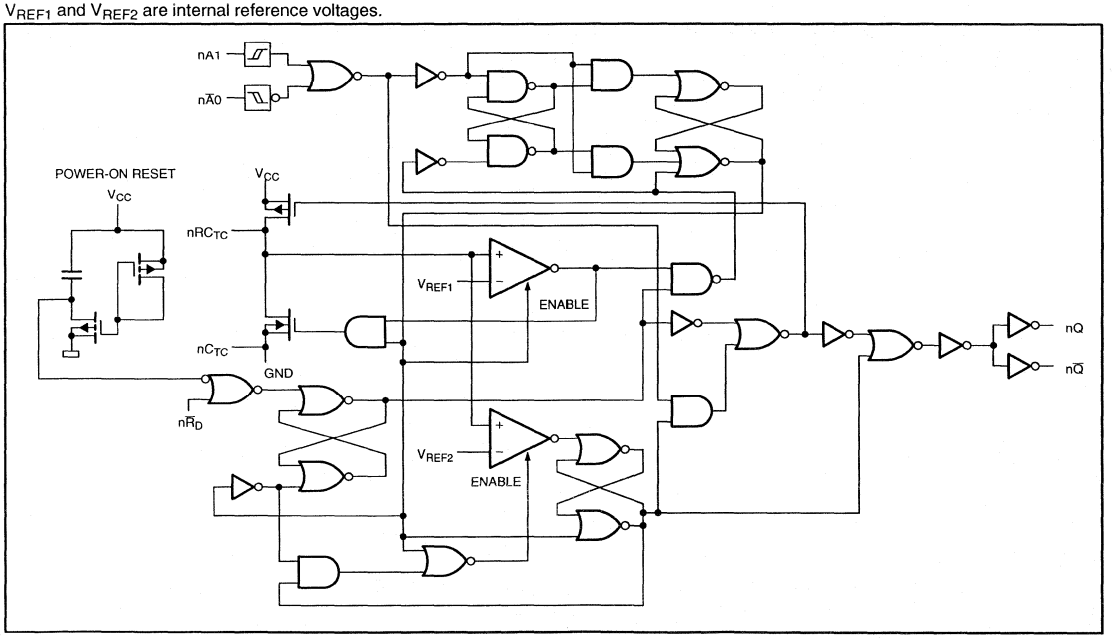
FUNCTION TABLE

INPUTS			OUTPUTS	
$n\overline{A}0$	nA1	$n\overline{R}_D$	nQ	$n\overline{Q}$
↓	L	H	⎍	⎎
H	↑	H	⎍	⎎
X	X	L	L	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
⎍ = one HIGH level output pulse
⎎ = one LOW level output pulse

LOGIC DIAGRAM

V_{REF1} and V_{REF2} are internal reference voltages.



HCMOS Netlists

HCMOS BERKELEY SPICE MODELS

```
* HCT.CIR
* HC AND HCT PRODUCT FAMILY
* STANDARD LOGIC PRODUCT GROUP
* PHILIPS SEMICONDUCTORS
* 3/28/95
*-------------------------------------------------------------*
*SIMULATION MODULES OF CMOS LOGIC PARTS OF PHILIPS HCMOS FAMILY*
*                    BERKELEY SPICE FORMAT                    *
*-------------------------------------------------------------*
* IN ORDER TO SIMULATE A SPECIFIC HCMOS DEVICE, GO TO THE END  *
* OF THE FILE UNDER HEADING 'START RUNNING CIRCUIT MODEL' AND  *
* REMOVE THE COMMENT STATEMENT '*' BEFORE THE REQUIRED DEVICE. *
* ALL OTHER DEVICES MUST HAVE AN '*' COMMENT STATEMENT.        *
* IF YOU LIKE TO SIMULATE WITH FAST OR SLOW PARAMETERS, GO TO  *
* HEADING 'PROCESS MODELS' AND REMOVE THE COMMENT STATEMENT '*'*
* BEFORE THE REQUIRED PROCESS MODEL.                           *
* YOU MAY ONLY SIMULATE ONE DEVICE AT THE TIME.                *
* THE LOAD CIRCUIT AND SIMULATION TIMING SHOULD NORMALLY BE    *
* ADAPTED TO YOUR SPECIFIC SITUATION.                          *
*-------------------------------------------------------------*

*****************************************************************
*                                                               *
* These HCMOS models represent only one data input and one output*
* of the device. Devices with a 3-state output buffer also have  *
* an Output Enable (OE) input. The LV138 also has an Input Enable*
* (EN) input. Other control inputs such as DIR or CLK inputs are *
* not modeled. Circuitry between the input and output buffers are*
* also omitted, such as gates, registers, latches, mux's and     *
* intermediate buffers. One result of this is that LV models do  *
* not show the exact function of the device.  Another result of  *
* this is that propagation delays in SPICE will not necessarily  *
* match with the published AC timing specifications in the device*
* datasheet.                                                    *
*                                                               *
*****************************************************************

***********************************************************

.OPTIONS  ACCT   LIST  OPTS  ITL5=25000  NOMOD

* Nominal parameters
.INC c:\spice\HCMOS\hc_tnomi.cir

* Fast parameters
*.INC c:\spice\HCMOS\hc_tfast.cir

* Slow parameters
*.INC c:\spice\HCMOS\hc_tslow.cir

*************  START RUNNING CIRCUIT MODEL  **************

*XHC00     2  3  1  0        INV2
*XHCT00    2  3  1  0        INV2T
*XHC04     2  3  1  0        INV0
*XHCT04    2  3  1  0        INV0T
*XHC14     2  3  1  0        INVSMT
*XHCT14    2  3  1  0        INVSMTT
*XHC32     2  3  1  0        NINV1
*XHCT32    2  3  1  0        NINV1T
```

```
*XHC74      2   3   1   0          INV1
*XHCT74     2   3   1   0          INV1T
*XHC123     2   3   1   0          INV1
*XHCT123    2   3   1   0          INV1T
*XHC132     2   3   1   0          INVSMT
*XHCT132    2   3   1   0          INVSMTT
*XHC138     2   5   3   1   0      NANDINV
*XHCT138    2   5   3   1   0      NANDINVT
*XHC161     2   3   1   0          INV2
*XHCT161    2   3   1   0          INV2T
*XHC163     2   3   1   0          INV2
*XHCT163    2   3   1   0          INV2T
*XHC244     2   5   3   1   0      NINV3
XHCT244    2   5   3   1   0      NINV3T
*XHC245     2   5   3   1   0      NINV3
*XHCT245    2   5   3   1   0      NINV3T
*XHC273     2   3   1   0          NINV1
*XHCT273    2   3   1   0          NINV1T
*XHC373     2   5   3   1   0      NINV3
*XHCT373    2   5   3   1   0      NINV3T
*XHC374     2   5   3   1   0      NINV3
*XHCT374    2   5   3   1   0      NINV3T
*XHC595     2   5   3   1   0      NINV3
*XHCT595    2   5   3   1   0      NINV3T
*XHC4040    2   3   1   0          NINV1
*XHCT4040   2   3   1   0          NINV1T
*XHC4051    2   3   4   5   1   0  SWI1
*XHCT4051   2   3   4   5   1   0  SWI1T
*XHC4052    2   3   4   5   1   0  SWI1
*XHCT4052   2   3   4   5   1   0  SWI1T
*XHC4053    2   3   4   5   1   0  SWI1
*XHCT4053   2   3   4   5   1   0  SWI1T
*XHC4066    2   3   4   1   0      SWI2
*XHCT4066   2   3   4   1   0      SWI2T
*XHC4316    2   3   4   5   1   0  SWI3
*XHCT4316   2   3   4   5   1   0  SWI3T
*XHC4538    2   3   1   0          INVSMT
*XHCT4538   2   3   1   0          INVSMTT

********************** EXTERNAL TEST LOAD ************************
*R1   3   1   1K
* Use only for 3-state Tplz

*R1   3   0   1K
* Use only for 3-state Tphz

R1   3   0   1K
C1   3   0   50P
*********************************************************************

VCC    1   0   DC    4.5
VIN1   2   0   PULSE 0   4.5   5N   6N   6N   40N   80N

VEN    5   0   DC    0.0
* Use for HC(T)138/244/245/373/374/595
```

```
***************************** SWITCH *******************************

****Use ONLY with TRAN. ANAL. (4051 / 4052 / 4053 / 4066 / 4316)****

*VCC   1  0  DC    4.5
*VIN1  2  0  PULSE 0  4.5  5N  6N  6N  80N  100N
*VIN2  3  0  DC    4.5

*VEE   5  0  DC    0.0
*Do not use with 4066

*RZ    4  0  1K
*CL    4  0  50P
************************************************************************

* Use this part only for 4051 - 4053 and the 4316 Ron calculations *
*VEE   5  0  DC  -4.5
*VIN2  2  0  DC   4.5

*VIN3  3  5  PULSE 0  4.5  5N  6N  6N  40N  80N
*Only for TRAN

*VIN4  3  5  DC   9.0
*ILAST 4  5  DC   1mA
*C2    4  0  50P
************************************************************************

******* Use this part only for the 4066 Ron calculations ***********
*VIN2  2  0  DC   4.5

*VIN3  3  0  PULSE 0  4.5  5N  6N  6N  40N  80N
*Only for TRAN

*VIN4  3  0  DC   4.5
*ILAST 4  0  DC   1mA
*C2    4  0  50P
************************************************************************

.TRAN  1N   80N
.PRINT TRAN  V(2)  V(3)

*PRINT TRAN  V(2)  V(4)
*Only for 4051 - 4316 with TRAN analyse

.PROBE V(2)  V(3)
.END
```

HC_TNOMI.CIR Subcircuit

```
* HCMOS Subcircuit and Primitive Elements Library
* HC_TNOMI.CIR
* Nominal Process Corner
* Standard Logic Product Group
* Philips Semiconductors
* 3/28/95
************************************************
*          NOMINAL N-Channel Transistor        *
*             UCB-3 Parameter Set              *
*          HIGH-SPEED CMOS Logic Family        *
*                 10-Jan.-1995                 *
************************************************
.Model MHCNEN NMOS
+LEVEL = 3
+KP    = 45.3E-6
+VTO   = 0.72
+TOX   = 51.5E-9
+NSUB  = 2.8E15
+GAMMA = 0.94
+PHI   = 0.65
+VMAX  = 150E3
+RS    = 40
+RD    = 40
+XJ    = 0.11E-6
+LD    = 0.52E-6
+DELTA = 0.315
+THETA = 0.054
+ETA   = 0.025
+KAPPA = 0.0
+WD    = 0.0

************************************************
*          NOMINAL P-Channel transistor        *
*             UCB-3 Parameter Set              *
*           HIGH-SPEED CMOS Logic Family       *
*                 10-Jan.-1995                 *
************************************************
.Model MHCPEN PMOS
+LEVEL = 3
+KP    = 22.1E-6
+VTO   = -0.71
+TOX   = 51.5E-9
+NSUB  = 3.3E16
+GAMMA = 0.92
+PHI   = 0.65
+VMAX  = 970E3
+RS    = 80
+RD    = 80
+XJ    = 0.63E-6
+LD    = 0.23E-6
+DELTA = 2.24
+THETA = 0.108
+ETA   = 0.322
+KAPPA = 0.0
+WD    = 0.0

.MODEL  INT D
```

```
****************************************
*   START OF SUB-CIRCUIT DESCRIPTION   *
*            MARCH 28, 1995            *
****************************************

*****NOMIN.CIR*****

.SUBCKT INP0N  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2  3  100
MP1 3 50 50 50  MHCPEN W=20U L=2.4U AD=100P AS=100P PD=40U PS= 20U
MN1 3 60 60 60  MHCNEN W=35U L=2.4U AD=260P AS=260P PD=70U PS= 20U
.ENDS

.SUBCKT INP1N  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MHCPEN W=20U L=2.4U AD=100P AS=100P PD=40U PS= 20U
MN1 4 60 60 60  MHCNEN W=35U L=2.4U AD=260P AS=260P PD=70U PS= 20U
MP2 3  4 50 50  MHCPEN W=88U L=2.4U AD=290P AS=550P PD=10U PS=100U
MN2 3  4 60 60  MHCNEN W=56U L=2.4U AD=162P AS=550P PD=10U PS= 75U
.ENDS

.SUBCKT INP1TN  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MHCPEN W= 20U L=2.4U AD=100P AS=100P PD= 40U PS= 20U
MN1 4 60 60 60  MHCNEN W= 35U L=2.4U AD=260P AS=260P PD= 70U PS= 20U
MP2 3  4  5 50  MHCPEN W= 88U L=2.4U AD=290P AS=550P PD=107U PS=195U
MN2 3  4 60 60  MHCNEN W= 56U L=2.4U AD=162P AS=550P PD= 55U PS=162U
D1 50  5  INT
MP4 3  6 50 50  MHCPEN W=6.4U L=4.0U AD= 60P AS= 60P PD=13U PS= 24U
MN4 3  4 60 60  MHCNEN W=185U L=2.4U AD=740P AS=740P PD=50U PS=185U
MP5 6  3 50 50  MHCPEN W=6.4U L=3.2U AD= 50P AS= 50P PD=10U PS= 20U
MN5 6  3 60 60  MHCNEN W=6.4U L=3.2U AD= 50P AS= 50P PD=10U PS= 20U
.ENDS

.SUBCKT INP2N  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MHCPEN W= 20U L=2.4U AD=100P AS=100P PD=40U PS= 20U
MN1 4 60 60 60  MHCNEN W= 35U L=2.4U AD=260P AS=260P PD=70U PS= 20U
MP2 3  4 50 50  MHCPEN W=176U L=2.4U AD=580P AS=580P PD=10U PS=200U
MN2 3  4 60 60  MHCNEN W=112U L=2.4U AD=325P AS=580P PD=10U PS=150U
.ENDS

.SUBCKT INP2TN  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MHCPEN W= 20U L=2.4U AD=100P AS= 100P PD=40U PS= 20U
MN1 4 60 60 60  MHCNEN W= 35U L=2.4U AD=260P AS= 260P PD=70U PS= 20U
MP2 3  4  5 50  MHCPEN W=176U L=2.4U AD=580P AS=1100P PD=10U PS=200U
MN2 3  4 60 60  MHCNEN W=112U L=2.4U AD=325P AS=1100P PD=10U PS=150U
D1 50  5   INT
MP4 3  6 50 50  MHCPEN W=6.4U L=4.0U AD= 60P AS= 60P PD=13U PS= 24U
MN4 3  4 60 60  MHCNEN W=348U L=2.4U AD=740P AS=740P PD=50U PS=348U
MP5 6  3 50 50  MHCPEN W=6.4U L=3.2U AD= 50P AS= 50P PD=10U PS= 20U
MN5 6  3 60 60  MHCNEN W=6.4U L=3.2U AD= 50P AS= 50P PD=10U PS= 20U
.ENDS
```

```
.SUBCKT SMT1N  2  3  50  60
* SCHMITT-TRIGGER INPUT FOR HC14 CMOS INPUT LEVELS
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MHCPEN W=20U L=2.4U AD=100P AS=100P PD=40U PS=20U
MN1 4 60 60 60  MHCNEN W=35U L=2.4U AD=140P AS=140P PD=50U PS=35U
MP2 5  4 50 50  MHCPEN W=36U L=2.4U AD=140P AS=140P PD=50U PS=35U
MN2 6  4 60 60  MHCNEN W=16U L=2.4U AD= 70P AS= 70P PD=15U PS=17U
MP3 3  4  5 50  MHCPEN W=44U L=2.4U AD=220P AS=220P PD=60U PS=44U
MN3 3  4  6  6  MHCNEN W=17U L=2.4U AD= 70P AS= 70P PD=15U PS=16U
MP4 5  3 60 50  MHCPEN W=36U L=2.4U AD=150P AS=150P PD=60U PS=36U
MN4 6  3 50  6  MHCNEN W= 6U L=  4U AD= 25P AS= 25P PD=10U PS= 6U
.ENDS

.SUBCKT SMTTL1N  2  3  50  60
* SCHMITT-TRIGGER INPUT FOR HCT14 WITH TTL INPUT LEVELS
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MHCPEN W= 20U L=2.4U AD= 100P AS= 100P PD= 40U PS= 20U
MN1 4 60 60 60  MHCNEN W= 35U L=2.4U AD= 140P AS= 140P PD= 50U PS= 35U
D1  50  7  INT
MP2 5  4  7  7  MHCPEN W= 36U L=2.4U AD= 140P AS= 140P PD= 50U PS= 35U
MN2 6  4 60 60  MHCNEN W=216U L=2.4U AD= 860P AS= 860P PD=140U PS=216U
MP3 3  4  5 50  MHCPEN W= 54U L=2.4U AD= 220P AS= 220P PD= 60U PS= 44U
MN3 3  4  6  6  MHCNEN W=257U L=2.4U AD=1000P AS=1000P PD=150U PS=257U
MP4 5  3 60 50  MHCPEN W= 32U L=  4U AD= 120P AS= 120P PD=100U PS= 32U
MN4 6  3 50  6  MHCNEN W= 14U L=  4U AD= 100P AS= 100P PD= 30U PS= 24U
MP5 8  3 50 50  MHCPEN W= 10U L=2.4U AD=  40P AS=  40P PD= 16U PS= 10U
MN5 8  3 60 60  MHCNEN W=  5U L=2.4U AD=  20P AS=  20P PD= 12U PS=  5U
MP6 3  8 50 50  MHCPEN W=  6U L=8.0U AD=  30P AS=  30P PD= 16U PS=  6U
.ENDS

.SUBCKT INVN   2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
MP1 3  2 50 50  MHCPEN W=364U L=2.4U AD=500P  AS=500P PD=10U PS=430U
MN1 3  2 60 60  MHCNEN W=184U L=2.4U AD=275P  AS=275P PD=10U PS=270U
.ENDS

.SUBCKT NANDN  2  3  4  50  60
*INTERNAL NAND
*IN1 = 2, IN2 = 3, OUT = 4, VCC= 50, GND = 60
MP1 4  2  50  50  MHCPEN W=112U  L=2.4U AD=150P AS=300P PD= 75U PS=150U
MP2 4  3  50  50  MHCPEN W=112U  L=2.4U AD=150P AS=300P PD= 75U PS=150U
MN1 4  2   5  60  MHCNEN W=300U  L=2.4U AD=300P AS=300P PD=300U PS=300U
MN2 5  3  60  60  MHCNEN W=300U  L=2.4U AD=300P AS=300P PD=300U PS=300U
.ENDS

.SUBCKT LLCN  2  3  40  50  60
* LEVEL CONVERTER
* INA = 2,  OUT = 3,  VEE = 40,  VCC = 50,  GND =  60
MP4 4  2  50  50  MHCPEN W= 30U  L= 2.4U AD=120P AS=120P PD= 40U PS= 30U
MN4 4  2  60  60  MHCNEN W= 15U  L= 2.4U AD= 60P AS= 60P PD= 20U PS= 15U
MP1 5  2  50  50  MHCPEN W=135U  L= 2.4U AD=500P AS=500P PD=100U PS=135U
MP2 6  2  50  50  MHCPEN W=135U  L= 2.4U AD=500P AS=500P PD=100U PS=135U
MN1 5  6  40  40  MHCNEN W=6.4U  L=18.8U AD= 25P AS= 25P PD= 20U PS=6.4U
MN2 6  5  40  40  MHCNEN W=6.4U  L=18.8U AD= 25P AS= 25P PD= 20U PS=6.4U
MP3 7  6  50  50  MHCPEN W= 10U  L= 4.0U AD= 40P AS= 40P PD= 20U PS= 10U
MN3 7  6  40  40  MHCNEN W=  5U  L= 4.0U AD= 20P AS= 20P PD= 10U PS=  5U
MP5 3  7  50  50  MHCPEN W= 30U  L= 2.4U AD=120P AS=120P PD= 40U PS= 30U
MN5 3  7  40  40  MHCNEN W= 15U  L= 2.4U AD= 60P AS= 60P PD= 20U PS= 15U
.ENDS
```

```
.SUBCKT SWITCH1N  2  8  9  40  50
* ANALOG SWITCH
* INPUT = 2,   Y = 8,  Z = 9,  VEE = 40,  VCC =50
MP1 3  2  50  50  MHCPEN W=  88U L=2.4U AD= 350P AS= 350P PD=100U PS=  88U
MN1 3  2  40  40  MHCNEN W=  56U L=2.4U AD= 225P AS= 225P PD= 70U PS=  56U
MP4 4  3  50  50  MHCPEN W= 350U L=2.4U AD= 900P AS= 900P PD=200U PS= 350U
MN4 4  3  40  40  MHCNEN W= 150U L=2.4U AD= 400P AS= 400P PD=100U PS= 150U
MP5 8  4   5  50  MHCPEN W= 216U L=2.4U AD= 900P AS= 900P PD=100U PS= 216U
MN5 8  3   5   5  MHCNEN W= 108U L=2.4U AD= 430P AS= 430P PD= 50U PS= 108U
MN6 5  4  40  40  MHCNEN W= 145U L=2.4U AD= 600P AS= 600P PD= 75U PS= 145U
MP7 9  4   8  50  MHCPEN W=1068U L=2.4U AD=2500P AS=2500P PD= 10U PS=1068U
MN7 9  3   8   5  MHCNEN W= 312U L=2.4U AD=1200P AS=1200P PD= 10U PS= 312U
.ENDS

.SUBCKT SWITCH2N  2  8  9  50  60
* ANALOG SWITCH
* INPUT= 2   Y= 8   Z= 9  VCC= 50   GND= 60
MP1 3  2  50  50  MHCPEN W=  88U L=2.4U AD= 350P AS= 350P PD=100U PS=  88U
MN1 3  2  60  60  MHCNEN W=  56U L=2.4U AD= 225P AS= 225P PD= 70U PS=  56U
MP4 4  3  50  50  MHCPEN W= 350U L=2.4U AD= 900P AS= 900P PD=200U PS= 350U
MN4 4  3  60  60  MHCNEN W= 150U L=2.4U AD= 400P AS= 400P PD=100U PS= 150U
MP5 5  3   8  50  MHCPEN W=  85U L=2.4U AD= 355P AS= 355P PD= 40U PS=  85U
MN5 5  4   8   5  MHCNEN W=  42U L=2.4U AD= 170P AS= 170P PD= 20U PS=  42U
MN6 5  3  60  60  MHCNEN W= 145U L=2.4U AD= 600P AS= 600P PD= 75U PS= 145U
MP7 9  3   8  50  MHCPEN W=1900U L=2.4U AD=2500P AS=2500P PD= 10U PS=1900U
MN7 9  4   8   5  MHCNEN W= 576U L=2.4U AD=1200P AS=1200P PD= 10U PS= 576U
.ENDS

.SUBCKT SWITCH3  2  8  9  40  50
* ANALOG SWITCHN
* INPUT = 2   Y = 8  Z = 9  VEE = 40  VCC = 50
MP1 3  2  50  50  MHCPEN W=  88U L=2.4U AD= 350P AS= 350P PD=100U PS=  88U
MN1 3  2  40  40  MHCNEN W=  56U L=2.4U AD= 225P AS= 225P PD= 70U PS=  56U
MP4 4  3  50  50  MHCPEN W= 350U L=2.4U AD= 900P AS= 900P PD=200U PS= 350U
MN4 4  3  40  40  MHCNEN W= 150U L=2.4U AD= 400P AS= 400P PD=100U PS= 150U
MP5 9  3   8  50  MHCPEN W=1168U L=2.4U AD=2730P AS=2730P PD= 10U PS=1168U
MN5 9  4   8  40  MHCNEN W= 312U L=2.4U AD=1200P AS=1200P PD= 10U PS= 312U
.ENDS

.SUBCKT BUSOUTPN  2   3   4   50   60
* INPUT = 2  OEN = 3 (LOW)  OUT = 4  VCC = 50  GND = 60
* 3-STATE BUS OUTPUT
MP1 5  3   50  50  MHCPEN W= 90U  L=2.4U AD= 360P AS= 360P PD= 30U PS=360U
MN1 5  3   60  60  MHCNEN W= 40U  L=2.4U AD= 160P AS= 160P PD= 20U PS= 40U
MP2 6  2   50  50  MHCPEN W=480U  L=2.4U AD=1800P AS=1800P PD=100U PS=480U
MN2 7  2   60  60  MHCNEN W=240U  L=2.4U AD=1000P AS=1000P PD= 50U PS=240U
MP3 7  3    6  50  MHCPEN W=280U  L=2.4U AD=1120P AS=1120P PD= 55U PS=280U
MN3 7  3   60  60  MHCNEN W=160U  L=2.4U AD= 640P AS= 640P PD= 40U PS=160U
MP4 6  5   50  50  MHCPEN W=240U  L=2.4U AD=1000P AS=1000P PD= 50U PS=240U
MN4 7  5    7  60  MHCNEN W=190U  L=2.4U AD= 760P AS= 760P PD= 45U PS=190U
R1  6  8  200
R2  7  9  200
MP5 4  8   50  50  MHCPEN W=540U  L=2.4U AD=1500P AS=1500P PD=10U PS=540U
MN5 4  9   60  60  MHCNEN W=233U  L=2.4U AD= 750P AS= 750P PD=10U PS=233U
R3  8  10 100
R4  9  11 100
MP6 4  10  50  50  MHCPEN W=540U  L=2.4U AD=1500P AS=1500P PD=10U PS=540U
MN6 4  11  60  60  MHCNEN W=233U  L=2.4U AD= 750P AS= 750P PD=10U PS=233U
R5 10  12  50
R6 11  13  50
MP7 4  12  50  50  MHCPEN W=540U  L=2.4U AD=1500P AS=1500P PD=10U PS=540U
MN7 4  13  60  60  MHCNEN W=233U  L=2.4U AD= 750P AS= 750P PD=10U PS=233U
.ENDS
```

```
.SUBCKT OUTPN 2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2 4 100
MP1 3 4 50 50  MHCPEN W=360U L=2.4U AD=400P AS=400P PD=10U PS=180U
MN1 3 4 60 60  MHCNEN W=140U L=2.4U AD=200P AS=300P PD=10U PS=130U
R2  4 5 50
MP2 3 5 50 50  MHCPEN W=360U L=2.4U AD=400P AS=400P PD=10U PS=180U
MN2 3 5 60 60  MHCNEN W=140U L=2.4U AD=200P AS=200P PD=10U PS=130U
R3  5 6 50
MP3 3 6 50 50  MHCPEN W=360U L=2.4U AD=400P AS=400P PD=10U PS=180U
MN3 3 6 60 60  MHCNEN W=140U L=2.4U AD=200P AS=200P PD=10U PS=130U
.ENDS

*********************************************************************
*********************************************************************

******CIR_NOMIN-HC TYPES******

.SUBCKT INV0  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP0N
XOUTP 25  30  50  60    OUTPN
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  30   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT INV1  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP1N
XINV  25  35  50  60    INVN
XOUTP 35  40  50  60    OUTPN
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  40   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT INV2  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP2N
XINV  25  35  50  60    INVN
XOUTP 35  40  50  60    OUTPN
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  40   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS
```

```
.SUBCKT INVSMT  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    SMT1N
XINV  25  30  50  60    INVN
XOUTP 30  40  50  60    OUTPN
L1  80  50   3.54NH
L2  60  90   3.54NH
L3   2  20   3.54NH
L4  40   3   3.54NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT NINV1  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP1N
XINV0 25  30  50  60    INVN
XINV1 30  35  50  60    INVN
XOUTP 35  40  50  60    OUTPN
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  40   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT NANDINV 2  5  3  80  90
*INVERTING 2-NAND
*EN = 5, IN = 2, OUT = 3, VCC = 80, GND = 90
XIN1  20  25      50  60   INP2N
XIN2  30  35      50  60   INP2N
XNAND 25  35  36  50  60   NANDN
XOUT  36  40      50  60   OUTPN
L1     2  20   4.28NH
L2     5  30   4.28NH
L3    40   3   6.08NH
L4    80  50   6.08NH
L5    60  90   6.08NH
C1    20  90   1.5P
C2    30  90   1.5P
C3    40  90   1.5P
C4    50  90   1.5P
C5    60  90   1.5P
.ENDS
```

```
.SUBCKT SWI1  2  3  4  70  80  90
* INP = 2  Y = 3  Z = 4  VEE = 70  VCC = 80  GND = 90
XINP 20  25  50  60      INP2N
XLC  25  30  40  50  60  LLCN
XAS  30   3   4  40  50  SWITCH1N
L1   80  50   6.08NH
L2   70  40   6.08NH
L3   60  90   6.08NH
L4    2  20   4.28NH
C1   50  90   1.5P
C2   40  90   1.5P
C3   60  90   1.5P
C4   20  90   1.5P
C5   3   90   1.5P
C6   4   90   1.5P
.ENDS

.SUBCKT SWI2  2  3  4  80  90
* INP = 2  Y = 3  Z = 4  VCC = 80  GND = 90
XINP  20  25  50  60      INP2N
XAS   25   8   9  50  60  SWITCH2N
L1   80  50   3.53NH
L2   60  90   3.54NH
L3    2  20   3.53NH
L4    8   3   3.54NH
L5    9   4   3.54NH
C1   50  90   1.5P
C2   60  90   1.5P
C3   20  90   1.5P
C4   3   90   1.5P
C5   4   90   1.5P
.ENDS

.SUBCKT SWI3  2  3  4  70  80  90
* INP = 2  Y = 3  Z = 4  VEE = 70  VCC = 80  GND = 90
XINP 20  25  50  60      INP1N
XLC  25  30  40  50  60  LLCN
XAS  30   3   4  40  50  SWITCH3N
L1   80  50   5.97NH
L2   70  40   5.97NH
L3   60  90   5.97NH
L4    2  20   4.28NH
C1   50  90   1.5P
C2   40  90   1.5P
C3   60  90   1.5P
C4   20  90   1.5P
C5   3   90   1.5P
C6   4   90   1.5P
.ENDS
```

```
.SUBCKT NINV3  2  5  3  80  90
* INP = 2  OEN = 5(LOW)  OUT = 3   VCC = 80  GND = 90
XINP       20  25  50  60       INP2N
XINV       25  30  50  60       INVN
XBUSOUTP   30  15  35  50  60   BUSOUTPN
L1   80  50    6.87NH
L2   60  90    6.87NH
L3    2  20    6.87NH
L4    5  15    5.97NH
L5   35   3    5.97NH
C1   50  90    1.5P
C2   60  90    1.5P
C4   20  90    1.5P
C5   15  90    1.5P
C6    3  90    1.5P
.ENDS

******CIR_NOMIN-HCT TYPES******

.SUBCKT INV0T  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60     INP0N
XOUTP 25  30  50  60     OUTPN
L1   80  50    6.87NH
L2   60  90    6.87NH
L3    2  20    5.97NH
L4   30   3    5.97NH
C1   50  90    1.5P
C2   60  90    1.5P
C3   20  90    1.5P
C4   3   90    1.5P
.ENDS

.SUBCKT INV1T  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60     INP1TN
XINV  25  35  50  60     INVN
XOUTP 35  40  50  60     OUTPN
L1   80  50    6.87NH
L2   60  90    6.87NH
L3    2  20    5.97NH
L4   40   3    5.97NH
C1   50  90    1.5P
C2   60  90    1.5P
C3   20  90    1.5P
C4   3   90    1.5P
.ENDS

.SUBCKT INV2T  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60     INP2TN
XINV  25  35  50  60     INVN
XOUTP 35  40  50  60     OUTPN
L1   80  50    6.87NH
L2   60  90    6.87NH
L3    2  20    5.97NH
L4   40   3    5.97NH
C1   50  90    1.5P
C2   60  90    1.5P
C3   20  90    1.5P
C4   3   90    1.5P
.ENDS
```

```
.SUBCKT INVSMTT  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    SMTTL1N
XINV  25  35  50  60    INVN
XOUTP 35  40  50  60    OUTPN
L1  80  50   3.54NH
L2  60  90   3.54NH
L3   2  20   3.54NH
L4  40   3   3.54NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT NINV1T  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP1TN
XINV0 25  30  50  60    INVN
XINV1 30  35  50  60    INVN
XOUTP 35  40  50  60    OUTPN
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  40   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT NANDINVT 2  5  3  80  90
*INVERTING 2-NAND
*EN = 5, IN = 2, OUT = 3, VCC = 80, GND = 90
XIN1  20  25      50  60   INP2TN
XIN2  30  35      50  60   INP2TN
XNAND 25  35  36  50  60   NANDN
XOUT  36  40      50  60   OUTPN
L1     2  20   5.29NH
L2     5  30   4.28NH
L3    40   3   3.78NH
L4    80  50   6.08NH
L5    60  90   6.08NH
C1    20  90   1.5P
C2    30  90   1.5P
C3    40  90   1.5P
C4    50  90   1.5P
C5    60  90   1.5P
.ENDS
```

```
.SUBCKT SWI1T  2  3  4  70  80  90
* INP = 2  Y = 3  Z = 4  VEE = 70  VCC = 80  GND = 90
XINP 20  25  50  60      INP2TN
XLC  25  30  40  50  60  LLCN
XAS  30   3   4  40  50  SWITCH1N
L1  80  50   6.08NH
L2  70  40   6.08NH
L3  60  90   6.08NH
L4   2  20   4.28NH
C1  50  90   1.5P
C2  40  90   1.5P
C3  60  90   1.5P
C4  20  90   1.5P
C5  3   90   1.5P
C6  4   90   1.5P
.ENDS

.SUBCKT SWI2T  2  3  4  80  90
* INP = 2  Y = 3  Z = 4  VCC = 80  GND = 90
XINP  20  25  50  60      INP1TN
XAS   25   8   9  50  60  SWITCH2N
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4   8   3   5.97NH
L5   9   4   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
C5  4   90   1.5P
.ENDS

.SUBCKT SWI3T  2  3  4  70  80  90
* INP = 2  Y = 3  Z = 4  VEE = 70  VCC = 80  GND = 90
XINP 20  25  50  60      INP1TN
XLC  25  30  40  50  60  LLCN
XAS  30   3   4  40  50  SWITCH3N
L1  80  50   6.08NH
L2  70  40   6.08NH
L3  60  90   6.08NH
L4   2  20   4.28NH
C1  50  90   1.5P
C2  40  90   1.5P
C3  60  90   1.5P
C4  20  90   1.5P
C5  3   90   1.5P
C6  4   90   1.5P
.ENDS
```

```
.SUBCKT NINV3T  2  5  3  80  90
*
* INP = 2  OEN = 5(LOW)  OUT = 3   VCC = 80  GND = 90
XINP       20  25  50  60       INP2TN
XINV       25  30  50  60       INVN
XBUSOUTP   30  15  35  50  60   BUSOUTPN
L1   80  50    6.87NH
L2   60  90    6.87NH
L3    2  20    6.87NH
L4    5  15    5.97NH
L5   35   3    5.97NH
C1   50  90    1.5P
C2   60  90    1.5P
C4   20  90    1.5P
C5   15  90    1.5P
C6    3  90    1.5P
.ENDS

************************************************************
```

HC_TFAST.CIR Subcircuit

```
* HCMOS Subcircuit and Primitive Elements Library
* HC_TFAST.CIR
* Fast Process Corner
* Standard Logic Product Group
* Philips Semiconductors
* 3/28/95
************************************************
*            FAST N-Channel Transistor         *
*             UCB-3 Parameter Set              *
*          HIGH-SPEED CMOS Logic Family        *
*                10-Jan.-1995                  *
************************************************
.Model MHCNEF NMOS
+LEVEL = 3
+KP    = 49.6E-6
+VTO   = 0.52
+TOX   = 49.0E-9
+NSUB  = 4.0E15
+GAMMA = 0.74
+PHI   = 0.65
+VMAX  = 135E3
+RS    = 30
+RD    = 30
+XJ    = 0.10E-6
+LD    = 0.69E-6
+DELTA = 0.38
+THETA = 0.048
+ETA   = 0.020
+KAPPA = 0.0
+WD    = 0.5E-6

************************************************
*           FAST P-Channel transistor          *
*            UCB-3 Parameter Set               *
*          HIGH-SPEED CMOS Logic Family        *
*                10-Jan.-1995                  *
************************************************
.Model MHCPEF PMOS
+LEVEL = 3
+KP    = 24.6E-6
+VTO   = -0.51
+TOX   = 49.0E-9
+NSUB  = 3.6E16
+GAMMA = 0.82
+PHI   = 0.65
+VMAX  = 600E3
+RS    = 60
+RD    = 60
+XJ    = 0.61E-6
+LD    = 0.35E-6
+DELTA = 2.12
+THETA = 0.100
+ETA   = 0.260
+KAPPA = 0.0
+WD    = 0.5E-6

.MODEL  INT  D
```

```
****************************************
*   START OF SUB-CIRCUIT DESCRIPTION   *
*             MARCH 28, 1995           *
****************************************

*****FAST.CIR*****

.SUBCKT INP0F  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2  3  100
MP1 3 50 50 50  MHCPEF W=20U L=2.4U AD=100P AS=100P PD=40U PS= 20U
MN1 3 60 60 60  MHCNEF W=35U L=2.4U AD=260P AS=260P PD=70U PS= 20U
.ENDS

.SUBCKT INP1F  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MHCPEF W=20U L=2.4U AD=100P AS=100P PD=40U PS= 20U
MN1 4 60 60 60  MHCNEF W=35U L=2.4U AD=260P AS=260P PD=70U PS= 20U
MP2 3  4 50 50  MHCPEF W=88U L=2.4U AD=290P AS=550P PD=10U PS=100U
MN2 3  4 60 60  MHCNEF W=56U L=2.4U AD=162P AS=550P PD=10U PS= 75U
.ENDS

.SUBCKT INP1TF  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MHCPEF W= 20U L=2.4U AD=100P AS=100P PD=40U PS= 20U
MN1 4 60 60 60  MHCNEF W= 35U L=2.4U AD=260P AS=260P PD=70U PS= 20U
MP2 3  4  5 50  MHCPEF W= 88U L=2.4U AD=290P AS=290P PD=10U PS=100U
MN2 3  4 60 60  MHCNEF W= 56U L=2.4U AD=162P AS=290P PD=10U PS= 75U
D1 50  5  INT
MP4 3  6 50 50  MHCPEF W=6.4U L=4.0U AD= 60P AS= 60P PD=13U PS= 24U
MN4 3  4 60 60  MHCNEF W=185U L=2.4U AD=740P AS=740P PD=50U PS=185U
MP5 6  3 50 50  MHCPEF W=6.4U L=3.2U AD= 50P AS= 50P PD=10U PS= 20U
MN5 6  3 60 60  MHCNEF W=6.4U L=3.2U AD= 50P AS= 50P PD=10U PS= 20U
.ENDS

.SUBCKT INP2F  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MHCPEF W= 20U L=2.4U AD=100P AS= 100P PD=40U PS= 20U
MN1 4 60 60 60  MHCNEF W= 35U L=2.4U AD=260P AS= 260P PD=70U PS= 20U
MP2 3  4 50 50  MHCPEF W=176U L=2.4U AD=580P AS= 580P PD=10U PS=200U
MN2 3  4 60 60  MHCNEF W=112U L=2.4U AD=325P AS= 580P PD=10U PS=150U
.ENDS

.SUBCKT INP2TF  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MHCPEF W= 20U L=2.4U AD=100P AS= 100P PD=40U PS= 20U
MN1 4 60 60 60  MHCNEF W= 35U L=2.4U AD=260P AS= 260P PD=70U PS= 20U
MP2 3  4  5 50  MHCPEF W=176U L=2.4U AD=580P AS=1100P PD=10U PS=200U
MN2 3  4 60 60  MHCNEF W=112U L=2.4U AD=325P AS=1100P PD=10U PS=150U
D1 50  5   INT
MP4 3  6 50 50  MHCPEF W=6.4U L=4.0U AD= 60P AS= 60P PD=13U PS= 24U
MN4 3  4 60 60  MHCNEF W=348U L=2.4U AD=740P AS=740P PD=50U PS=348U
MP5 6  3 50 50  MHCPEF W=6.4U L=3.2U AD= 50P AS= 50P PD=10U PS= 20U
MN5 6  3 60 60  MHCNEF W=6.4U L=3.2U AD= 50P AS= 50P PD=10U PS= 20U
.ENDS
```

```
.SUBCKT SMT1F  2  3  50  60
* SCHMITT-TRIGGER INPUT FOR HC14 CMOS INPUT LEVELS
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MHCPEF W=20U L=2.4U AD=100P AS=100P PD=40U PS=20U
MN1 4 60 60 60  MHCNEF W=35U L=2.4U AD=140P AS=140P PD=50U PS=35U
MP2 5  4 50 50  MHCPEF W=36U L=2.4U AD=140P AS=140P PD=50U PS=35U
MN2 6  4 60 60  MHCNEF W=16U L=2.4U AD= 70P AS= 70P PD=15U PS=17U
MP3 3  4  5 50  MHCPEF W=44U L=2.4U AD=220P AS=220P PD=60U PS=44U
MN3 3  4  6  6  MHCNEF W=17U L=2.4U AD= 70P AS= 70P PD=15U PS=16U
MP4 5  3 60 50  MHCPEF W=36U L=2.4U AD=150P AS=150P PD=60U PS=36U
MN4 6  3 50  6  MHCNEF W= 6U L=4.0U AD= 25P AS= 25P PD=10U PS= 6U
.ENDS

.SUBCKT SMTTL1F  2  3  50  60
* SCHMITT-TRIGGER INPUT FOR HCT14 WITH TTL INPUT LEVELS
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MHCPEF W= 20U L=2.4U AD= 100P AS= 100P PD= 40U PS= 20U
MN1 4 60 60 60  MHCNEF W= 35U L=2.4U AD= 140P AS= 140P PD= 50U PS= 35U
D1  50  7  INT
MP2 5  4  7  7  MHCPEF W= 36U L=2.4U AD= 140P AS= 140P PD= 50U PS= 35U
MN2 6  4 60 60  MHCNEF W=216U L=2.4U AD= 860P AS= 860P PD=140U PS=216U
MP3 3  4  5 50  MHCPEF W= 54U L=2.4U AD= 220P AS= 220P PD= 60U PS= 44U
MN3 3  4  6  6  MHCNEF W=257U L=2.4U AD=1000P AS=1000P PD=150U PS=257U
MP4 5  3 60 50  MHCPEF W= 32U L=4.0U AD= 120P AS= 120P PD=100U PS= 32U
MN4 6  3 50  6  MHCNEF W= 14U L=4.0U AD= 100P AS= 100P PD= 30U PS= 24U
MP5 8  3 50 50  MHCPEF W= 10U L=2.4U AD=  40P AS=  40P PD= 16U PS= 10U
MN5 8  3 60 60  MHCNEF W=  5U L=2.4U AD=  20P AS=  20P PD= 12U PS=  5U
MP6 3  8 50 50  MHCPEF W=  6U L=8.0U AD=  30P AS=  30P PD= 16U PS=  6U
.ENDS

.SUBCKT INVF   2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
MP1 3  2 50 50  MHCPEF W=364U L=2.4U AD=500P  AS=500P PD=10U PS=430U
MN1 3  2 60 60  MHCNEF W=184U L=2.4U AD=275P  AS=275P PD=10U PS=270U
.ENDS

.SUBCKT NANDF  2  3  4  50  60
*INTERNAL NAND
*IN1 = 2, IN2 = 3, OUT = 4, VCC= 50, GND = 60
MP1 4  2  50  50  MHCPEF W=112U  L=2.4U AD=150P AS=300P PD= 75U PS=150U
MP2 4  3  50  50  MHCPEF W=112U  L=2.4U AD=150P AS=300P PD= 75U PS=150U
MN1 4  2   5  60  MHCNEF W=300U  L=2.4U AD=300P AS=300P PD=300U PS=300U
MN2 5  3  60  60  MHCNEF W=300U  L=2.4U AD=300P AS=300P PD=300U PS=300U
.ENDS

.SUBCKT LLCF  2  3  40  50  60
* LEVEL CONVERTER
* INA = 2,  INB = 3,   VEE = 40,  VCC = 50,  GND = 60
MP4 4  2  50  50  MHCPEF W= 30U  L= 2.4U AD=120P AS=120P PD= 40U PS= 30U
MN4 4  2  60  60  MHCNEF W= 15U  L= 2.4U AD= 60P AS= 60P PD= 20U PS= 15U
MP1 5  2  50  50  MHCPEF W=135U  L= 2.4U AD=500P AS=500P PD=100U PS=135U
MP2 6  2  50  50  MHCPEF W=135U  L= 2.4U AD=500P AS=500P PD=100U PS=135U
MN1 5  6  40  40  MHCNEF W=6.4U  L=18.8U AD= 25P AS= 25P PD= 20U PS=6.4U
MN2 6  5  40  40  MHCNEF W=6.4U  L=18.8U AD= 25P AS= 25P PD= 20U PS=6.4U
MP3 7  6  50  50  MHCPEF W= 10U  L= 4.0U AD= 40P AS= 40P PD= 20U PS= 10U
MN3 7  6  40  40  MHCNEF W=  5U  L= 4.0U AD= 20P AS= 20P PD= 10U PS=  5U
MP5 3  7  50  50  MHCPEF W= 30U  L= 2.4U AD=120P AS=120P PD= 40U PS= 30U
MN5 3  7  40  40  MHCNEF W= 15U  L= 2.4U AD= 60P AS= 60P PD= 20U PS= 15U
.ENDS
```

```
.SUBCKT SWITCH1F  2  8  9  40  50
* ANALOG SWITCH
* INPUT = 2   Y = 8  Z = 9  VEE = 40  VCC =50
MP1 3  2  50  50  MHCPEF W=  88U L=2.4U AD= 350P AS= 350P PD=100U PS=  88U
MN1 3  2  40  40  MHCNEF W=  56U L=2.4U AD= 225P AS= 225P PD= 70U PS=  56U
MP4 4  3  50  50  MHCPEF W= 350U L=2.4U AD= 900P AS= 900P PD=200U PS= 350U
MN4 4  3  40  40  MHCNEF W= 150U L=2.4U AD= 400P AS= 400P PD=100U PS= 150U
MP5 8  4   5  50  MHCPEF W= 216U L=2.4U AD= 900P AS= 900P PD=100U PS= 216U
MN5 8  3   5   5  MHCNEF W= 108U L=2.4U AD= 430P AS= 430P PD= 50U PS= 108U
MN6 5  4  40  40  MHCNEF W= 145U L=2.4U AD= 600P AS= 600P PD= 75U PS= 145U
MP7 9  4   8  50  MHCPEF W=1068U L=2.4U AD=2500P AS=2500P PD= 10U PS=1068U
MN7 9  3   8   5  MHCNEF W= 312U L=2.4U AD=1200P AS=1200P PD= 10U PS= 312U
.ENDS

.SUBCKT SWITCH2F  2  8  9  50  60
* ANALOG SWITCH
* INPUT= 2   Y= 8   Z= 9  VCC= 50   GND= 60
MP1 3  2  50  50  MHCPEF W=  88U L=2.4U AD= 350P AS= 350P PD=100U PS=  88U
MN1 3  2  60  60  MHCNEF W=  56U L=2.4U AD= 225P AS= 225P PD= 70U PS=  56U
MP4 4  3  50  50  MHCPEF W= 350U L=2.4U AD= 900P AS= 900P PD=200U PS= 350U
MN4 4  3  60  60  MHCNEF W= 150U L=2.4U AD= 400P AS= 400P PD=100U PS= 150U
MP5 5  3   8  50  MHCPEF W=  85U L=2.4U AD= 355P AS= 355P PD= 40U PS=  85U
MN5 5  4   8   5  MHCNEF W=  42U L=2.4U AD= 170P AS= 170P PD= 20U PS=  42U
MN6 5  3  60  60  MHCNEF W= 145U L=2.4U AD= 600P AS= 600P PD= 75U PS= 145U
MP7 9  3   8  50  MHCPEF W=1900U L=2.4U AD=2500P AS=2500P PD= 10U PS=1900U
MN7 9  4   8   5  MHCNEF W= 576U L=2.4U AD=1200P AS=1200P PD= 10U PS= 576U
.ENDS

.SUBCKT SWITCH3F  2  8  9  40  50
* ANALOG SWITCH
* INPUT = 2   Y = 8  Z = 9  VEE = 40  VCC = 50
MP1 3  2  50  50  MHCPEF W=  88U L=2.4U AD= 350P AS= 350P PD=100U PS=  88U
MN1 3  2  40  40  MHCNEF W=  56U L=2.4U AD= 225P AS= 225P PD= 70U PS=  56U
MP4 4  3  50  50  MHCPEF W= 350U L=2.4U AD= 900P AS= 900P PD=200U PS= 350U
MN4 4  3  40  40  MHCNEF W= 150U L=2.4U AD= 400P AS= 400P PD=100U PS= 150U
MP5 9  3   8  50  MHCPEF W=1168U L=2.4U AD=2730P AS=2730P PD= 10U PS=1168U
MN5 9  4   8  40  MHCNEF W= 312U L=2.4U AD=1200P AS=1200P PD= 10U PS= 312U
.ENDS
```

```
.SUBCKT BUSOUTPF  2   3   4   50   60
* INPUT = 2  OEN = 3 (LOW)  OUT = 4  VCC = 50  GND = 60
* 3-STATE BUS OUTPUT
MP1 5  3   50  50  MHCPEF W= 90U  L=2.4U AD= 360P AS= 360P PD= 30U PS=360U
MN1 5  3   60  60  MHCNEF W= 40U  L=2.4U AD= 160P AS= 160P PD= 20U PS= 40U
MP2 6  2   50  50  MHCPEF W=480U  L=2.4U AD=1800P AS=1800P PD=100U PS=480U
MN2 7  2   60  60  MHCNEF W=240U  L=2.4U AD=1000P AS=1000P PD= 50U PS=240U
MP3 7  3    6  50  MHCPEF W=280U  L=2.4U AD=1120P AS=1120P PD= 55U PS=280U
MN3 7  3   60  60  MHCNEF W=160U  L=2.4U AD= 640P AS= 640P PD= 40U PS=160U
MP4 6  5   50  50  MHCPEF W=240U  L=2.4U AD=1000P AS=1000P PD= 50U PS=240U
MN4 7  5    7  60  MHCNEF W=190U  L=2.4U AD= 760P AS= 760P PD= 45U PS=190U
R1  6  8  200
R2  7  9  200
MP5 4  8   50  50  MHCPEF W=540U  L=2.4U AD=1500P AS=1500P PD=10U PS=540U
MN5 4  9   60  60  MHCNEF W=233U  L=2.4U AD= 750P AS= 750P PD=10U PS=233U
R3  8  10 100
R4  9  11 100
MP6 4  10  50  50  MHCPEF W=540U  L=2.4U AD=1500P AS=1500P PD=10U PS=540U
MN6 4  11  60  60  MHCNEF W=233U  L=2.4U AD= 750P AS= 750P PD=10U PS=233U
R5 10  12  50
R6 11  13  50
MP7 4  12  50  50  MHCPEF W=540U  L=2.4U AD=1500P AS=1500P PD=10U PS=540U
MN7 4  13  60  60  MHCNEF W=233U  L=2.4U AD= 750P AS= 750P PD=10U PS=233U
.ENDS

.SUBCKT OUTPF 2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2 4 100
MP1 3 4 50 50  MHCPEF W=360U L=2.4U AD=400P AS=400P PD=10U PS=180U
MN1 3 4 60 60  MHCNEF W=140U L=2.4U AD=200P AS=300P PD=10U PS=130U
R2  4 5 50
MP2 3 5 50 50  MHCPEF W=360U L=2.4U AD=400P AS=400P PD=10U PS=180U
MN2 3 5 60 60  MHCNEF W=140U L=2.4U AD=200P AS=200P PD=10U PS=130U
R3  5 6 50
MP3 3 6 50 50  MHCPEF W=360U L=2.4U AD=400P AS=400P PD=10U PS=180U
MN3 3 6 60 60  MHCNEF W=140U L=2.4U AD=200P AS=200P PD=10U PS=130U
.ENDS

*********************************************************************
*********************************************************************
```

```
******CIR_FAST_HC TYPES******

.SUBCKT INV0  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP0F
XOUTP 25  30  50  60    OUTPF
L1   80  50   6.87NH
L2   60  90   6.87NH
L3    2  20   5.97NH
L4   30   3   5.97NH
C1   50  90   1.5P
C2   60  90   1.5P
C3   20  90   1.5P
C4   3   90   1.5P
.ENDS

.SUBCKT INV1  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP1F
XINV  25  35  50  60    INVF
XOUTP 35  40  50  60    OUTPF
L1   80  50   6.87NH
L2   60  90   6.87NH
L3    2  20   5.97NH
L4   40   3   5.97NH
C1   50  90   1.5P
C2   60  90   1.5P
C3   20  90   1.5P
C4   3   90   1.5P
.ENDS

.SUBCKT INV2  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP2F
XINV  25  35  50  60    INVF
XOUTP 35  40  50  60    OUTPF
L1   80  50   6.87NH
L2   60  90   6.87NH
L3    2  20   5.97NH
L4   40   3   5.97NH
C1   50  90   1.5P
C2   60  90   1.5P
C3   20  90   1.5P
C4   3   90   1.5P
.ENDS

.SUBCKT INVSMT  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    SMT1F
XINV  25  30  50  60    INVF
XOUTP 30  40  50  60    OUTPF
L1   80  50   3.54NH
L2   60  90   3.54NH
L3    2  20   3.54NH
L4   40   3   3.54NH
C1   50  90   1.5P
C2   60  90   1.5P
C3   20  90   1.5P
C4   3   90   1.5P
.ENDS
```

```
.SUBCKT NINV1  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP1F
XINV0 25  30  50  60    INVF
XINV1 30  35  50  60    INVF
XOUTP 35  40  50  60    OUTPF
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  40   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT NANDINV 2  5  3  80  90
*INVERTING 2-NAND
*EN = 5, IN = 2, OUT = 3, VCC = 80, GND = 90
XIN1  20  25      50  60   INP2F
XIN2  30  35      50  60   INP2F
XNAND 25  35  36  50  60   NANDF
XOUT  36  40      50  60   OUTPF
L1     2  20   4.28NH
L2     5  30   4.28NH
L3    40   3   6.08NH
L4    80  50   6.08NH
L5    60  90   6.08NH
C1    20  90   1.5P
C2    30  90   1.5P
C3    40  90   1.5P
C4    50  90   1.5P
C5    60  90   1.5P
.ENDS

.SUBCKT SWI1  2  3  4  70  80  90
* INP = 2  Y = 3  Z = 4  VEE = 70  VCC = 80  GND = 90
XINP 20  25  50  60      INP2F
XLC  25  30  40  50  60  LLCF
XAS  30   3   4  40  50  SWITCH1F
L1  80  50   6.08NH
L2  70  40   6.08NH
L3  60  90   6.08NH
L4   2  20   4.28NH
C1  50  90   1.5P
C2  40  90   1.5P
C3  60  90   1.5P
C4  20  90   1.5P
C5  3   90   1.5P
C6  4   90   1.5P
.ENDS
```

```
.SUBCKT SWI2  2  3  4  80  90
* INP = 2  Y = 3  Z = 4  VCC = 80  GND = 90
XINP  20  25  50  60      INP2F
XAS   25   8   9  50  60  SWITCH2F
L1  80  50   3.53NH
L2  60  90   3.54NH
L3   2  20   3.53NH
L4   8   3   3.54NH
L5   9   4   3.54NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
C5  4   90   1.5P
.ENDS

.SUBCKT SWI3  2  3  4  70  80  90
* INP = 2  Y = 3  Z = 4  VEE = 70  VCC = 80  GND = 90
XINP 20  25  50  60      INP1F
XLC  25  30  40  50  60  LLCF
XAS  30   3   4  40  50  SWITCH3F
L1  80  50   5.97NH
L2  70  40   5.97NH
L3  60  90   5.97NH
L4   2  20   4.28NH
C1  50  90   1.5P
C2  40  90   1.5P
C3  60  90   1.5P
C4  20  90   1.5P
C5  3   90   1.5P
C6  4   90   1.5P
.ENDS

.SUBCKT NINV3  2  5  3  80  90
* INP = 2  OEN = 5(LOW)  OUT = 3  VCC = 80  GND = 90
XINP      20  25  50  60      INP2F
XINV      25  30  50  60      INVF
XBUSOUTP  30  15  35  50  60  BUSOUTPF
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   6.87NH
L4   5  15   5.97NH
L5  35   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C4  20  90   1.5P
C5  15  90   1.5P
C6   3  90   1.5P
.ENDS
```

```
******CIR_FAST_HCT TYPES******

.SUBCKT INV0T  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP0F
XOUTP 25  30  50  60    OUTPF
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  30   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT INV1T  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP1TF
XINV  25  35  50  60    INVF
XOUTP 35  40  50  60    OUTPF
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  40   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT INV2T  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP2TF
XINV  25  35  50  60    INVF
XOUTP 35  40  50  60    OUTPF
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  40   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT INVSMTT  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    SMTTL1F
XINV  25  35  50  60    INVF
XOUTP 35  40  50  60    OUTPF
L1  80  50   3.54NH
L2  60  90   3.54NH
L3   2  20   3.54NH
L4  40   3   3.54NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS
```

```
.SUBCKT NINV1T  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP1TF
XINV0 25  30  50  60    INVF
XINV1 30  35  50  60    INVF
XOUTP 35  40  50  60    OUTPF
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  40   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT NANDINVT 2  5  3  80  90
*INVERTING 2-NAND
*EN = 5, IN = 2, OUT = 3, VCC = 80, GND = 90
XIN1  20  25      50  60   INP2TF
XIN2  30  35      50  60   INP2TF
XNAND 25  35  36  50  60   NANDF
XOUT  36  40      50  60   OUTPF
L1     2  20   5.29NH
L2     5  30   4.28NH
L3    40   3   3.78NH
L4    80  50   6.08NH
L5    60  90   6.08NH
C1    20  90   1.5P
C2    30  90   1.5P
C3    40  90   1.5P
C4    50  90   1.5P
C5    60  90   1.5P
.ENDS

.SUBCKT SWI1T  2  3  4  70  80  90
* INP = 2  Y = 3  Z = 4  VEE = 70  VCC = 80  GND = 90
XINP 20  25  50  60      INP2TF
XLC  25  30  40  50  60  LLCF
XAS  30   3   4  40  50  SWITCH1F
L1  80  50   6.08NH
L2  70  40   6.08NH
L3  60  90   6.08NH
L4   2  20   4.28NH
C1  50  90   1.5P
C2  40  90   1.5P
C3  60  90   1.5P
C4  20  90   1.5P
C5  3   90   1.5P
C6  4   90   1.5P
.ENDS
```

```
.SUBCKT SWI2T  2  3  4  80  90
* INP = 2  Y = 3  Z = 4  VCC = 80  GND = 90
XINP  20  25  50  60      INP1TF
XAS   25   8   9  50  60  SWITCH2F
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4   8   3   5.97NH
L5   9   4   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
C5  4   90   1.5P
.ENDS

.SUBCKT SWI3T  2  3  4  70  80  90
* INP = 2  Y = 3  Z = 4  VEE = 70  VCC = 80  GND = 90
XINP 20  25  50  60      INP1TF
XLC  25  30  40  50  60  LLCF
XAS  30   3   4  40  50  SWITCH3F
L1  80  50   6.08NH
L2  70  40   6.08NH
L3  60  90   6.08NH
L4   2  20   4.28NH
C1  50  90   1.5P
C2  40  90   1.5P
C3  60  90   1.5P
C4  20  90   1.5P
C5  3   90   1.5P
C6  4   90   1.5P
.ENDS

.SUBCKT NINV3T  2  5  3  80  90
*
* INP = 2  OEN = 5(LOW)  OUT = 3   VCC = 80  GND = 90
XINP      20  25  50  60      INP2TF
XINV      25  30  50  60      INVF
XBUSOUTP  30  15  35  50  60  BUSOUTPF
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   6.87NH
L4   5  15   5.97NH
L5  35   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C4  20  90   1.5P
C5  15  90   1.5P
C6   3  90   1.5P
.ENDS

************************************************************
```

HC_TSLOW.CIR Subcircuit

```
* HCMOS Subcircuit and Primitive Elements Library
* HC_TSLOW.CIR
* Slow Process Corner
* Standard Logic Product Group
* Philips Semiconductors
* 3/28/95
************************************************
*          SLOW N-Channel Transistor           *
*            UCB-3 Parameter Set               *
*         HIGH-SPEED CMOS Logic Family         *
*                10-Jan.-1995                  *
************************************************
.Model MHCNES NMOS
+LEVEL = 3
+KP    = 41.0E-6
+VTO   = 0.92
+TOX   = 54.0E-9
+NSUB  = 2.0E15
+GAMMA = 1.14
+PHI   = 0.65
+VMAX  = 175E3
+RS    = 50
+RD    = 50
+XJ    = 0.12E-6
+LD    = 0.35E-6
+DELTA = 0.25
+THETA = 0.060
+ETA   = 0.030
+KAPPA = 0.0
+WD    = -0.5E-6

************************************************
*          SLOW P-Channel transistor           *
*           UCB-3 Parameter Set                *
*         HIGH-SPEED CMOS Logic Family         *
*                10-Jan.-1995                  *
************************************************
.Model MHCPES PMOS
+LEVEL = 3
+KP    = 19.6E-6
+VTO   = -0.91
+TOX   = 54.0E-9
+NSUB  = 3.0E16
+GAMMA = 1.02
+PHI   = 0.65
+VMAX  = 190E4
+RS    = 100
+RD    = 100
+XJ    = 0.65E-6
+LD    = 0.10E-6
+DELTA = 2.35
+THETA = 0.120
+ETA   = 0.380
+KAPPA = 0.0
+WD    = -0.5E-6

.MODEL  INT D
```

```
****************************************
*   START OF SUB-CIRCUIT DESCRIPTION   *
*            MARCH 28, 1995            *
****************************************

*****SLOW.CIR*****

.SUBCKT INP0S  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2  3  100
MP1 3 50 50 50  MHCPES W=20U L=2.4U AD=100P AS=100P PD=40U PS= 20U
MN1 3 60 60 60  MHCNES W=35U L=2.4U AD=260P AS=260P PD=70U PS= 20U
.ENDS

.SUBCKT INP1S  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MHCPES W=20U L=2.4U AD=100P AS=100P PD=40U PS= 20U
MN1 4 60 60 60  MHCNES W=35U L=2.4U AD=260P AS=260P PD=70U PS= 20U
MP2 3  4 50 50  MHCPES W=88U L=2.4U AD=290P AS=550P PD=10U PS=100U
MN2 3  4 60 60  MHCNES W=56U L=2.4U AD=162P AS=550P PD=10U PS= 75U
.ENDS

.SUBCKT INP1TS  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MHCPES W= 20U L=2.4U AD=100P AS=100P PD= 40U PS= 20U
MN1 4 60 60 60  MHCNES W= 35U L=2.4U AD=260P AS=260P PD= 70U PS= 20U
MP2 3  4  5 50  MHCPES W= 88U L=2.4U AD=290P AS=550P PD=107U PS=195U
MN2 3  4 60 60  MHCNES W= 56U L=2.4U AD=162P AS=550P PD= 55U PS=162U
D1 50  5  INT
MP4 3  6 50 50  MHCPES W=6.4U L=4.0U AD= 60P AS= 60P PD= 13U PS= 24U
MN4 3  4 60 60  MHCNES W=185U L=2.4U AD=740P AS=740P PD= 50U PS=185U
MP5 6  3 50 50  MHCPES W=6.4U L=3.2U AD= 50P AS= 50P PD= 10U PS= 20U
MN5 6  3 60 60  MHCNES W=6.4U L=3.2U AD= 50P AS= 50P PD= 10U PS= 20U
.ENDS

.SUBCKT INP2S  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MHCPES W= 20U L=2.4U AD= 100P AS=100P PD= 40U PS= 20U
MN1 4 60 60 60  MHCNES W= 35U L=2.4U AD= 260P AS=260P PD= 70U PS= 20U
MP2 3  4 50 50  MHCPES W=176U L=2.4U AD= 580P AS=580P PD=10U PS=200U
MN2 3  4 60 60  MHCNES W=112U L=2.4U AD= 325P AS=580P PD=10U PS=150U
.ENDS

.SUBCKT INP2TS  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MHCPES W= 20U L=2.4U AD= 100P AS= 100P PD= 40U PS= 20U
MN1 4 60 60 60  MHCNES W= 35U L=2.4U AD= 260P AS= 260P PD= 70U PS= 20U
MP2 3  4  5 50  MHCPES W=176U L=2.4U AD= 580P AS=1100P PD=215U PS=390U
MN2 3  4 60 60  MHCNES W=440U L=2.4U AD=1320P AS=1840P PD=190U PS=650U
D1 50  5   INT
MP4 3  6 50 50  MHCPES W=6.4U L=4.0U AD=  60P AS=  60P PD= 13U PS= 24U
MP5 6  3 50 50  MHCPES W=6.4U L=3.2U AD=  50P AS=  50P PD= 10U PS= 20U
MN5 6  3 60 60  MHCNES W=6.4U L=3.2U AD=  50P AS=  50P PD= 10U PS= 20U
.ENDS
```

```
.SUBCKT SMT1S  2  3  50  60
* SCHMITT-TRIGGER INPUT FOR HC14 CMOS INPUT LEVELS
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MHCPES W=20U L=2.4U AD=100P AS=100P PD=40U PS=20U
MN1 4 60 60 60  MHCNES W=35U L=2.4U AD=140P AS=140P PD=50U PS=35U
MP2 5  4 50 50  MHCPES W=36U L=2.4U AD=140P AS=140P PD=50U PS=35U
MN2 6  4 60 60  MHCNES W=16U L=2.4U AD= 70P AS= 70P PD=15U PS=17U
MP3 3  4  5 50  MHCPES W=44U L=2.4U AD=220P AS=220P PD=60U PS=44U
MN3 3  4  6  6  MHCNES W=17U L=2.4U AD= 70P AS= 70P PD=15U PS=16U
MP4 5  3 60 50  MHCPES W=36U L=2.4U AD=150P AS=150P PD=60U PS=36U
MN4 6  3 50  6  MHCNES W= 6U L=  4U AD= 25P AS= 25P PD=10U PS= 6U
.ENDS

.SUBCKT SMTTL1S  2  3  50  60
* SCHMITT-TRIGGER INPUT FOR HCT14 WITH TTL INPUT LEVELS
*IN=2, OUT=3, VCC=50, GND=60
R1  2  4  100
MP1 4 50 50 50  MHCPES W= 20U L=2.4U AD= 100P AS= 100P PD= 40U PS= 20U
MN1 4 60 60 60  MHCNES W= 35U L=2.4U AD= 140P AS= 140P PD= 50U PS= 35U
D1  50  7  INT
MP2 5  4  7  7  MHCPES W= 36U L=2.4U AD= 140P AS= 140P PD= 50U PS= 35U
MN2 6  4 60 60  MHCNES W=216U L=2.4U AD= 860P AS= 860P PD=140U PS=216U
MP3 3  4  5 50  MHCPES W= 54U L=2.4U AD= 220P AS= 220P PD= 60U PS= 44U
MN3 3  4  6  6  MHCNES W=257U L=2.4U AD=1000P AS=1000P PD=150U PS=257U
MP4 5  3 60 50  MHCPES W= 32U L=  4U AD= 120P AS= 120P PD=100U PS= 32U
MN4 6  3 50  6  MHCNES W= 14U L=  4U AD= 100P AS= 100P PD= 30U PS= 24U
MP5 8  3 50 50  MHCPES W= 10U L=2.4U AD=  40P AS=  40P PD= 16U PS= 10U
MN5 8  3 60 60  MHCNES W=  5U L=2.4U AD=  20P AS=  20P PD= 12U PS=  5U
MP6 3  8 50 50  MHCPES W=  6U L=8.0U AD=  30P AS=  30P PD= 16U PS=  6U
.ENDS

.SUBCKT INVS   2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
MP1 3  2 50 50  MHCPES W=364U L=2.4U AD=500P  AS=500P PD=10U PS=430U
MN1 3  2 60 60  MHCNES W=184U L=2.4U AD=275P  AS=275P PD=10U PS=270U
.ENDS

.SUBCKT NANDS  2  3  4  50  60
*INTERNAL NAND
*IN1 = 2, IN2 = 3, OUT = 4, VCC= 50, GND = 60
MP1 4  2  50  50  MHCPES W=112U  L=2.4U AD=150P AS=300P PD= 75U PS=150U
MP2 4  3  50  50  MHCPES W=112U  L=2.4U AD=150P AS=300P PD= 75U PS=150U
MN1 4  2   5  60  MHCNES W=300U  L=2.4U AD=300P AS=300P PD=300U PS=300U
MN2 5  3  60  60  MHCNES W=300U  L=2.4U AD=300P AS=300P PD=300U PS=300U
.ENDS

.SUBCKT LLCS  2  3  40  50  60
* LEVEL CONVERTER
* INA = 2,  OUT = 3,  VEE = 40,  VCC = 50,  GND =  60
MP4 4  2  50  50  MHCPES W= 30U  L= 2.4U AD=120P AS=120P PD= 40U PS= 30U
MN4 4  2  60  60  MHCNES W= 15U  L= 2.4U AD= 60P AS= 60P PD= 20U PS= 15U
MP1 5  2  50  50  MHCPES W=135U  L= 2.4U AD=500P AS=500P PD=100U PS=135U
MP2 6  2  50  50  MHCPES W=135U  L= 2.4U AD=500P AS=500P PD=100U PS=135U
MN1 5  6  40  40  MHCNES W=6.4U  L=18.8U AD= 25P AS= 25P PD= 20U PS=6.4U
MN2 6  5  40  40  MHCNES W=6.4U  L=18.8U AD= 25P AS= 25P PD= 20U PS=6.4U
MP3 7  6  50  50  MHCPES W= 10U  L= 4.0U AD= 40P AS= 40P PD= 20U PS= 10U
MN3 7  6  40  40  MHCNES W=  5U  L= 4.0U AD= 20P AS= 20P PD= 10U PS=  5U
MP5 3  7  50  50  MHCPES W= 30U  L= 2.4U AD=120P AS=120P PD= 40U PS= 30U
MN5 3  7  40  40  MHCNES W= 15U  L= 2.4U AD= 60P AS= 60P PD= 20U PS= 15U
.ENDS
```

```
.SUBCKT SWITCH1S  2  8  9  40  50
* ANALOG SWITCH
* INPUT = 2   Y = 8  Z = 9  VEE = 40  VCC =50
MP1 3  2  50  50  MHCPES W=  88U L=2.4U AD= 350P AS= 350P PD=100U PS=  88U
MN1 3  2  40  40  MHCNES W=  56U L=2.4U AD= 225P AS= 225P PD= 70U PS=  56U
MP4 4  3  50  50  MHCPES W= 350U L=2.4U AD= 900P AS= 900P PD=200U PS= 350U
MN4 4  3  40  40  MHCNES W= 150U L=2.4U AD= 400P AS= 400P PD=100U PS= 150U
MP5 8  4   5  50  MHCPES W= 216U L=2.4U AD= 900P AS= 900P PD=100U PS= 216U
MN5 8  3   5   5  MHCNES W= 108U L=2.4U AD= 430P AS= 430P PD= 50U PS= 108U
MN6 5  4  40  40  MHCNES W= 145U L=2.4U AD= 600P AS= 600P PD= 75U PS= 145U
MP7 9  4   8  50  MHCPES W=1068U L=2.4U AD=2500P AS=2500P PD= 10U PS=1068U
MN7 9  3   8   5  MHCNES W= 312U L=2.4U AD=1200P AS=1200P PD= 10U PS= 312U
.ENDS

.SUBCKT SWITCH2S  2  8  9  50  60
* ANALOG SWITCH
* INPUT= 2   Y= 8   Z= 9  VCC= 50   GND= 60
MP1 3  2  50  50  MHCPES W=  88U L=2.4U AD= 350P AS= 350P PD=100U PS=  88U
MN1 3  2  60  60  MHCNES W=  56U L=2.4U AD= 225P AS= 225P PD= 70U PS=  56U
MP4 4  3  50  50  MHCPES W= 350U L=2.4U AD= 900P AS= 900P PD=200U PS= 350U
MN4 4  3  60  60  MHCNES W= 150U L=2.4U AD= 400P AS= 400P PD=100U PS= 150U
MP5 5  3   8  50  MHCPES W=  85U L=2.4U AD= 355P AS= 355P PD= 40U PS=  85U
MN5 5  4   8   5  MHCNES W=  42U L=2.4U AD= 170P AS= 170P PD= 20U PS=  42U
MN6 5  3  60  60  MHCNES W= 145U L=2.4U AD= 600P AS= 600P PD= 75U PS= 145U
MP7 9  3   8  50  MHCPES W=1900U L=2.4U AD=2500P AS=2500P PD= 10U PS=1900U
MN7 9  4   8   5  MHCNES W= 576U L=2.4U AD=1200P AS=1200P PD= 10U PS= 576U
.ENDS

.SUBCKT SWITCH3S  2  8  9  40  50
* ANALOG SWITCH
* INPUT = 2   Y = 8  Z = 9  VEE = 40  VCC = 50
MP1 3  2  50  50  MHCPES W=  88U L=2.4U AD= 350P AS= 350P PD=100U PS=  88U
MN1 3  2  40  40  MHCNES W=  56U L=2.4U AD= 225P AS= 225P PD= 70U PS=  56U
MP4 4  3  50  50  MHCPES W= 350U L=2.4U AD= 900P AS= 900P PD=200U PS= 350U
MN4 4  3  40  40  MHCNES W= 150U L=2.4U AD= 400P AS= 400P PD=100U PS= 150U
MP5 9  3   8  50  MHCPES W=1168U L=2.4U AD=2730P AS=2730P PD= 10U PS=1168U
MN5 9  4   8  40  MHCNES W= 312U L=2.4U AD=1200P AS=1200P PD= 10U PS= 312U
.ENDS
```

```
.SUBCKT BUSOUTPS  2   3   4   50   60
* INPUT = 2  OEN = 3 (LOW)  OUT = 4  VCC = 50  GND = 60
* 3-STATE BUS OUTPUT
MP1 5  3   50  50  MHCPES W= 90U  L=2.4U AD= 360P AS= 360P PD= 30U PS=360U
MN1 5  3   60  60  MHCNES W= 40U  L=2.4U AD= 160P AS= 160P PD= 20U PS= 40U
MP2 6  2   50  50  MHCPES W=480U  L=2.4U AD=1800P AS=1800P PD=100U PS=480U
MN2 7  2   60  60  MHCNES W=240U  L=2.4U AD=1000P AS=1000P PD= 50U PS=240U
MP3 7  3    6  50  MHCPES W=280U  L=2.4U AD=1120P AS=1120P PD= 55U PS=280U
MN3 7  3   60  60  MHCNES W=160U  L=2.4U AD= 640P AS= 640P PD= 40U PS=160U
MP4 6  5   50  50  MHCPES W=240U  L=2.4U AD=1000P AS=1000P PD= 50U PS=240U
MN4 7  5    7  60  MHCNES W=190U  L=2.4U AD= 760P AS= 760P PD= 45U PS=190U
R1  6  8  200
R2  7  9  200
MP5 4  8   50  50  MHCPES W=540U  L=2.4U AD=1500P AS=1500P PD=10U PS=540U
MN5 4  9   60  60  MHCNES W=233U  L=2.4U AD= 750P AS= 750P PD=10U PS=233U
R3  8  10 100
R4  9  11 100
MP6 4  10  50  50  MHCPES W=540U  L=2.4U AD=1500P AS=1500P PD=10U PS=540U
MN6 4  11  60  60  MHCNES W=233U  L=2.4U AD= 750P AS= 750P PD=10U PS=233U
R5 10  12  50
R6 11  13  50
MP7 4  12  50  50  MHCPES W=540U  L=2.4U AD=1500P AS=1500P PD=10U PS=540U
MN7 4  13  60  60  MHCNES W=233U  L=2.4U AD= 750P AS= 750P PD=10U PS=233U
.ENDS

.SUBCKT OUTPS  2  3  50  60
*IN=2, OUT=3, VCC=50, GND=60
R1  2 4 100
MP1 3 4 50 50  MHCPES W=360U L=2.4U AD=400P AS=400P PD=10U PS=180U
MN1 3 4 60 60  MHCNES W=140U L=2.4U AD=200P AS=300P PD=10U PS=130U
R2  4 5 50
MP2 3 5 50 50  MHCPES W=360U L=2.4U AD=400P AS=400P PD=10U PS=180U
MN2 3 5 60 60  MHCNES W=140U L=2.4U AD=200P AS=200P PD=10U PS=130U
R3  5 6 50
MP3 3 6 50 50  MHCPES W=360U L=2.4U AD=400P AS=400P PD=10U PS=180U
MN3 3 6 60 60  MHCNES W=140U L=2.4U AD=200P AS=200P PD=10U PS=130U
.ENDS

********************************************************************************
********************************************************************************
```

```
******CIR_SLOW_HC TYPES******

.SUBCKT INV0  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP0S
XOUTP 25  30  50  60    OUTPS
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  30   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT INV1  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP1S
XINV  25  35  50  60    INVS
XOUTP 35  40  50  60    OUTPS
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  40   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT INV2  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP2S
XINV  25  35  50  60    INVS
XOUTP 35  40  50  60    OUTPS
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  40   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT INVSMT  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    SMT1S
XINV  25  30  50  60    INVS
XOUTP 30  40  50  60    OUTPS
L1  80  50   3.54NH
L2  60  90   3.54NH
L3   2  20   3.54NH
L4  40   3   3.54NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS
```

```
.SUBCKT NINV1  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP1S
XINV0 25  30  50  60    INVS
XINV1 30  35  50  60    INVS
XOUTP 35  40  50  60    OUTPS
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  40   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT NANDINV 2  5  3  80  90
*INVERTING 2-NAND
*EN = 5, IN = 2, OUT = 3, VCC = 80, GND = 90
XIN1  20  25      50  60   INP2S
XIN2  30  35      50  60   INP2S
XNAND 25  35  36  50  60   NANDS
XOUT  36  40      50  60   OUTPS
L1     2  20   4.28NH
L2     5  30   4.28NH
L3    40   3   6.08NH
L4    80  50   6.08NH
L5    60  90   6.08NH
C1    20  90   1.5P
C2    30  90   1.5P
C3    40  90   1.5P
C4    50  90   1.5P
C5    60  90   1.5P
.ENDS

.SUBCKT SWI1  2  3  4  70  80  90
* INP = 2  Y = 3  Z = 4  VEE = 70  VCC = 80  GND = 90
XINP 20  25  50  60      INP2S
XLC  25  30  40  50  60  LLCS
XAS  30   3   4  40  50  SWITCH1S
L1  80  50   6.08NH
L2  70  40   6.08NH
L3  60  90   6.08NH
L4   2  20   4.28NH
C1  50  90   1.5P
C2  40  90   1.5P
C3  60  90   1.5P
C4  20  90   1.5P
C5  3   90   1.5P
C6  4   90   1.5P
.ENDS
```

```
.SUBCKT SWI2  2  3  4  80  90
* INP = 2  Y = 3  Z = 4  VCC = 80  GND = 90
XINP  20  25  50  60      INP2S
XAS   25   8   9  50  60  SWITCH2S
L1  80  50   3.53NH
L2  60  90   3.54NH
L3   2  20   3.53NH
L4   8   3   3.54NH
L5   9   4   3.54NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
C5  4   90   1.5P
.ENDS

.SUBCKT SWI3  2  3  4  70  80  90
* INP = 2  Y = 3  Z = 4  VEE = 70  VCC = 80  GND = 90
XINP 20  25  50  60      INP1S
XLC  25  30  40  50  60  LLCS
XAS  30   3   4  40  50  SWITCH3S
L1  80  50   5.97NH
L2  70  40   5.97NH
L3  60  90   5.97NH
L4   2  20   4.28NH
C1  50  90   1.5P
C2  40  90   1.5P
C3  60  90   1.5P
C4  20  90   1.5P
C5  3   90   1.5P
C6  4   90   1.5P
.ENDS

.SUBCKT NINV3  2  5  3  80  90
* INP = 2  OEN = 5(LOW)  OUT = 3  VCC = 80  GND = 90
XINP      20  25  50  60      INP2S
XINV      25  30  50  60      INVS
XBUSOUTP  30  15  35  50  60  BUSOUTPS
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   6.87NH
L4   5  15   5.97NH
L5  35   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C4  20  90   1.5P
C5  15  90   1.5P
C6   3  90   1.5P
.ENDS
```

```
******CIR_SLOW_HCT TYPES******

.SUBCKT INV0T  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP0S
XOUTP 25  30  50  60    OUTPS
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  30   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT INV1T  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP1TS
XINV  25  35  50  60    INVS
XOUTP 35  40  50  60    OUTPS
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  40   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT INV2T  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP2TS
XINV  25  35  50  60    INVS
XOUTP 35  40  50  60    OUTPS
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  40   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT INVSMTT  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    SMTTL1S
XINV  25  35  50  60    INVS
XOUTP 35  40  50  60    OUTPS
L1  80  50   3.54NH
L2  60  90   3.54NH
L3   2  20   3.54NH
L4  40   3   3.54NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS
```

```
.SUBCKT NINV1T  2  3  80 90
*IN=2, OUT=3, VCC=80, GND=90
XINP  20  25  50  60    INP1TS
XINV0 25  30  50  60    INVS
XINV1 30  35  50  60    INVS
XOUTP 35  40  50  60    OUTPS
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4  40   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
.ENDS

.SUBCKT NANDINVT 2  5  3  80  90
*INVERTING 2-NAND
*EN = 5, IN = 2, OUT = 3, VCC = 80, GND = 90
XIN1  20  25      50  60   INP2TS
XIN2  30  35      50  60   INP2TS
XNAND 25  35  36  50  60   NANDS
XOUT  36  40      50  60   OUTPS
L1     2  20   5.29NH
L2     5  30   4.28NH
L3    40   3   3.78NH
L4    80  50   6.08NH
L5    60  90   6.08NH
C1    20  90   1.5P
C2    30  90   1.5P
C3    40  90   1.5P
C4    50  90   1.5P
C5    60  90   1.5P
.ENDS

.SUBCKT SWI1T  2  3  4  70  80  90
* INP = 2  Y = 3  Z = 4  VEE = 70  VCC = 80  GND = 90
XINP 20  25  50  60      INP2TS
XLC  25  30  40  50  60  LLCS
XAS  30   3   4  40  50  SWITCH1S
L1  80  50   6.08NH
L2  70  40   6.08NH
L3  60  90   6.08NH
L4   2  20   4.28NH
C1  50  90   1.5P
C2  40  90   1.5P
C3  60  90   1.5P
C4  20  90   1.5P
C5  3   90   1.5P
C6  4   90   1.5P
.ENDS
```

```
.SUBCKT SWI2T  2  3  4  80  90
* INP = 2  Y = 3  Z = 4  VCC = 80  GND = 90
XINP  20  25  50  60      INP1TS
XAS   25   8   9  50  60  SWITCH2S
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   5.97NH
L4   8   3   5.97NH
L5   9   4   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C3  20  90   1.5P
C4  3   90   1.5P
C5  4   90   1.5P
.ENDS

.SUBCKT SWI3T  2  3  4  70  80  90
* INP = 2  Y = 3  Z = 4  VEE = 70  VCC = 80  GND = 90
XINP 20  25  50  60      INP1TS
XLC  25  30  40  50  60  LLCS
XAS  30   3   4  40  50  SWITCH3S
L1  80  50   6.08NH
L2  70  40   6.08NH
L3  60  90   6.08NH
L4   2  20   4.28NH
C1  50  90   1.5P
C2  40  90   1.5P
C3  60  90   1.5P
C4  20  90   1.5P
C5  3   90   1.5P
C6  4   90   1.5P
.ENDS

.SUBCKT NINV3T  2  5  3  80  90
*
* INP = 2  OEN = 5(LOW)  OUT = 3  VCC = 80  GND = 90
XINP      20  25  50  60      INP2TS
XINV      25  30  50  60      INVS
XBUSOUTP  30  15  35  50  60  BUSOUTPS
L1  80  50   6.87NH
L2  60  90   6.87NH
L3   2  20   6.87NH
L4   5  15   5.97NH
L5  35   3   5.97NH
C1  50  90   1.5P
C2  60  90   1.5P
C4  20  90   1.5P
C5  15  90   1.5P
C6   3  90   1.5P
.ENDS

************************************************************
```

Section 11
Packaging

SPICE

CONTENTS

Packaging

Parasitic Reactance Due to Packaging Effects

To improve the accuracy of a simulation, the user should include inductors and capacitors representing package parasitics. Parasitics are intrinsic to the connecting pins and bonding methods used in device packages. These parasitics are necessary when simulating ground bounce and ringing. They are included in the subcircuit netlists. Figure 11-1 is an illustration of the parasitics for one device pin.

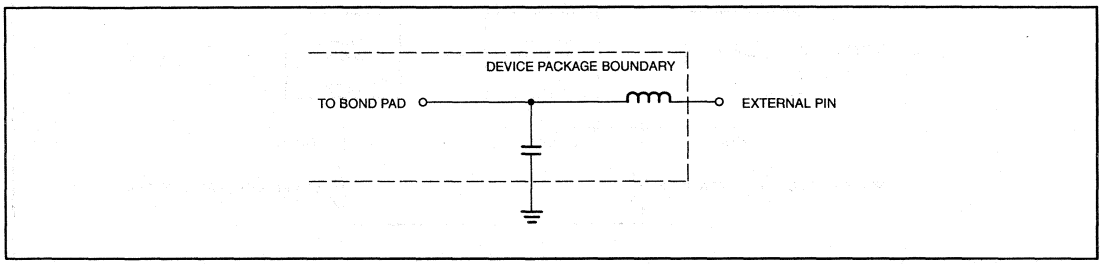


Figure 11-1. Package Model

Although the values listed for the packages are accurate, there is one value common to all circuits that is not. The interconnect metal from the outputs of the driving devices to the bonding pad is different for each device. A method to accurately determine the effects of interconnect metal is being worked on, but for now, a generalized value can only be provided. Use the following values of capacitance between each pin to system ground (Node 0):

Plastic Dual Inline Package (PDIP) = 2.0 pF

Small Outline Package (SO) = 1.5 pF

Shrink Small Outline Package (SSOP) = 1.0 pF

Thin Shrink Small Outline Package (TSSOP) = 1.0 pF

The following tables contain self inductance values for various package types. These values can be substituted for the values already in the subcircuit files when simulating a part in a particular package. Many 8-bit ABT part types and all 8-bit LVT part types have split lead frames. The split lead frame is used to reduce the effective inductance of the ground pin, thereby reducing internal switching noise and ground bounce. Notes under each table are included to determine what type of lead frame is used for the particular product family or part type.

The following example shows how to model ABT and LVT parts with the split ground pins. Refer to the subcircuit files ABTXXX.SUB and LVTXXXYY.LIB to modify the node connections for the split ground pins. PDIP, PLCC, and TSSOP packages are not modeled with split lead frames. For ABT part types, just connect SUBGND and OGND together. For LVT part types, connect INT_GND and INTOGND together.

Packaging

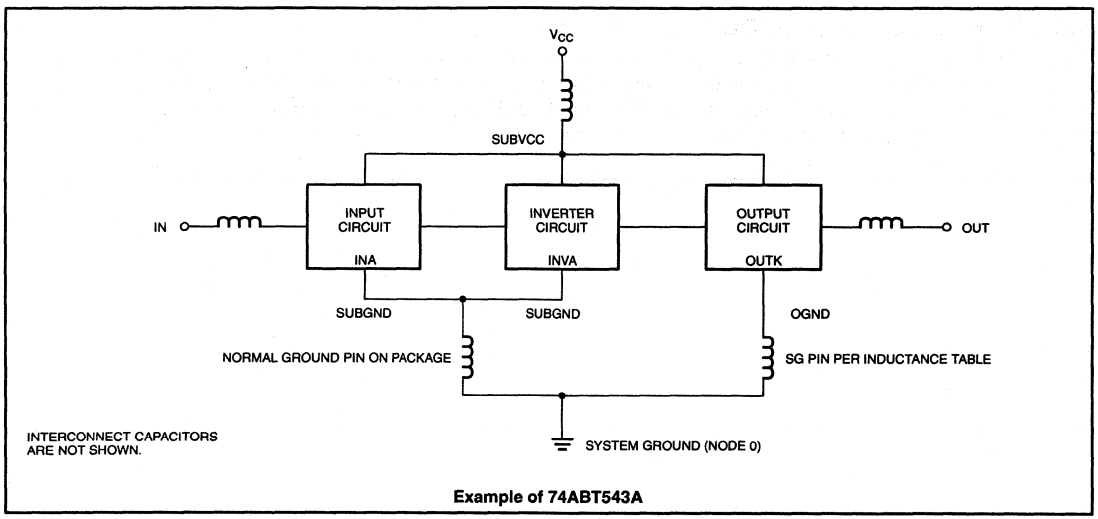


Figure 11-2. Split Ground Connections for ABT Part Types

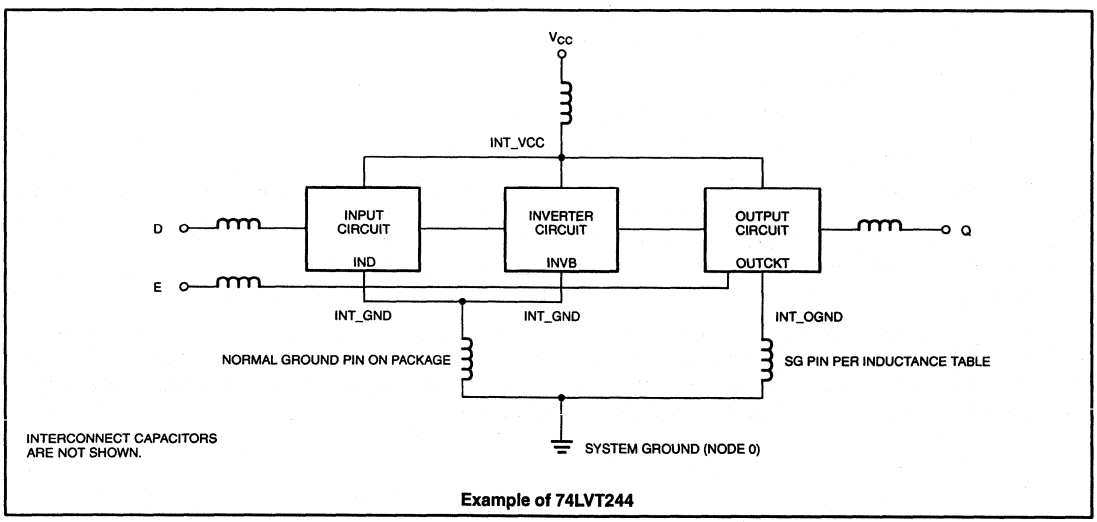


Figure 11-3. Split Ground Connections for LVT Family

Small Outline (SO) Packages

Table 11-1. 14 Pin SO Package (Normal Lead Frame)
Use for 14 pin HC(T)/LV/LVC part types and ABT5074.

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	3.53	8	3.54
2	2.55	9	2.55
3	1.79	10	1.77
4	1.49	11	1.49
5	1.77	12	1.79
6	2.55	13	2.56
7	3.54	14	3.53

Table 11-2. 14 Pin SO Package (Split Lead Frame)
Use for ABT125/126 and LVT125/126.

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	3.53	9	2.55
2	2.55	10	1.77
3	1.79	11	1.49
4	1.49	12	1.79
5	1.77	13	2.55
6	2.55	14	3.53
7	3.54	SG	3.93
8	3.54		

Table 11-3. 16 Pin SO Package (Normal Lead Frame)
Use for 16 pin HC(T)/LV/LVC part types.

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	6.08	9	6.08
2	5.29	10	5.29
3	4.28	11	4.28
4	3.78	12	3.78
5	3.78	13	3.78
6	4.28	14	4.28
7	5.29	15	5.29
8	6.08	16	6.08

Packaging

Table 11-4. 20 Pin SO Package (Normal Lead Frame)
Use for 20 pin HC(T)/LV/LVC part types ABT241/377/534/544/623

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	6.87	11	6.87
2	5.97	12	5.97
3	4.99	13	4.99
4	4.21	14	4.20
5	3.80	15	3.80
6	3.80	16	3.80
7	4.20	17	4.21
8	4.99	18	4.99
9	5.97	19	5.97
10	6.87	20	6.87

Table 11-5. 20 Pin SO Package (Split Lead Frame)
Use for 20 pin LVT part types and
ABT240/240–1/244/244–1/245/245–1/273A/373A/374A/540/541/543A/573/574/620/640

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	6.87	12	5.97
2	5.97	13	4.99
3	4.99	14	4.21
4	4.21	15	3.80
5	3.80	16	3.80
6	3.80	17	4.21
7	4.21	18	4.99
8	4.99	19	5.97
9	5.97	20	6.87
10	6.87	SG	7.61
11	6.87		

Packaging

Table 11-6. 24 Pin SO Package (Normal Lead Frame)
Use for 24 pin LVC part types and ABT648/657/863

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	7.77	13	7.77
2	6.88	14	6.88
3	5.80	15	5.80
4	4.77	16	4.77
5	4.13	17	4.13
6	3.78	18	3.78
7	3.78	19	3.78
8	4.13	20	4.13
9	4.77	21	4.77
10	5.80	22	5.80
11	6.88	23	6.88
12	7.77	24	7.77

Table 11-7. 24 Pin SO Package (Split Lead Frame)
Use for ABT646A/651/652A/821/823/827/833/841/843/845/853/861/2952/2953 and 24 pin LVT part types

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	7.77	14	6.88
2	6.88	15	5.80
3	5.80	16	4.77
4	4.77	17	4.13
5	4.13	18	3.78
6	3.78	19	3.78
7	3.78	50	4.13
8	4.13	21	4.77
9	4.77	22	5.80
10	5.80	23	6.88
11	6.88	24	7.77
12	4.03	SG	8.41
13	7.77		

Packaging

Table 11-8. 24 Pin SO Package
Use for 24 pin HLL part types

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	7.77	13	7.77
2	6.88	14	6.88
3	5.80	15	5.80
4	4.77	16	4.77
5	1.60	17	4.13
6	1.60	18	2.20
7	1.60	19	2.20
8	1.60	20	4.13
9	4.77	21	4.77
10	5.80	22	5.80
11	6.88	23	6.88
12	7.77	24	7.77

Table 11-9. 28 SO Package (Split Lead Frame)
Use for ABT899

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	8.89	16	7.54
2	7.54	17	6.46
3	6.46	18	5.61
4	5.61	19	5.04
5	5.04	20	4.45
6	4.45	21	3.94
7	3.94	22	3.94
8	3.94	23	4.45
9	4.45	24	5.04
10	5.04	25	5.61
11	5.61	26	6.46
12	6.46	27	7.54
13	7.54	28	8.79
14	8.79	SG	9.23
15	8.79		

Packaging

Table 11-10. 28 Pin SO Package
Use for 28 pin HLL part types

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	8.89	15	8.79
2	7.54	16	7.54
3	6.46	17	6.46
4	5.61	18	5.61
5	5.04	19	5.04
6	1.80	20	4.45
7	1.80	21	2.40
8	1.80	22	2.40
9	1.80	23	4.45
10	5.04	24	5.04
11	5.61	25	5.61
12	6.46	26	6.46
13	7.54	27	7.54
14	8.79	28	8.79

Shrink Small Outline Packages (SSOP)

Table 11-11. 14 Pin SSOP (Normal Lead Frame)
Use for 14 pin HC(T)/LV/LVC part types and ABT5074

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	2.65	8	2.65
2	2.07	9	2.07
3	1.82	10	1.82
4	1.76	11	1.76
5	1.82	12	1.82
6	2.07	13	2.07
7	2.65	14	2.65

Table 11-12. 14 Pin SSOP (Split Lead Frame)
Use for ABT125/126 and LVT125/126

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	2.65	9	2.07
2	2.07	10	1.82
3	1.82	11	1.76
4	1.76	12	1.82
5	1.82	13	2.07
6	2.07	14	2.65
7	2.65	SG	2.93
8	2.65		

Table 11-13. 16 Pin SSOP (Normal Lead Frame)
Use for 16 pin HC(T)/LV/LVC part types

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	3.16	9	3.16
2	2.41	10	2.41
3	1.93	11	1.93
4	1.87	12	1.87
5	1.87	13	1.87
6	1.93	14	1.93
7	2.41	15	2.41
8	3.16	16	3.16

Packaging

Table 11-14. 20 Pin SSOP (Normal Lead Frame)
Use for 20 pin HC(T)/LV/LVC part types and ABT241/377/534/544/623

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	3.11	11	3.11
2	2.47	12	2.31
3	1.87	13	1.80
4	1.61	14	1.61
5	1.63	15	1.61
6	1.61	16	1.63
7	1.61	17	1.61
8	1.80	18	1.87
9	2.31	19	2.47
10	3.11	20	3.11

Table 11-15. 20 Pin SSOP (Split Lead Frame)
Use for 20 pin LVT part types and
ABT240/240–1/244/244–1/245/245–1/273A/373A/374A/540/541/543A/573/574/620/640

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	2.80	12	2.37
2	2.36	13	2.11
3	2.10	14	1.86
4	1.85	15	1.70
5	1.70	16	1.70
6	1.70	17	1.85
7	1.85	18	2.10
8	2.10	19	2.36
9	2.36	20	2.74
10	2.80	SG	3.06
11	2.81	SV	3.07

Packaging

Table 11-16. 24 Pin SSOP (Normal Lead Frame)
Use for 24 pin LVC part types and ABT648/657/863

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	3.11	13	3.11
2	2.46	14	2.46
3	1.91	15	1.91
4	1.61	16	1.61
5	1.64	17	1.64
6	1.64	18	1.64
7	1.64	19	1.64
8	1.64	20	1.64
9	1.61	21	1.61
10	1.92	22	1.91
11	2.46	23	2.46
12	3.11	24	3.11

Table 11-17. 24 Pin SSOP (Split Lead Frame)
Use for ABT646A/651/652A/821/823/827/833/841/843/845/853/861/2952/2953 and 24 pin LVT part types

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	3.36	14	2.87
2	2.87	15	2.33
3	2.33	16	1.97
4	1.98	17	1.83
5	1.84	18	1.69
6	1.69	19	1.69
7	1.69	20	1.84
8	1.83	21	1.98
9	1.97	22	2.33
10	2.33	23	2.86
11	2.87	24	3.34
12	3.36	SG	3.69
13	3.36	SV	3.69

Table 11-18. 28 Pin SSOP
Use for 74HL33646/952

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	3.52	15	3.52
2	2.72	16	2.72
3	2.00	17	2.00
4	1.49	18	1.49
5	1.49	19	1.49
6	1.49	20	1.49
7	1.49	21	1.49
8	1.49	22	1.49
9	1.49	23	1.49
10	1.49	24	1.49
11	1.49	25	1.49
12	2.00	26	2.00
13	2.72	27	2.72
14	3.52	28	3.52

Table 11-19. 48 Pin SSOP
Use for ABT16/ALVC/LVT16

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	6.56	25	6.56
2	5.78	26	5.78
3	5.13	27	5.13
4	4.52	28	4.52
5	3.68	29	3.68
6	3.28	30	3.28
7	2.93	31	2.93
8	2.68	32	2.68
9	2.43	33	2.43
10	2.27	34	2.27
11	2.09	35	2.09
12	2.01	36	2.00
13	2.01	37	2.00
14	2.09	38	2.09
15	2.27	39	2.27
16	2.43	40	2.43
17	2.68	41	2.68
18	2.93	42	2.93
19	3.28	43	3.28
20	3.68	44	3.68
21	4.52	45	4.52
22	5.13	46	5.13
23	5.78	47	5.78
24	6.56	48	6.56

Packaging

Table 11-20. 56 Pin SSOP
Use for ABT16/ALVC/LVT16

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	6.14	29	6.14
2	5.40	30	5.40
3	4.64	31	4.64
4	3.88	32	3.88
5	3.07	33	3.07
6	2.48	34	2.48
7	2.08	35	2.08
8	2.04	36	2.04
9	1.63	37	1.62
10	1.50	38	1.50
11	1.29	39	1.29
12	1.14	40	1.14
13	0.99	41	0.99
14	1.00	42	1.00
15	1.00	43	1.00
16	0.99	44	0.99
17	1.14	45	1.14
18	1.29	46	1.29
19	1.50	47	1.50
20	1.63	48	1.63
21	2.05	49	2.05
22	2.08	50	2.08
23	2.48	51	2.48
24	3.07	52	3.07
25	3.88	53	3.88
26	4.64	54	4.64
27	5.41	55	5.40
28	6.15	56	6.14

Thin Shrink Small Outline Packages (TSSOP)

Table 11-21. 14 Pin TSSOP
Use for 14 pin ABT/HC(T)/LV/LVC/LVT part types

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	2.32	8	2.32
2	2.04	9	2.04
3	1.36	10	1.36
4	1.38	11	1.38
5	1.36	12	1.36
6	2.04	13	2.04
7	2.32	14	2.31

Table 11-22. 16 Pin TSSOP
Use for 16 pin HC(T)/LV/LVC part types

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	2.40	9	2.40
2	1.93	10	1.93
3	1.76	11	1.76
4	1.65	12	1.65
5	1.65	13	1.65
6	1.76	14	1.76
7	1.93	15	1.93
8	2.40	16	2.40

Table 11-23. 20 Pin TSSOP
Use for 20 pin ABT/HC(T)/LV/LVC/LVT part types

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	2.29	11	2.29
2	1.71	12	1.72
3	1.31	13	1.31
4	1.32	14	1.32
5	1.27	15	1.27
6	1.27	16	1.27
7	1.31	17	1.32
8	1.31	18	1.31
9	1.72	19	1.72
10	2.29	20	2.29

Table 11-24. 24 Pin TSSOP
Use for 24 pin ABT/HLL/LVC/LVT part types

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	2.40	13	2.40
2	1.83	14	1.83
3	1.33	15	1.33
4	1.19	16	1.19
5	1.20	17	1.20
6	1.33	18	1.13
7	1.33	19	1.13
8	1.20	20	1.20
9	1.19	21	1.19
10	1.33	22	1.33
11	1.83	23	1.83
12	2.40	24	2.40

Table 11-25. 48 Pin TSSOP
Use for 48 pin ALVC/ABT16/LVT16 part types

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	7.29	25	7.29
2	6.60	26	6.60
3	6.00	27	6.00
4	5.38	28	5.38
5	4.77	29	4.77
6	4.16	30	4.16
7	3.96	31	3.96
8	3.77	32	3.77
9	3.57	33	3.57
10	3.44	34	3.44
11	3.36	35	3.36
12	3.33	36	3.33
13	3.33	37	3.33
14	3.36	38	3.36
15	3.44	39	3.44
16	3.57	40	3.57
17	3.77	41	3.77
18	3.96	42	3.96
19	4.16	43	4.16
20	4.77	44	4.77
21	5.38	45	5.38
22	6.00	46	6.00
23	6.60	47	6.60
24	7.29	48	7.29

Packaging

Table 11-26. 56 Pin TSSOP
Use for 56 pin ABT16/ALVC/LVT16 part types

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	7.61	29	7.61
2	7.08	30	7.08
3	6.49	31	6.49
4	5.96	32	5.96
5	5.38	33	5.38
6	4.93	34	4.93
7	4.50	35	4.50
8	4.27	36	4.27
9	3.91	37	3.91
10	3.69	38	3.69
11	3.30	39	3.46
12	3.30	40	3.30
13	3.15	41	3.15
14	3.09	42	3.09
15	3.09	43	3.09
16	3.15	44	3.15
17	3.30	45	3.30
18	3.46	46	3.46
19	3.69	47	3.69
20	3.91	48	3.91
21	4.27	49	4.27
22	4.50	50	4.50
23	4.93	51	4.93
24	5.38	52	5.38
25	5.96	53	5.96
26	6.49	54	6.49
27	7.08	55	7.08
28	7.61	56	7.61

Plastic Leaded Chip Carrier (PLCC) Package

Table 11-27. 28 Pin PLCC
Use for ABT899

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	4.46	15	4.44
2	4.37	16	4.37
3	4.73	17	5.22
4	5.22	18	5.22
5	5.21	19	5.21
6	4.72	20	4.72
7	4.36	21	4.36
8	4.21	22	4.21
9	4.36	23	4.36
10	4.72	24	4.72
11	5.21	25	5.21
12	5.22	26	5.22
13	4.73	27	4.73
14	4.37	28	4.37

Plastic Dual Inline Packages (PDIP)

Table 11-28. 14 Pin PDIP
Use for 14 pin ABT/HC(T)/LV part types

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	6.02	8	7.23
2	4.00	9	5.19
3	2.57	10	3.32
4	2.33	11	2.33
5	3.32	12	2.57
6	5.19	13	4.00
7	7.23	14	6.02

Table 11-29. 16 Pin PDIP
Use for 16 pin HC(T)/LV part types

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	7.14	9	7.14
2	4.98	10	4.98
3	3.55	11	3.55
4	2.73	12	2.73
5	2.73	13	2.73
6	3.55	14	3.55
7	4.98	15	4.98
8	7.14	16	7.14

Table 11-30. 20 Pin PDIP
Use for 20 pin ABT/HC(T)/LV part types

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	9.14	11	9.15
2	6.98	12	6.99
3	4.91	13	4.91
4	3.58	14	3.59
5	2.79	15	2.79
6	2.79	16	2.79
7	3.58	17	3.59
8	4.91	18	4.91
9	6.98	19	6.99
10	9.14	20	9.14

Packaging

Table 11-31. 24 Pin PDIP
Use for 24 pin ABT/LVC part types

Pin Number	Inductance (nH)	Pin Number	Inductance (nH)
1	15.10	13	14.50
2	12.20	14	11.70
3	9.54	15	8.96
4	7.44	16	6.95
5	5.31	17	4.66
6	3.73	18	3.41
7	3.41	19	3.27
8	4.66	20	5.31
9	6.95	21	7.44
10	8.96	22	9.58
11	11.70	23	12.20
12	14.50	24	15.10

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